Sup*IR*Buck™

USER GUIDE FOR Vtt RAIL EVALUATION BOARD USING IR3898

DESCRIPTION

The IR3898 is a synchronous buck converter, providing a compact, high performance and flexible solution in a small 4mm X 5 mm Power QFN package.

Key features offered by the IR3898 include internal Digital Soft Start/Soft Stop, precision 0.5Vreference voltage, Power Good, thermal protection, programmable switching frequency, Enable input, input under-voltage lockout for proper start-up, enhanced line/ load regulation with feed forward, external frequency synchronization with smooth clocking, internal LDO and pre-bias start-up.

Pulse by pulse current limit and output over-current protection function is implemented by sensing the voltage developed across the on-resistance of the synchronous rectifier MOSFET for optimum cost and performance and the current limit is thermally compensated.

This user guide contains the schematic and bill of materials for the IR3898 evaluation board. The guide describes operation and use of the evaluation board itself. Detailed application information for IR3898 is available in the IR3898 data sheet.

BOARD FEATURES

- V_{in} = +1.5V (1.35Vminimum)
- V_{out} = +0.75V @ 0- 4.3A (+0.675V@0-4.3A)
- F_s=600KHz
- L= 1.0uH
- C_{in}= 3x22uF (ceramic 805)
- C_{out}=4x22uF (Ceramic 0805)

CONNECTIONS and OPERATING INSTRUCTIONS

A well regulated +1.5V input supply should be connected to VIN+ and VIN-. A maximum of 4.3A load should be connected to VOUT+ and VOUT-. The inputs and output connections of the board are listed in Table I.

IR3898 has an internal LDO which generates Vcc from Vin. To use internal LDO, 12V input should be connected between Vin pin and PGnd. (Vin can be applied across C32 capacitor.)

If operation with external Vcc is required, then external Vcc can be applied between Vcc+ and Vcc- pins. Vin pin and Vcc/LDOout pins should be shorted together for external Vcc operation.

External Enable signal must be applied to the board between Enable and Agnd pins.

Table I. Connections

Connection	Signal Name
VIN+	Vin (+12V)
VIN-	Ground of Vin
Vout+	Vout(+1V0)
Vout-	Ground for Vout
Vcc+	Vcc/ LDO_out Pin
Vcc-	Ground for Vcc input
Enable	Enable
P_Good	Power Good Signal
AGnd	Analog ground

LAYOUT

The PCB is a 4-layer board. All layers use 2 Oz. copper. The IR3898 and other major power components are mounted on the top side of the board.

Power supply decoupling capacitors, the bootstrap capacitor and feedback components are located close to IR3898. To improve efficiency, the circuit board is designed to minimize the length of the on-board power ground current path.

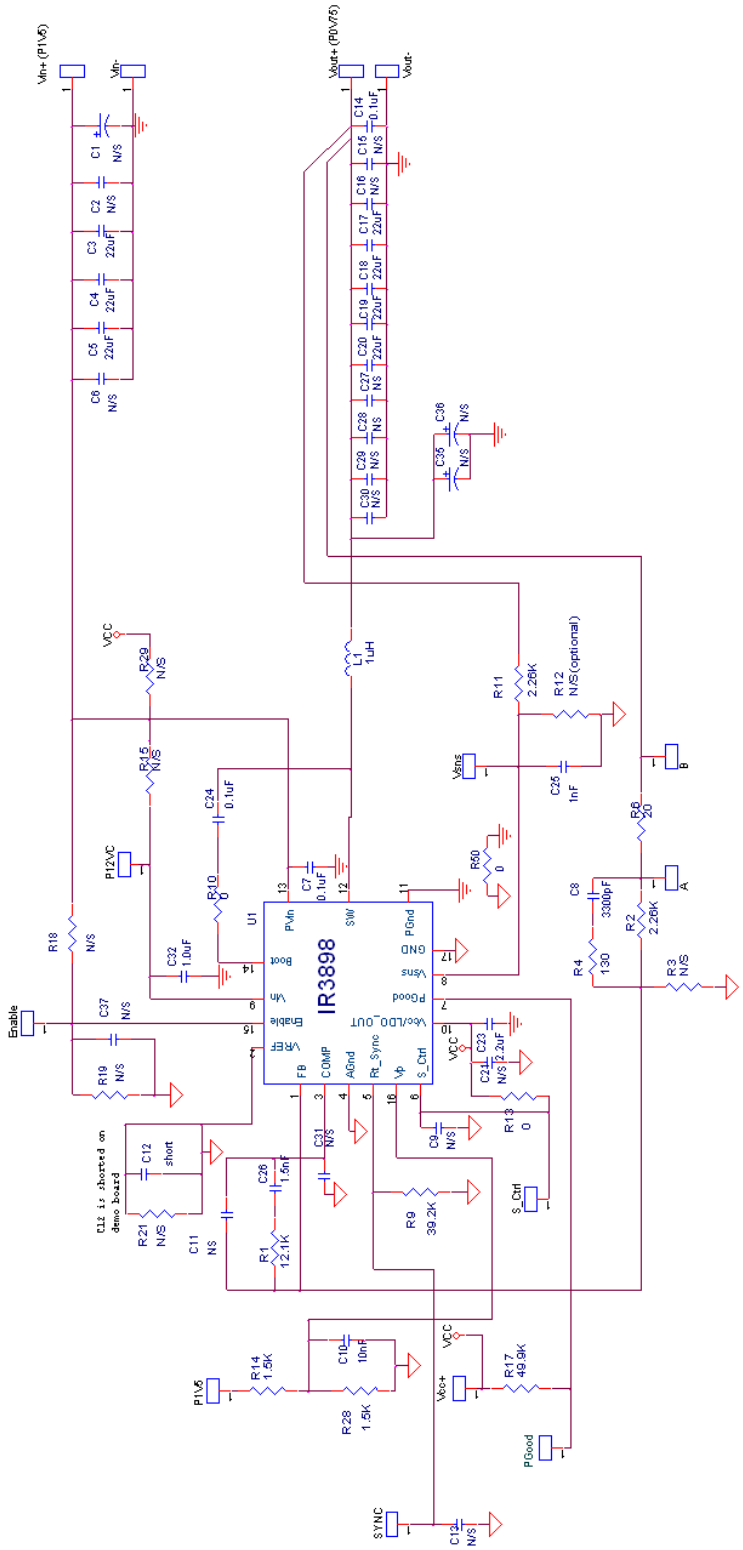

Fig. 1: Schematic of the IR3898 evaluation board

This evaluation board is a preliminary version meant for the engineering evaluation of the IR3898. Based on the results of the continuing evaluation, this board can evolve and change without notice

Bill of Materials

Item	Qty	Part Reference	Value	Description	Manufacturer	Part Number
1	3	C7 C14 C24	0.1uF	0603, 25V, X7R, 10%	Murata	GRM188R71E104KA01B
2	1	C8	3300pF	0603,50V,X7R	Murata	GRM188R71H332KA01B
3	1	C11	39pF	0603, 50V, NP0, 5%	Murata	GRM1885C1H390JA01D
6	4	C17 C18 C19 C20	22uF	0805, 6.3V, X5R, 20%	TDK	C2012X5R0J226M
7	1	C23	2.2uF	0603, 16V, X5R, 20%	TDK	C1608X5R1C225M
8	1	C26	1.5nF	0603, 25V, X7R, 10%	Murata	GRM188R71E152KA01J
9	1	C25	1nF	0603, 25V, X7R, 10%	Murata	GRM188R71E102KA01J
10	1	C10	10nF	0603, 25V, X7R, 10%	Murata	GRM188R71E103KA01J
11	1	C32	1.0uF	0603, 25V, X5R, 10%	Murata	GRM188R61E105KA12D
12	1	L1	1uh	SMD 7.1x6.5x5mm,4.7mΩ	TDK	SPM6550T-1R0M
13	1	R1	12.1K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1212V
14	2	R2 R11	2.26K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF2261V
15	1	R4	130	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF2100V
16	1	R6	20	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF20R0V
17	1	R9	39.2K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF3922V
18	5	R10 R13 R14 R15 R50	0	Thick Film, 0603,1/10W	Panasonic	ERJ-3GEY0R00V
19	2	R14 R28	1.5K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF1501V
20	1	R17	49.9K	Thick Film, 0603,1/10W,1%	Panasonic	ERJ-3EKF4992V
21	1	U1	IR3898	PQFN 4x5mm	IR	IR3898MPBF

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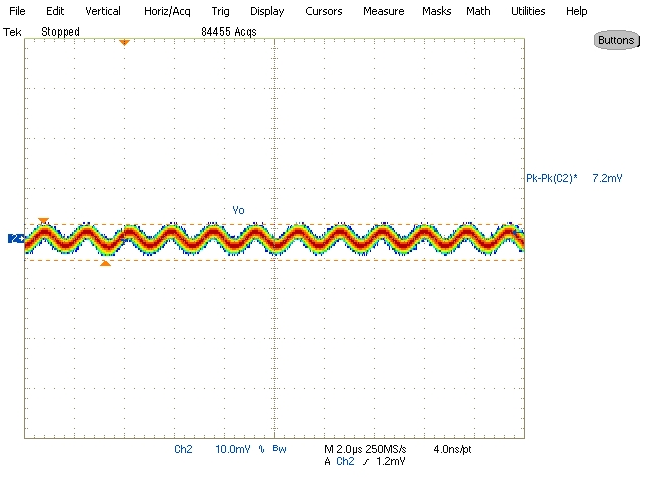
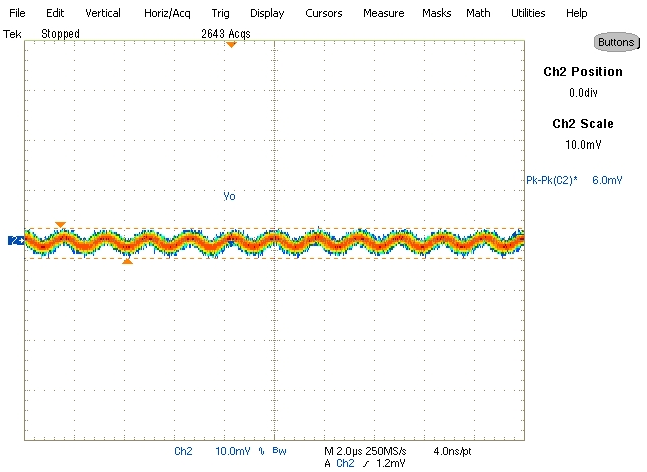
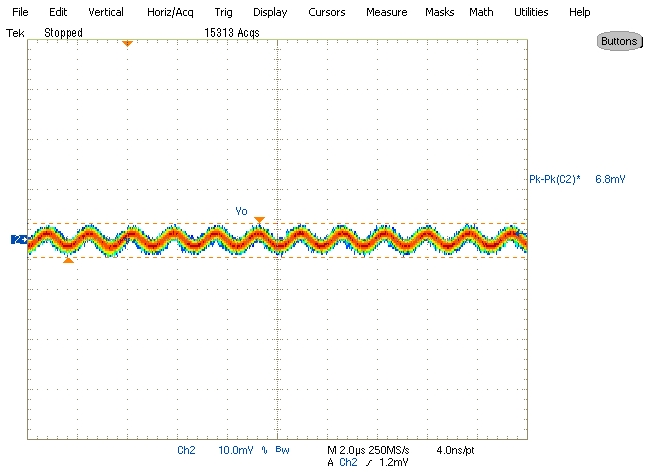
1) Output Ripple Voltage



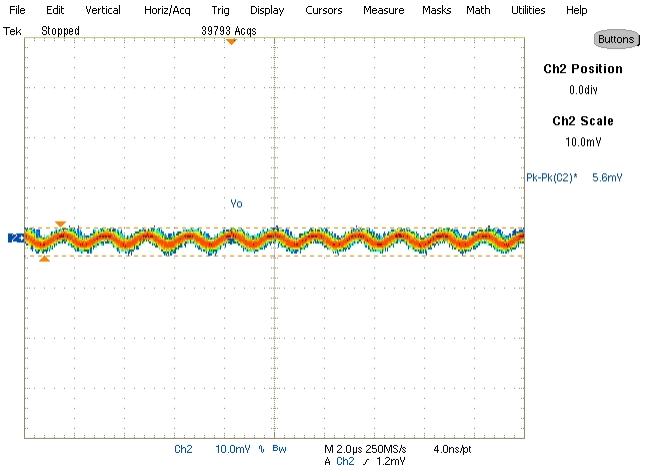
O/P Ripple Voltage-Sourcing mode
Vin-1.5V Vout-0.75V/4.3A



O/P Ripple Voltage-Sinking mode
Vin-1.5V Vout-0.75V/4.3A



O/P Ripple Voltage-Sourcing mode
Vin-1.35V Vout-0.675V/4.3A



O/P Ripple Voltage-Sinking mode
Vin-1.35V Vout-0.675V/4.3A

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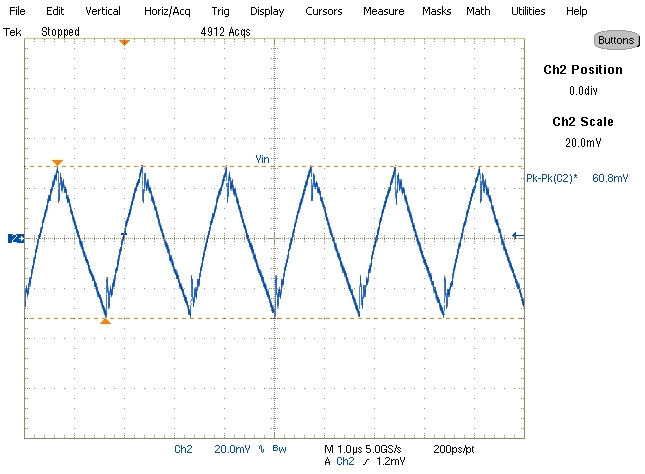
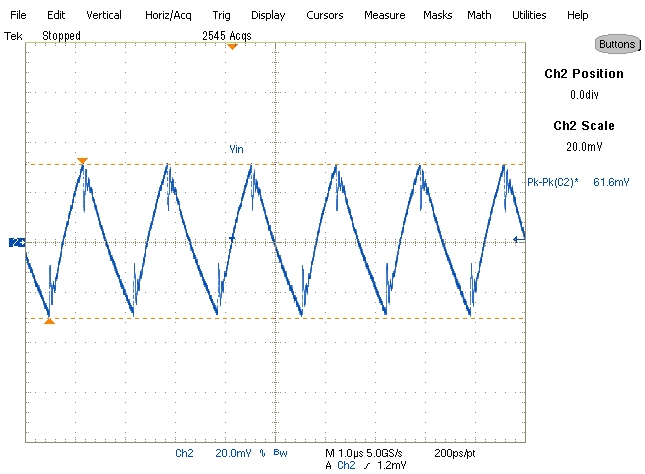
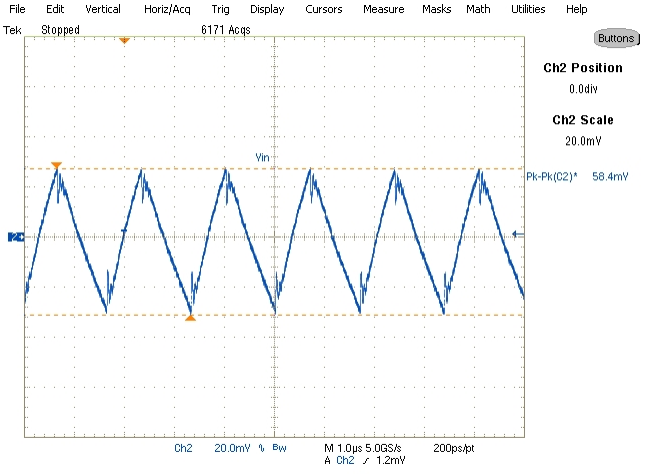
2) Input Ripple Voltage



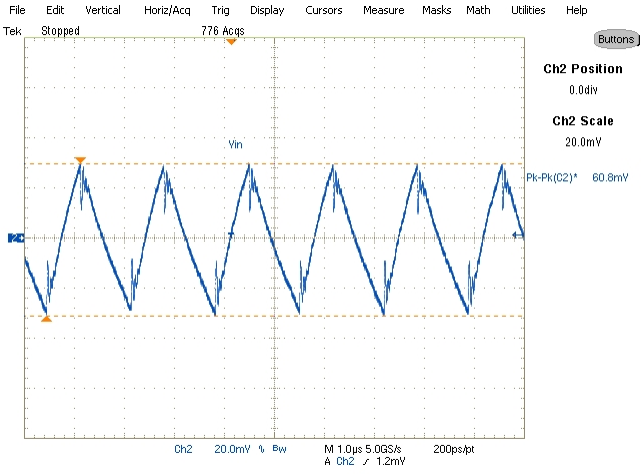
I/P Ripple Voltage-Sourcing mode
Vin-1.5V Vout-0.75V/4.3A



I/P Ripple Voltage-Sinking mode
Vin-1.5V Vout-0.75V/4.3A

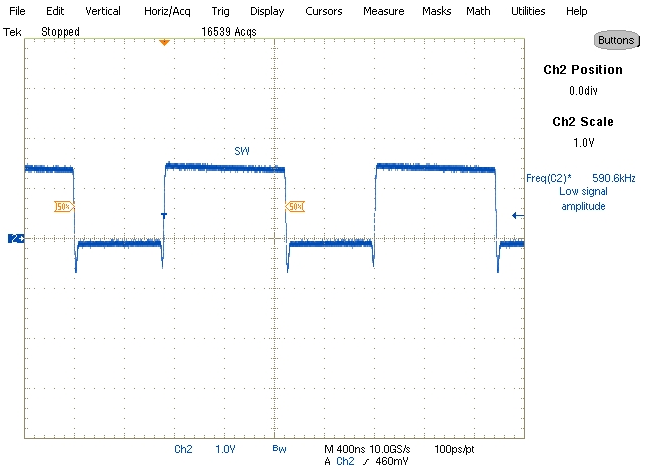


I/P Ripple Voltage-Sourcing mode
Vin-1.35V Vout-0.675V/4.3A

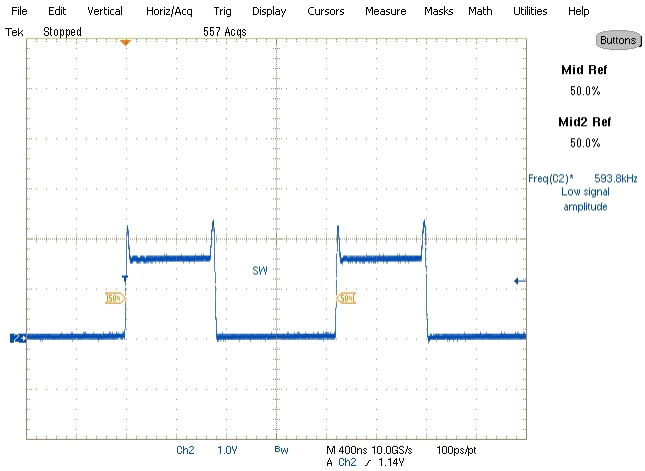


I/P Ripple Voltage-Sinking mode
Vin-1.35V Vout-0.675V/4.3A

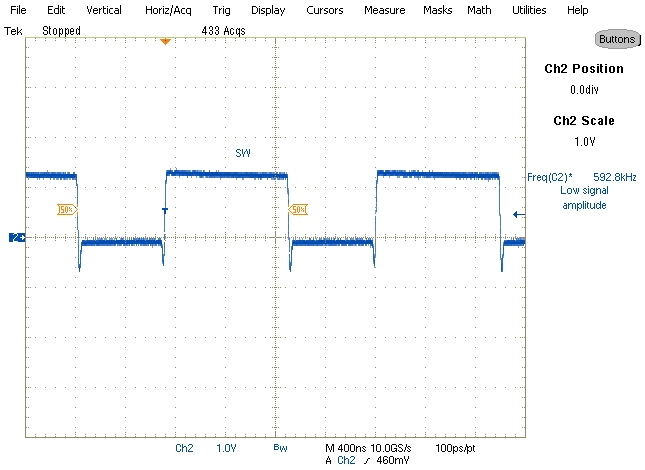
3) Switch Node Voltage



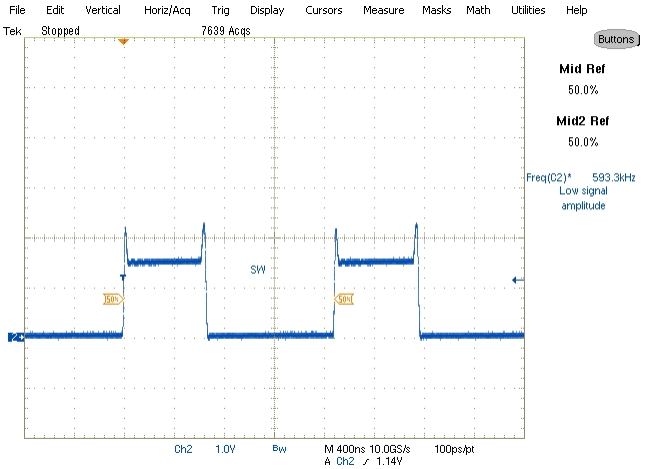
Switch node Voltage (20MHz BW)-Sourcing mode
Vin-1.5V Vout-0.75V/4.3A



Switch node Voltage (20MHz BW)-Sinking mode
Vin-1.5V Vout-0.75V/4.3A



Switch node Voltage (20MHz BW)-Sourcing mode
Vin-1.35V Vout-0.675V/4.3A



Switch node Voltage (20MHZ BW)-Sinking mode
Vin-1.35V Vout-0.675V/4.3A

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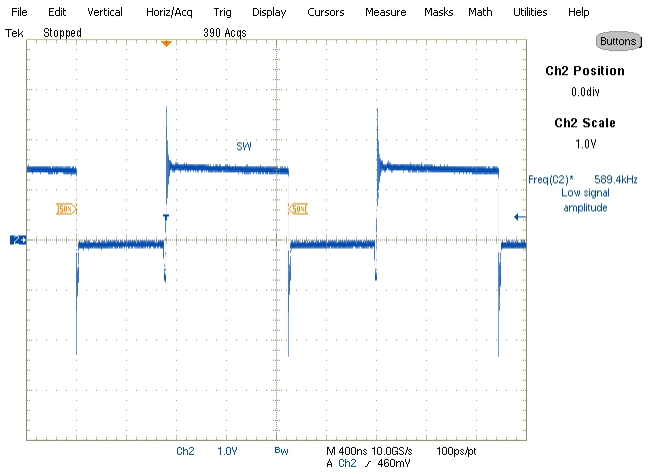
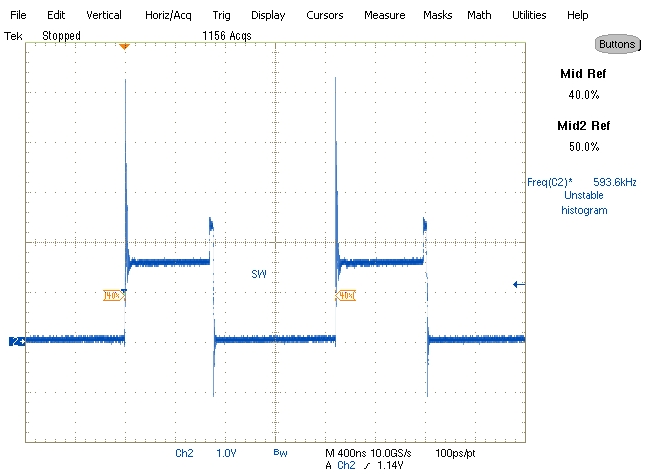
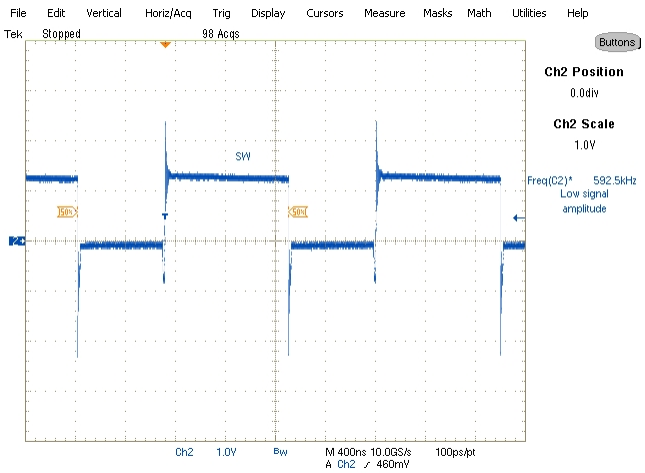


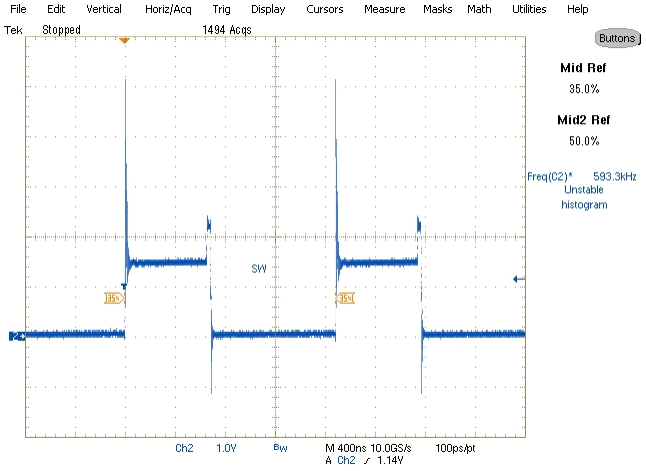
Switch node Voltage (250MHz BW)-Sourcing mode
Vin-1.5V Vout-0.75V/4.3A



Switch node Voltage (250MHZ BW)-Sinking mode
Vin-1.5V Vout-0.75V/4.3A



Switch node Voltage (250MHz BW)-Sourcing mode
Vin-1.35V Vout-0.675V/4.3A



Switch node Voltage (250MHZ BW)-Sinking mode
Vin-1.35V Vout-0.675V/4.3A

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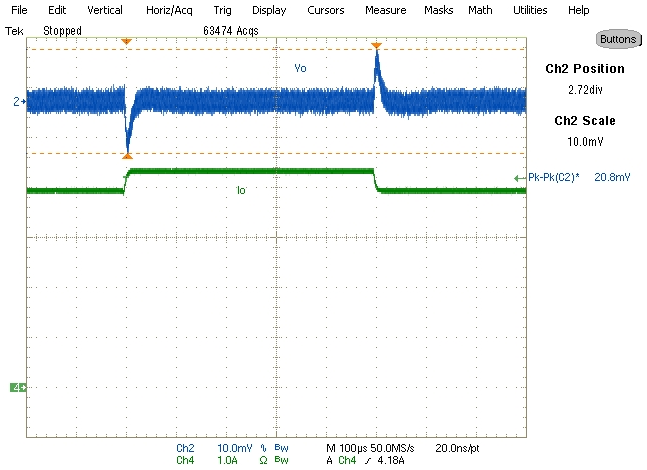
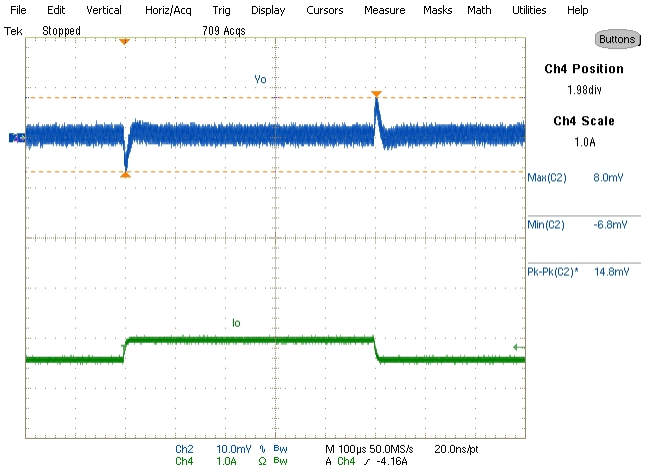
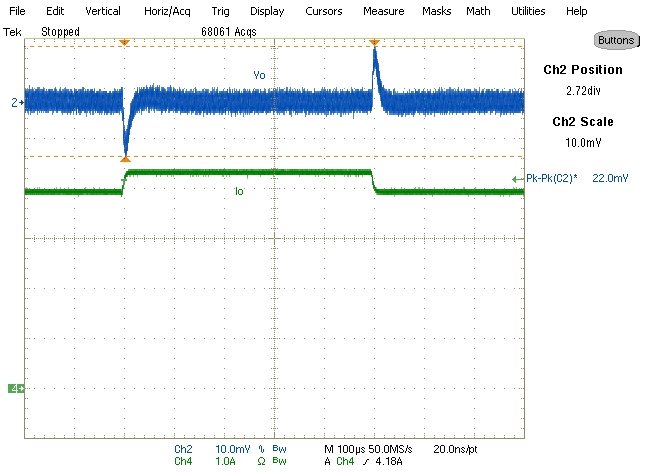
4) Transient Response



Transient response-Sourcing mode
Vin-1.5V Vout-0.75V/3.9-4.3-3.9A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)



Transient response-Sinking mode
Vin-1.5V Vout-0.75V/3.9-4.3-3.9A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)



Transient response-Sourcing mode
Vin-1.35V Vout-0.675V/3.9-4.3-3.9A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)

Transient response-Sinking mode
Vin-1.35V Vout-0.675V/3.9-4.3-3.9A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)

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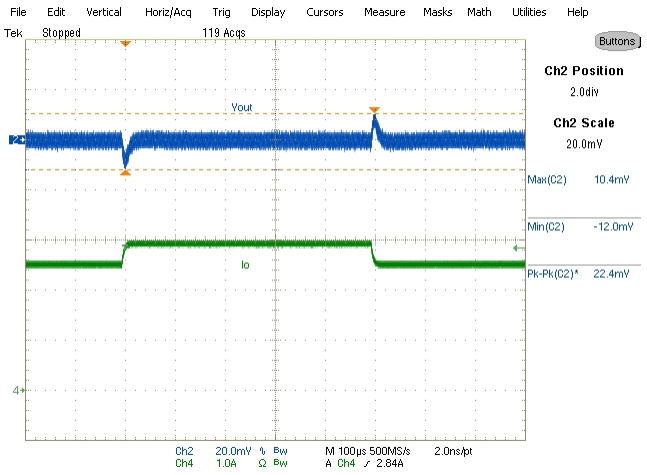
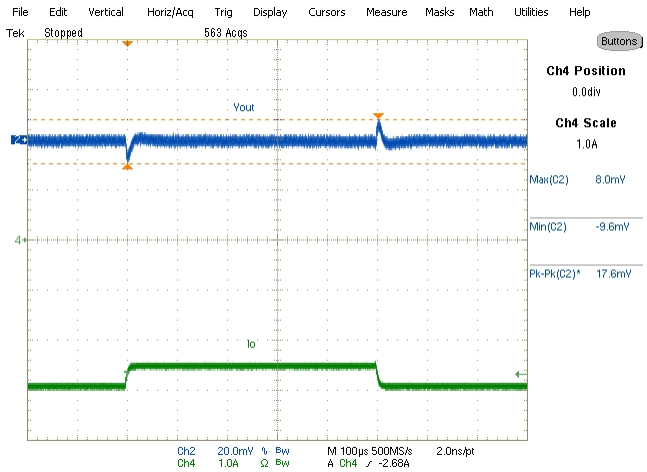
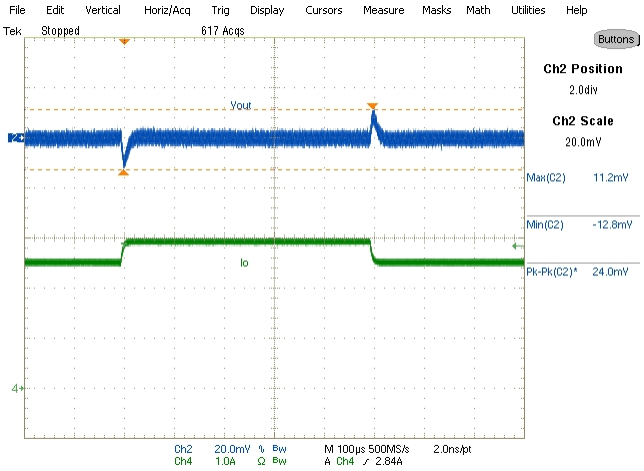


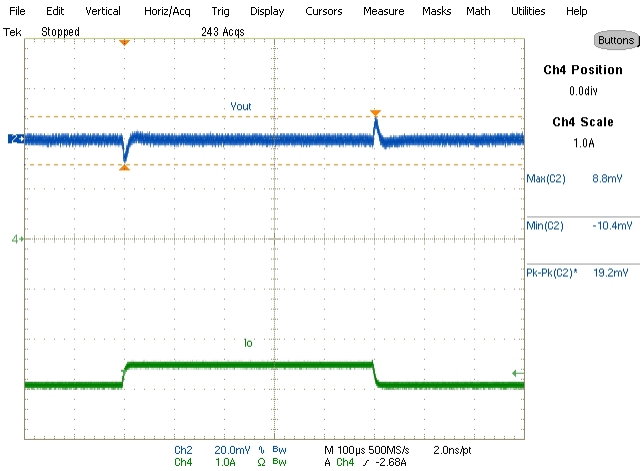
Transient response-Sourcing mode
Vin-1.5V Vout-0.75V/2.5-2.9-2.5A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)



Transient response-Sourcing mode
Vin-1.5V Vout-0.75V/2.5-2.9-2.5A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)



Transient response-Sourcing mode
Vin-1.35V Vout-0.675V/2.5-2.9-2.5A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)



Transient response-Sinking mode
Vin-1.35V Vout-0.675V/2.5-2.9-2.5A
Ch4-Vout Ch3-Iout (1A/µSec slew rate)

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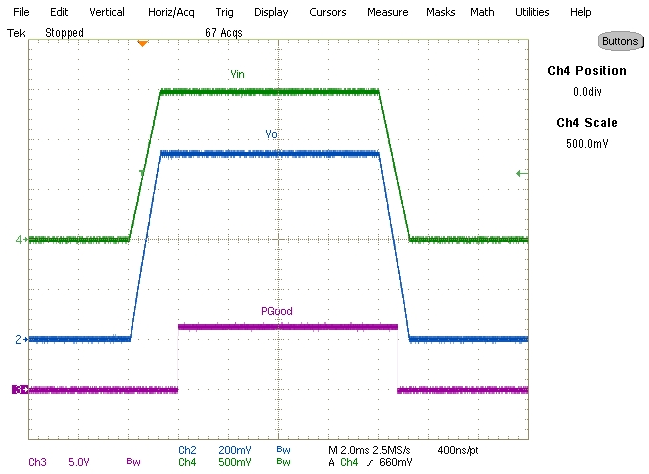
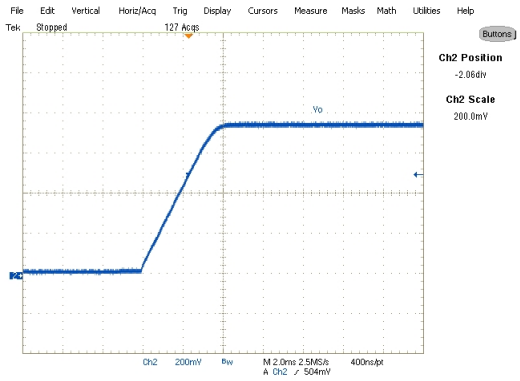
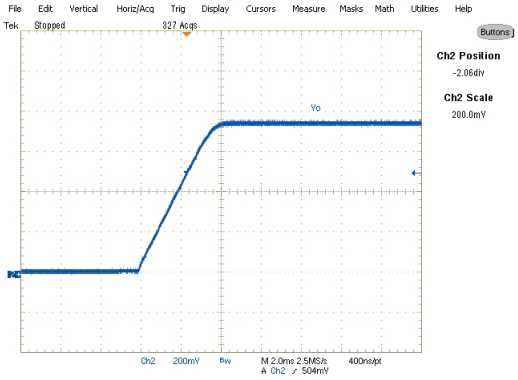
5) Turn on Waveforms



Tracking mode operation
Ch1-PGood Ch3-Vin Ch4-Vout



Turn on-Vin-1.5V Vout-0.75V/No load
Ch4-Vout



Turn on-Vin-1.5V Vout-0.75V/4.3A
Ch4-Vout

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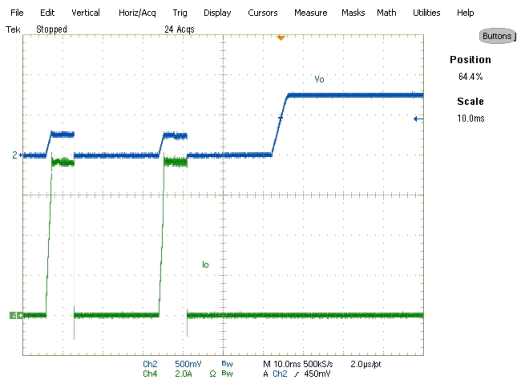
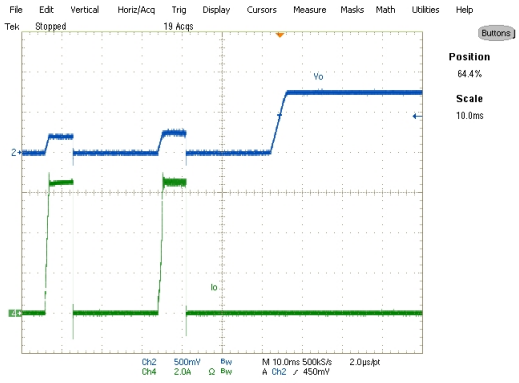
6) Over Current Protection

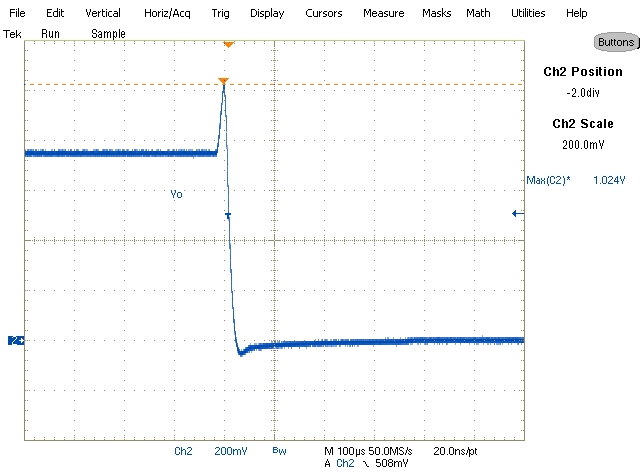


Recovery after OCP- Vcc-6.4V
Ch3-Iout Ch4-Vout



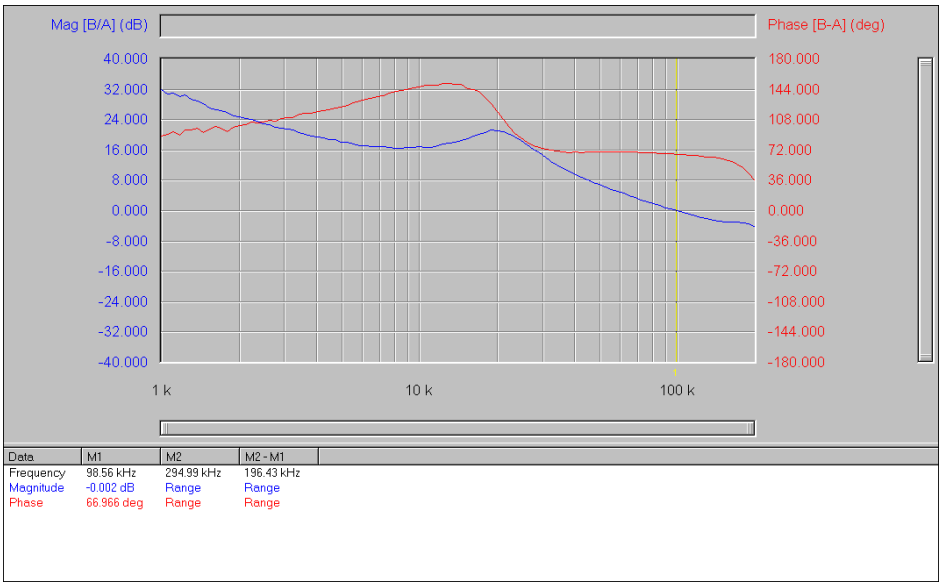
Recovery after OCP- Vcc-5.0V
Ch3-Iout Ch4-Vout

7) Over Voltage Protection

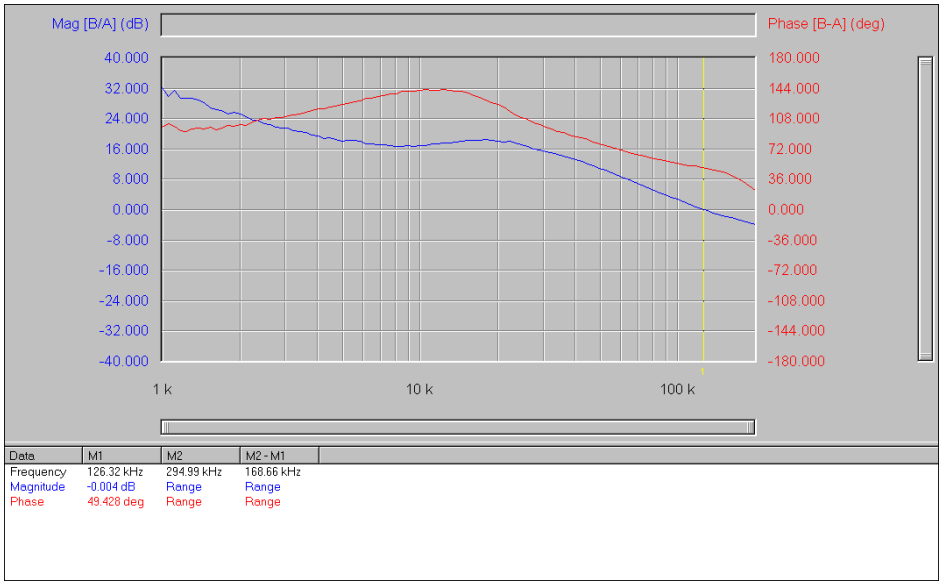


Feedback loop shorted to ground to test OVP
OVP is at 0.968V.

8) Bode Plots

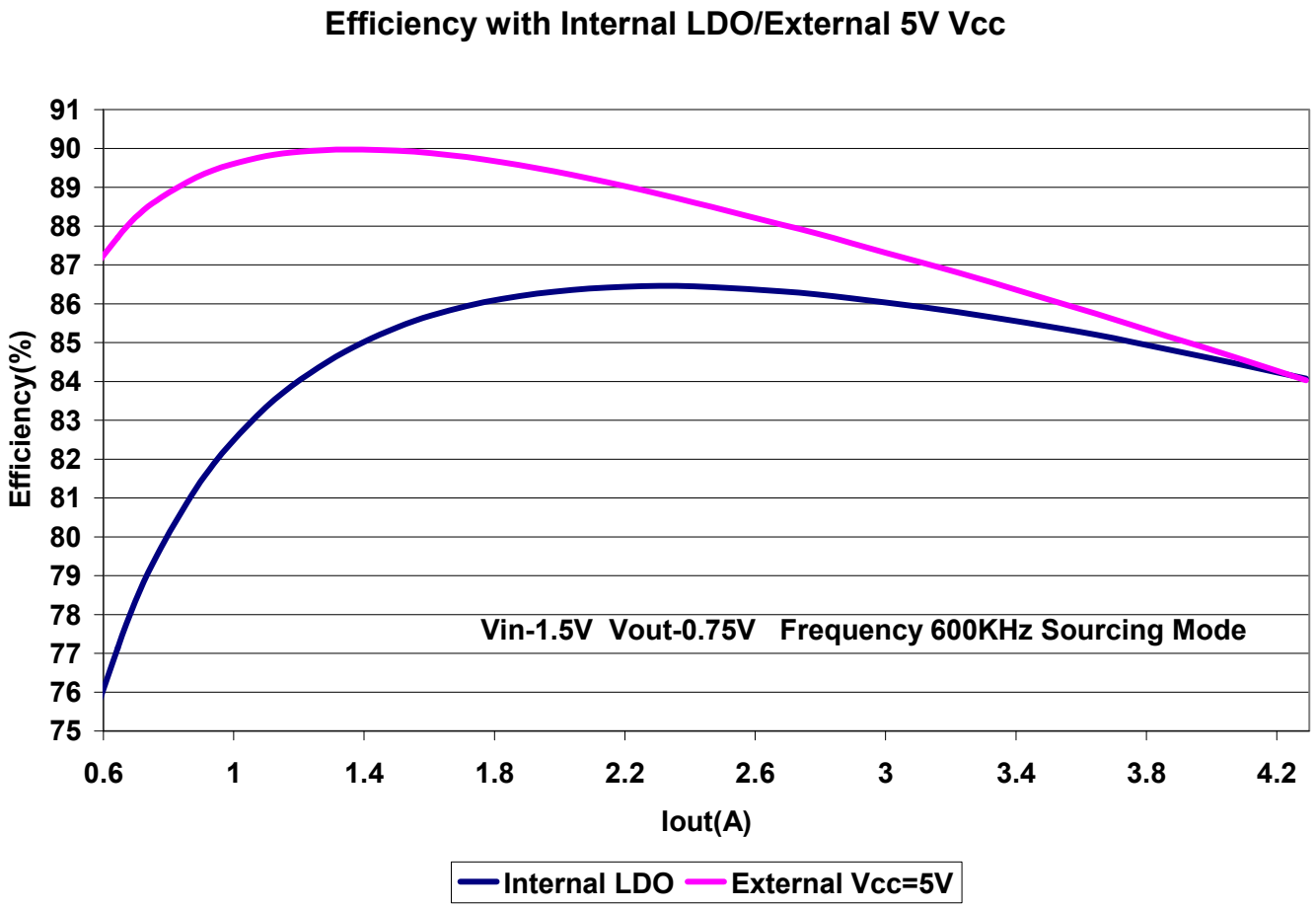


Bode plot-Sourcing mode
Vin-1.5V Vout-0.75V/4.3A



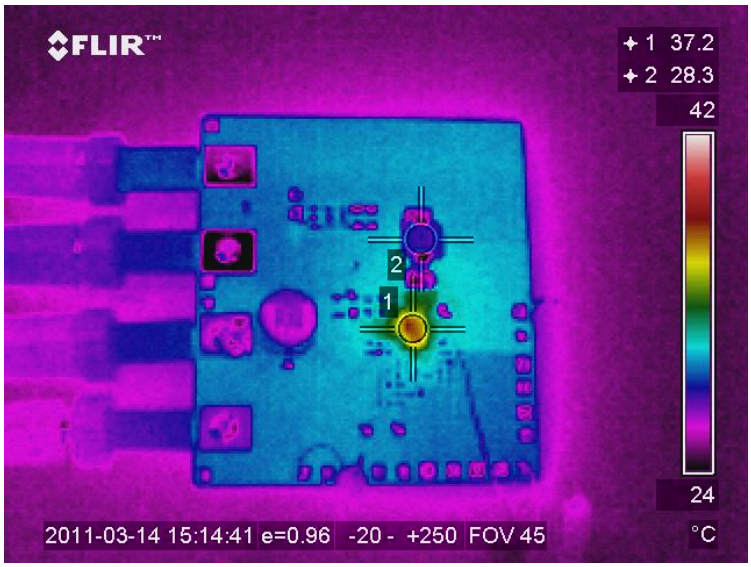
Bode plot-Sinking mode
Vin-1.5V Vout-0.75V/4.3A

9) Efficiency



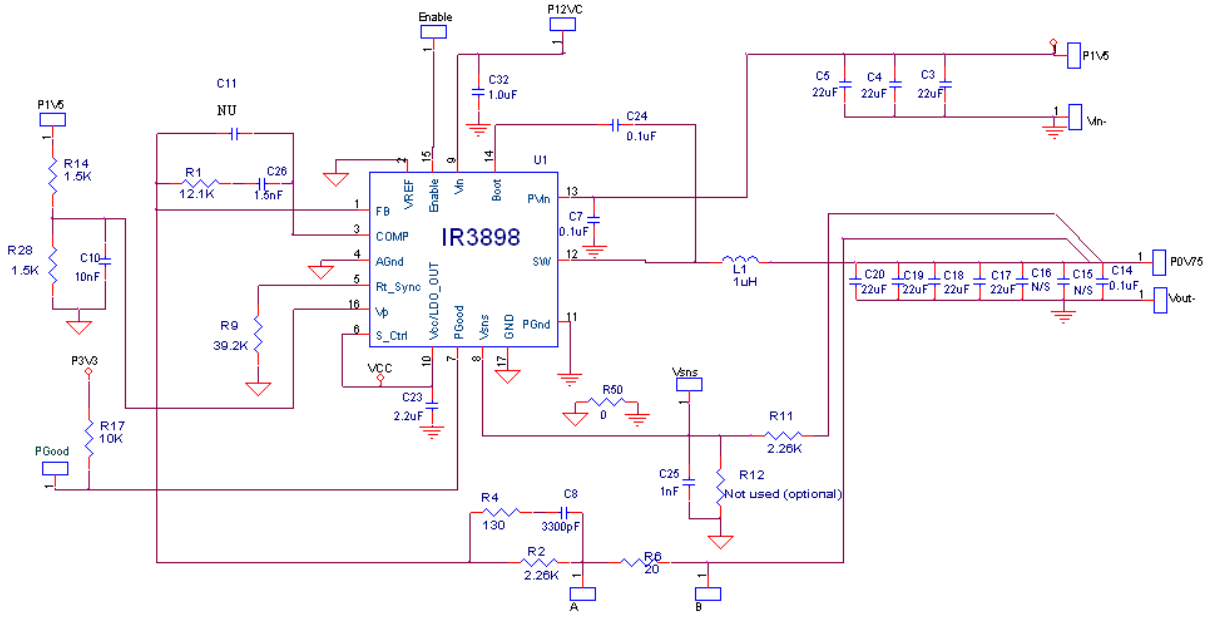
Efficiency with Vin-1.5V Vout-0.75V/4.3A with Vcc/ Internal LDO power dissipation

10) Thermal Image



Thermal image at room amb. with no air flow
Vin-1.5V Vout-0.75V/4.3A with Internal LDO (sourcing mode)
Spot 1 is IC and Spot 2 is inductor

11) Schematic



Note : Inductor used is 1.0uH, 4.7mΩ from TDK (SPM6550T-1R0)

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12) Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

Make the connections for the power components in the top layer with wide, copper filled areas or polygons. In general, it is desirable to make proper use of power planes and polygons for power distribution and heat dissipation.

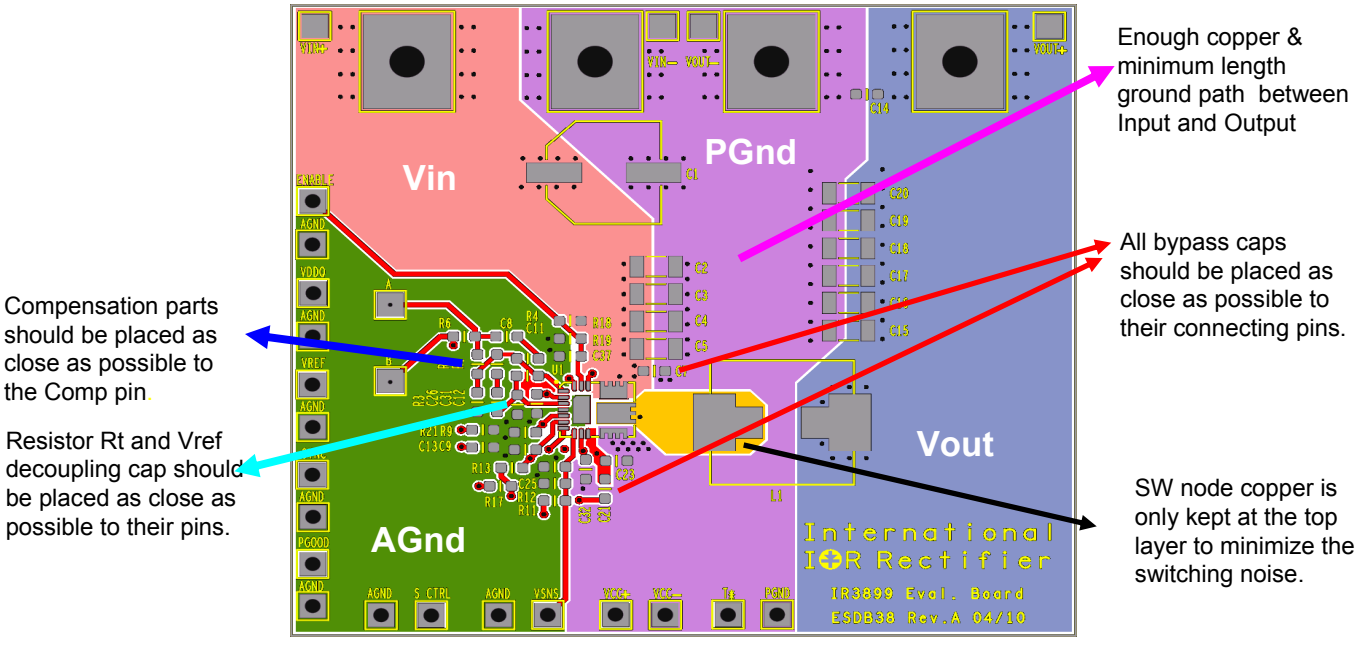
The inductor, output capacitors and the IR3898 should be as close to each other as possible. This helps to reduce the EMI radiated by the power traces due to the high switching currents through them. Place the input capacitor directly at the PVin pin of IR3898.

The feedback part of the system should be kept away from the inductor and other noise sources.

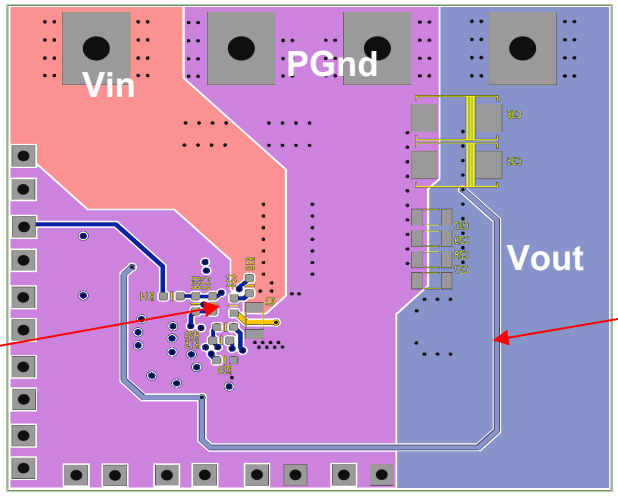
The critical bypass components such as capacitors for Vin, Vcc and Vref should be close to their respective pins. It is important to place the feedback components including feedback resistors and compensation components close to Fb and Comp pins.

In a multilayer PCB use one layer as a power ground plane and have a control circuit ground (analog ground), to which all signals are referenced. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function. These two grounds must be connected together on the PC board layout at a single point. It is recommended to place all the compensation parts over the analog ground plane in top layer.

The Power QFN is a thermally enhanced package. Based on thermal performance it is recommended to use at least a 4-layers PCB. To effectively remove heat from the device the exposed pad should be connected to the ground plane using vias. Figure 43 illustrates the implementation of the layout guidelines outlined above, on the IRDC3899 4 layer demoboard.



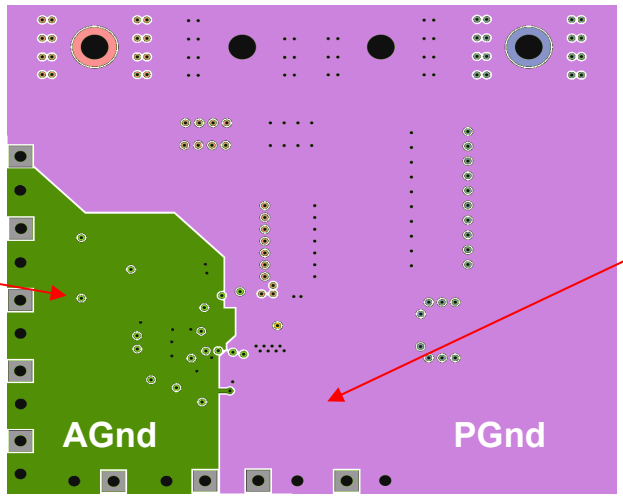
IRDC3898 Demo board layout considerations – Top Layer



Single point connection between AGND & PGND, should be close to the SupIRBuck, kept away from noise sources.

Feedback trace should be kept away form noise sources

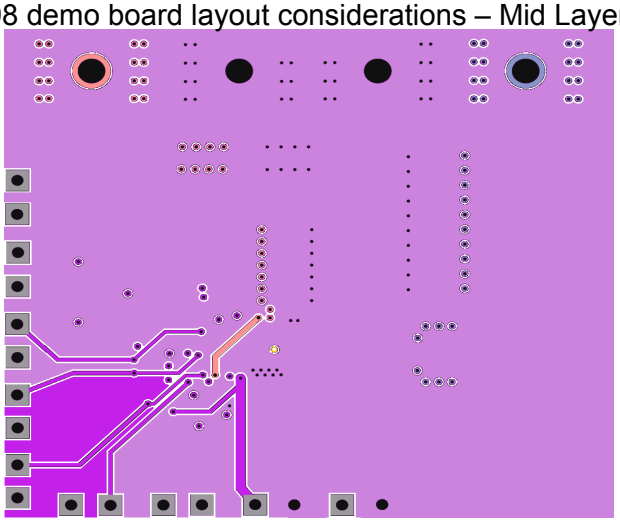
IRDC3898 demo board layout considerations – Bottom Layer



Analog Ground plane

Power Ground plane

IRDC3898 demo board layout considerations – Mid Layer 1



IRDC3898 demo board layout considerations – Mid Layer 2