P2110CSR

Powerharvester® Chipset Reference Design

DESCRIPTION

The Powercast P2110CSR Powerharvester® Chipset Reference Design (CSR) is an RF energy harvesting device that converts RF to DC. The P2110CSR receiver provides RF energy harvesting and power management for battery-free, micro-power devices. The P2110CSR converts RF energy to DC and stores it in a capacitor. When a charge threshold on the capacitor is achieved, the P2110CSR boosts the voltage to the set output voltage level and enables the voltage output. When the charge on the capacitor declines to the low voltage threshold the voltage output is turned off.

ORDERING INFORMATION

The P2110CSR can be evaluated on the P2110CSR-EVB evaluation board. Contact Powercast for information about obtaining a design license of the P2110CSR for integration onto your PCB. Additional CSR designs are available to support different frequencies and power ranges.

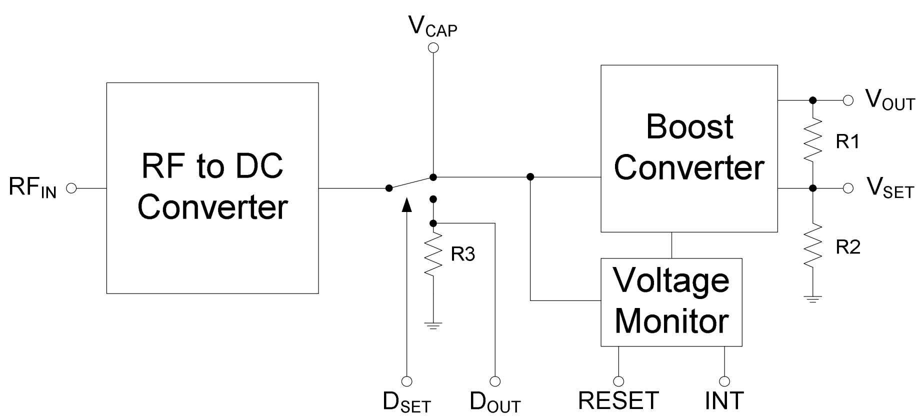
FEATURES

- High conversion efficiency
- Converts low-level RF signals enabling long range applications
- Regulated voltage output up to 5.5V
- Up to 50mA output current
- Received signal strength indicator
- Wide RF operating range
- Operation down to -11.5 dBm input power
- Externally resettable by microprocessor
- RoHS compliant

APPLICATIONS

- Battery-free wireless sensors
  - Industrial Monitoring
  - Smart Grid
  - Defense
  - Building automation
  - Oil & Gas
- Battery recharging
  -Coin cells
  -Thin-film cells
- Low power electronics

FUNCTIONAL BLOCK DIAGRAM



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6,289,237 | 6,615,074 | 6,856,291 | 7,027,311 | 7,057,514 | 7,639,994 | 7,643,312 | 7,812,771 | 7,844,306 | 7,868,482 | 7,898,105 | 7,925,308 | 8,159,090

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Parameter	Rating	Unit
RF Input Power	23	dBm
RF_{IN} to GND	0	V
D_{SET} to GND	6	V
RESET to GND	6	V
V_{CAP} to GND	2.3	V
V_{OUT} to GND	6	V
V_{OUT} Current	100	mA
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-40 to 140	°C

Exceeding the absolute maximum ratings may cause permanent damage to the device.

ESD CAUTION

This is an ESD (electrostatic discharge) sensitive device. Proper ESD precautions should be taken to avoid degradation or damage to the component.

INPUT/OUTPUT DESCRIPTION

PORT	Function
RF_{IN}	RF Input. Connect to 50Ω antenna through a 50Ω transmission line. Add a DC block if antenna is a DC short.
V_{OUT}	DC Output.
V_{SET}	Output Voltage Adjustment.
V_{CAP}	Connect to an external capacitor for energy storage.
INT	Digital Output. Indicates that voltage is present at V_{OUT}. Can be used to trigger output switch for battery recharging.
RESET	Digital Input. Set to disable V_{OUT}. If this function is not desired leave unconnected.
D_{SET}	Digital Input. Set to enable measurement of harvested power or capture of TX91501 data. If this function is not desired leave unconnected.
D_{OUT}	Analog/Digitial Output. Provides an analog voltage level corresponding to the harvested power. Provides a digital indication of the TX91501 data.

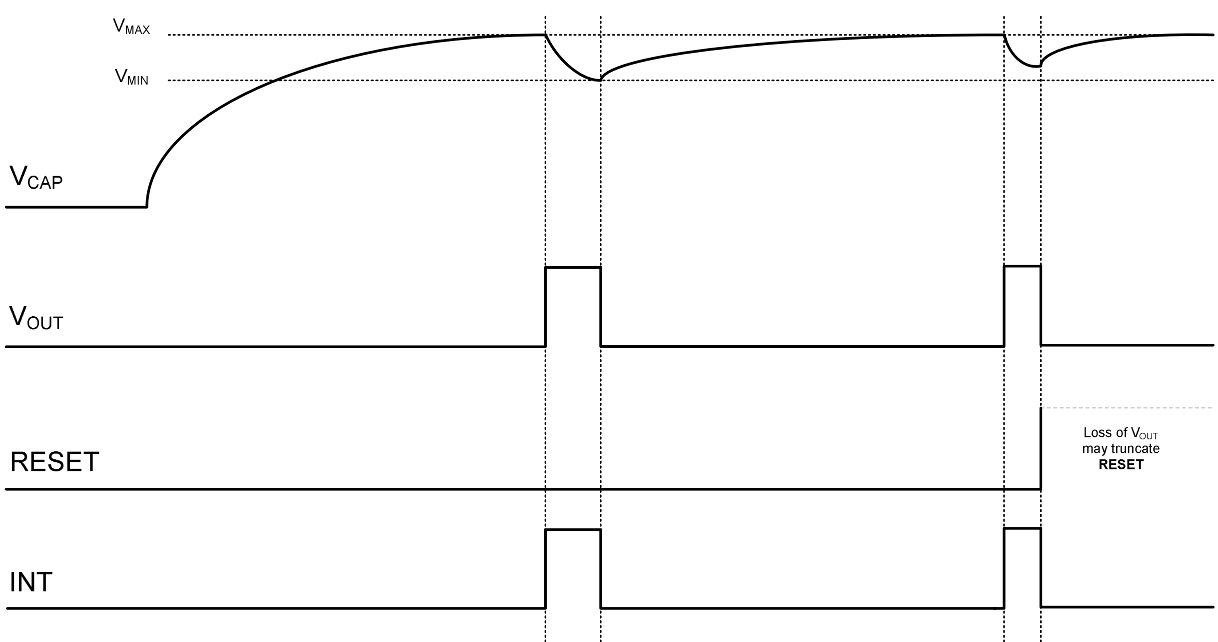
SPECIFICATIONS

T_A = 25°C, RF_{IN} = 915MHz unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
RF Characteristics[1]						
Input Power	RF_{IN}		-11.5		10	dBm
Frequency			902		928	MHz
DC Characteristics						
Output Voltage	V_{OUT}		2.0	3.3	5.5	V
Output Current	I_{OUT}				50	mA
V_{CAP} Maximum	V_{MAX}			1.25		V
V_{CAP} Minimum	V_{MIN}			1.02		V
Signal Strength	D_{OUT}	RF_{IN} = 0dBm		275		mV
Boost Efficiency		I_{OUT} = 20mA		85		%
Maximum INT Current				0.1		mA
Digital Characteristics						
RESET Input High				1		V
D_{SET} Input High			1.8			V
INT Output High			V_{MIN}		V_{MAX}	V
Timing Characteristics						
D_{SET} Delay				50		µs
RESET Delay				6.6		µs
RESET Pulse Width			20			ns

[1] See typical performance graphs for operation at other frequencies or power levels.

TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

RF INPUT (RF_{IN})

The RF input is an unbalanced input from the antenna. Any standard or custom 50Ω antenna may be used with the receiver. The P2110CSR has been optimized for operation in the 902-928MHz band but will operate outside this band with reduced efficiency. Contact Powercast for custom frequency requirements.

The RF input must be isolated from ground. For antennas that are a DC short, a high-Q DC blocking capacitor should be added in series with the antenna.

STORAGE CAPACITOR SELECTION (V_{CAP})

The P2110CSR requires an external storage capacitor connected at V_{CAP}. The value of the capacitor will determine the amount of energy available from the V_{OUT} pin. The capacitor should have a leakage current as small as possible. It is recommended that the leakage current of the capacitor be less than 1µA at 1.2V. The capacitor ESR should be 200mΩ or less.

Smaller capacitors will charge more quickly but will result in shorter operation cycles. Larger capacitors will charge more slowly, but will provide for longer operation cycles. The minimum required capacitor value can be estimated using the following equation.

$$C = 15\, V_{OUT} I_{OUT} t_{ON}$$

Where,
V_{OUT} - Output voltage
I_{OUT} - Average output current
t_{ON} - On-time of the output voltage

When using the RESET function, the size of the capacitor is less important. A larger capacitor can be used to facilitate intermittent functions that require more energy. The RESET will control the amount of energy removed from the capacitor during operation which will minimize the required recharge time. It should be noted that when RESET is used, a larger capacitor will not affect charge time during operation, but it will require more time to initially charge from a completely discharged state.

The voltage on the V_{CAP} pin under normal operation will vary between approximately 1.25V and 1.02V. If the harvested energy becomes too large, the voltage on the capacitor will be internally clamped to protect low voltage supercapacitors. Clamping will begin at approximately 1.8V and will limit the voltage to less than 2.3V at the maximum rated input power.

RSSI OPERATION (D_{OUT}, D_{SET})

The RSSI functionality allows the sampling of the received signal to provide an indication of the amount of energy being harvested. When D_{SET} is driven high the harvested DC power will be directed to the resistor R3, and the corresponding voltage will be provided to D_{OUT}. The voltage on D_{OUT} can be read after a 50µs settling time. When the RSSI functionality is being used, the harvested DC power is not being stored.

If the RSSI functionality is not used, D_{OUT} and D_{SET} should be left unconnected. D_{SET} is pulled down.

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RESET

The RESET function allows the voltage from V_{OUT} to be turned off before the storage capacitor reaches the lower threshold, V_{MIN}, thereby saving energy and improving the recharge time back to the activation threshold, V_{MAX}. The RESET function can be implemented by a microcontroller. When the function of the microcontroller is completed, driving RESET high will disable the voltage from V_{OUT}. Care should be taken to ensure that the microcontroller, especially during power-on, does not inadvertently drive RESET high. This will immediately shutdown the output voltage.

If the RESET functionality is not used, RESET should be left unconnected.

INTERRUPT (INT)

The interrupt function provides a digital indication that voltage is present at the V_{OUT} pin. INT can be used in more sophisticated systems that contain other storage elements and can be used as an external interrupt to bring a device such as microcontroller out of a deep sleep mode. The digital high level of the INT pin will be between V_{MIN} and V_{MAX}. The INT pin can provide a maximum of 0.1mA of current.

If the INT functionality is not used, INT should be left unconnected.

SETTING THE OUTPUT VOLTAGE (V_{OUT})

The DC output voltage from the P2110CSR can be adjusted to any voltage between 2.0V and 5.5V. V_{OUT} is set by resistors R1 and R2. The equation for determining R1 and R2 is as follows:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{1.108} - 1\right)}$$

It is recommended that a 1MΩ be used for R1, which is connected between V_{OUT} and V_{SET}. With this is mind, some common values for V_{OUT} would result in the following R2 values:

For V_{OUT} = 3.3V, R2 = 505.5kΩ (510kΩ std)
For V_{OUT} = 4.1V, R2 = 370.3kΩ (374kΩ std)
For V_{OUT} = 4.2V, R2 = 358.3kΩ (360kΩ std)

DATA RETRIEVAL (D_{OUT}, D_{SET})

Using D_{OUT} and D_{SET} it is possible to collect data from the RF transmitter that is supplying power to the P2110CSR. As discussed previously in the RSSI section, with D_{SET} high, D_{OUT} will provide a voltage across R3 that can be read by an ADC. However, the voltage on D_{OUT} will also follow the power level of the RF field as the power level changes. If the RF field is being provided by a transmitter that is also communicating by modulating its amplitude, such as the Powercast TX91501-3W-ID Powercaster® transmitter, the data can be read by the P2110CSR. The voltage level will need gained up using operation amplifiers and supplied to a device that can read the data pattern supplied by the transmitter.

LAYOUT CONSIDERATIONS

The RF_{IN} feed line should be designed as a 50Ω trace and should be as short as possible to minimize feed line losses. The following table provides recommended

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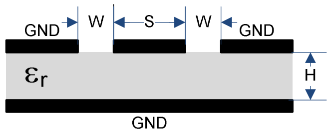
dimensions for 50Ω feed lines (CPWG) for different circuit board configurations.

PCB Side View



Material	Thickness (H)	Trace Width (S)	Spacing (W)
FR4 (ε_r = 4.2)	62	50	9
FR4 (ε_r = 4.2)	31	50	20

*All dimensions are in mils.

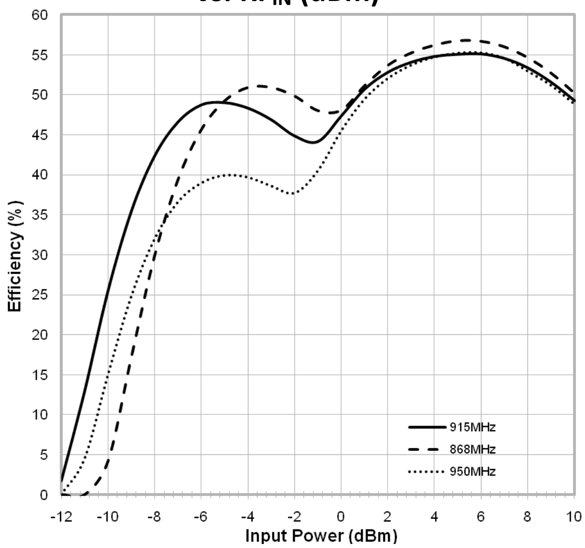
The CPWG GND on each side of the RF_{IN} pin should be connected to the bottom layer PCB ground plane through vias.

The D_{OUT} pin can contain low-level analog voltage signals. If a long trace is connected to this pin, additional filtering capacitance next to the A/D converter may be required. Additional capacitance on this pin will increase the D_{SET} delay time.

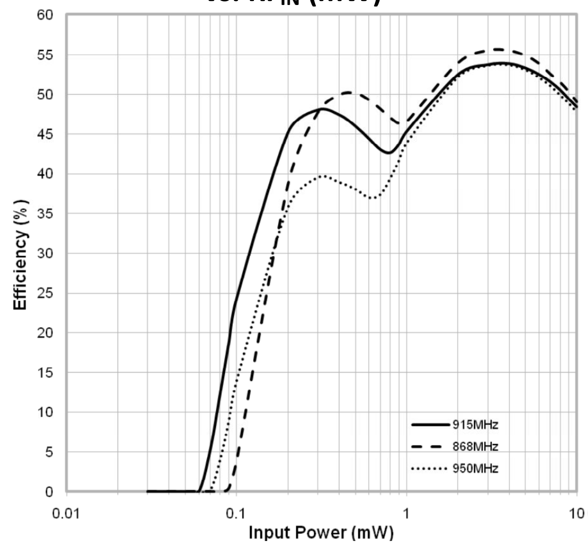
TYPICAL PERFORMANCE GRAPHS

T_A = 25°C, V_{OUT} = 3.3V, V_{CAP} = 1.2V, unless otherwise noted

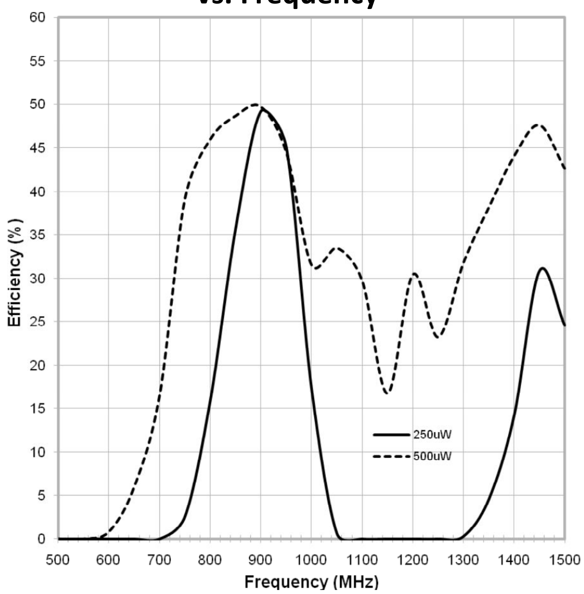
Powerharvester Efficiency vs. RF_{IN} (dBm)



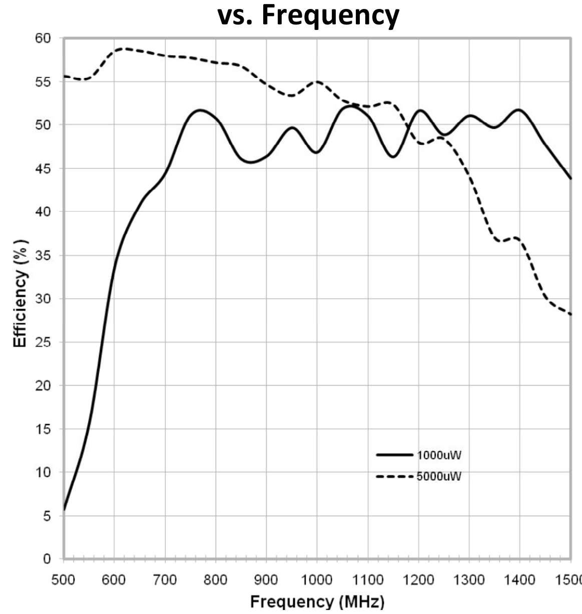
Powerharvester Efficiency vs. RF_{IN} (mW)



Powerharvester Efficiency vs. Frequency



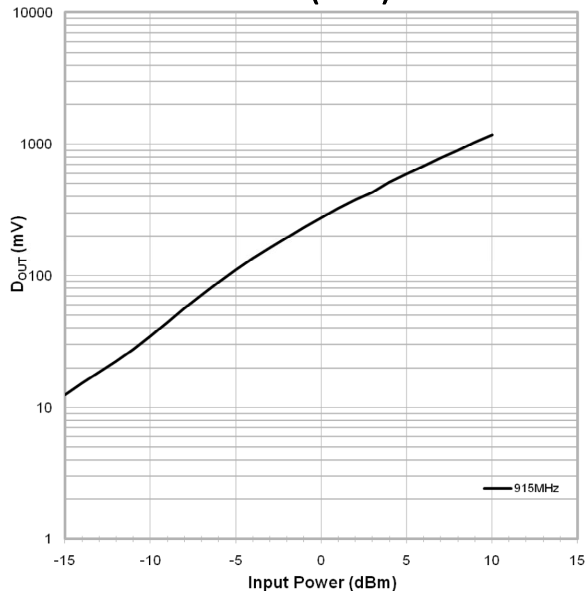
Powerharvester Efficiency vs. Frequency



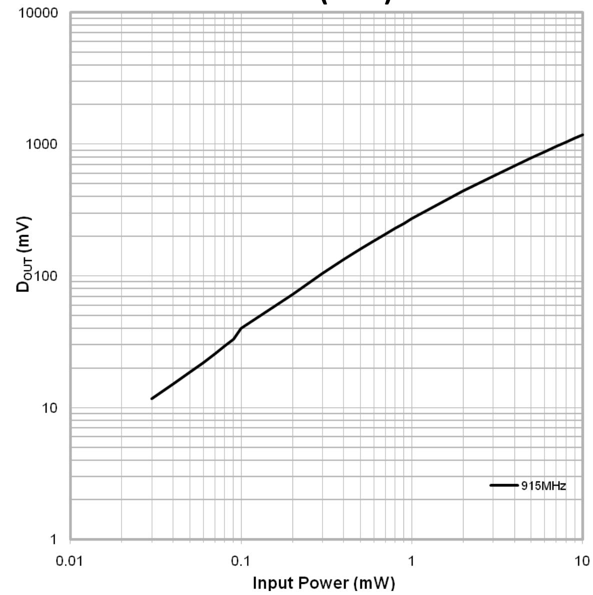
TYPICAL PERFORMANCE GRAPHS

T_A = 25°C, V_{OUT} = 3.3V, V_{CAP} = 1.2V, unless otherwise noted

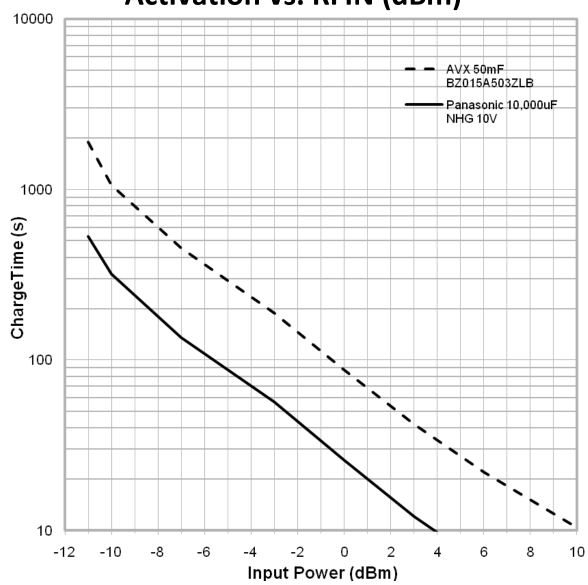
Received Signal Strength Indicator vs. RFIN (dBm)



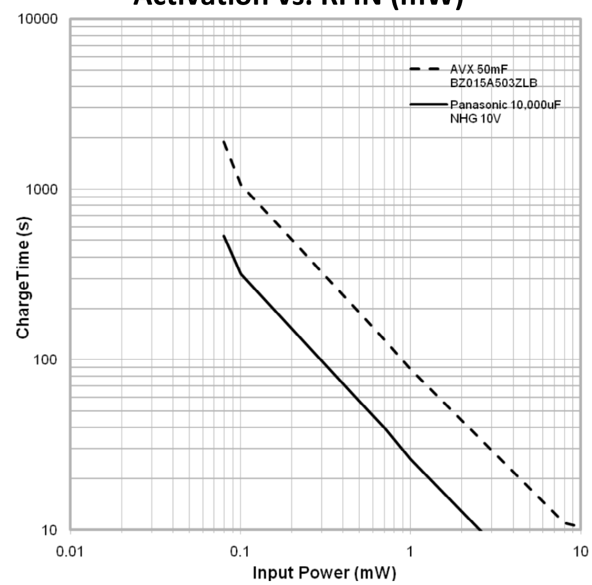
Received Signal Strength Indicator vs. RFIN (mW)



Initial CAP Charge Time to First Activation vs. RFIN (dBm)



Initial CAP Charge Time to First Activation vs. RFIN (mW)



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