User Guide for

FEBFSQ500L_H257v1

Evaluation Board

Compact, Green-Mode Controller FSQ500L
5.1V / 400mA Flyback Design

Featured Fairchild Product:

FSQ500L

Direct questions or comments about this evaluation board to: "Worldwide Direct Support"

Fairchild Semiconductor.com

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Table of Contents

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This user guide supports the evaluation kit for the FSQ500L. It should be used in conjunction with the FSQ500L datasheet as well as Fairchild's application notes and technical support team. Please visit Fairchild's website at www.fairchildsemi.com.

1. Introduction

This engineering report describes a 2.04W power supply using a FSQ500L. This power supply is targeted for a flyback converter replaces linear power supplies with low cost and small size.

1.1. General Description

This device combines a current-mode Pulse Width Modulator (PWM) with a SenseFET and high-voltage regulator connected from the DRAIN pin to supply the V_{CC}. This device does not need to use bias winding and associated external components.

Using a SOT-223 package, FSQ500L reduces total size and weight while increasing efficiency, productivity, and system reliability. Using FSQ500L, this design example for 2.04W can be implemented with few external components and minimized cost.

1.2. Features

- Single-Chip 700V SenseFET Power Switch
- Precision Fixed Operating Frequency: 130kHz
- No-load consumption 250mW at 265V_{AC} with Burst Mode and Down to 60mW with External Bias
- Internal Startup Switch
- Soft-Start Time Tuned by External Capacitor
- Under-Voltage Lockout (UVLO) with Hysteresis
- Pulse-by-Pulse Current Limit
- Overload Protection (OLP) and Internal Thermal Shutdown Function (TSD) with Hysteresis
- Auto-Restart Mode
- No Need for Auxiliary Bias Winding

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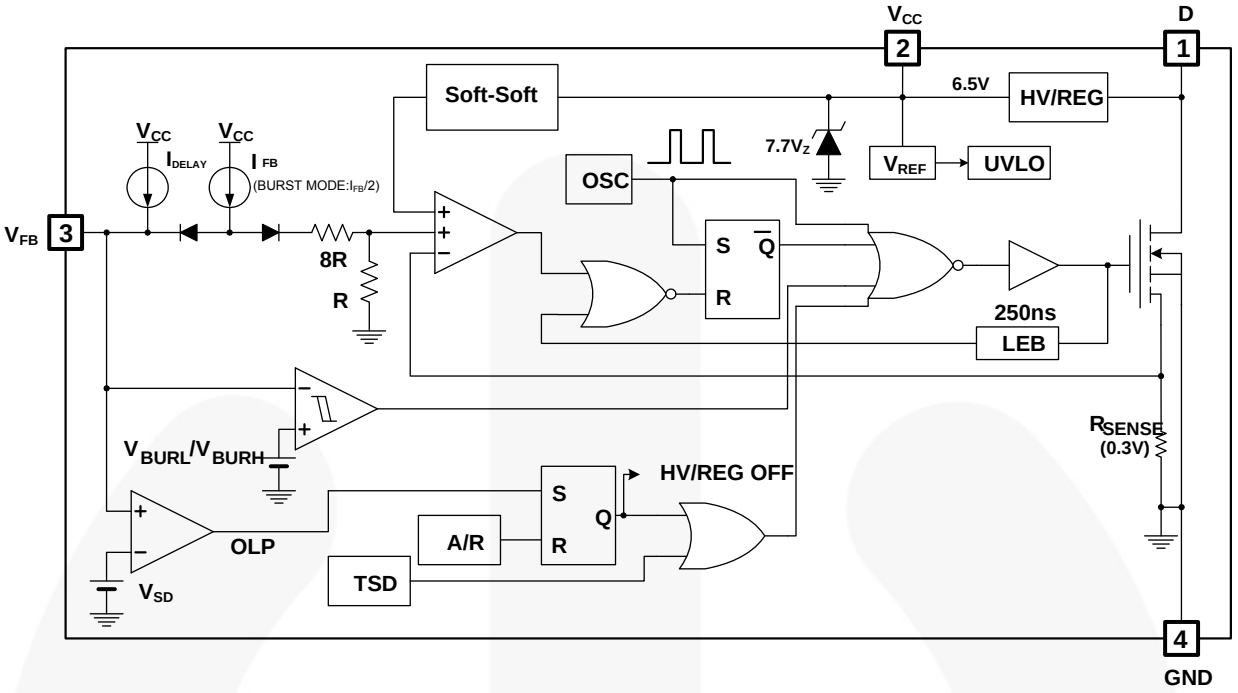

Figure 1. Internal Block Diagram

2. Specifications

Table 1. Summary of Features and Performance

Description	Min.	Max.	Unit
Input			
Voltage	90	264	V_{AC}
Frequency	47	63	Hz
Output			
Output Voltage 1		5.1	V
Output Current 1	0	0.4	A
Total Output Power			
Full-load Output Power	0	2.04	W
Peak Output Power			W

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3. Photographs & PCB Layout

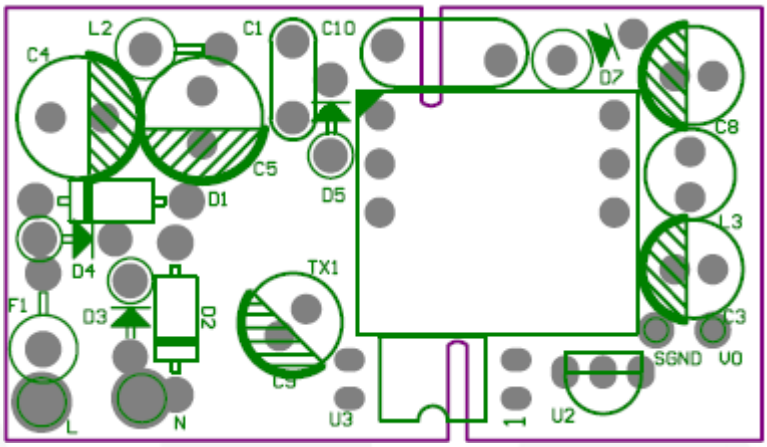

Figure 2. Top Overlay Silk Screen

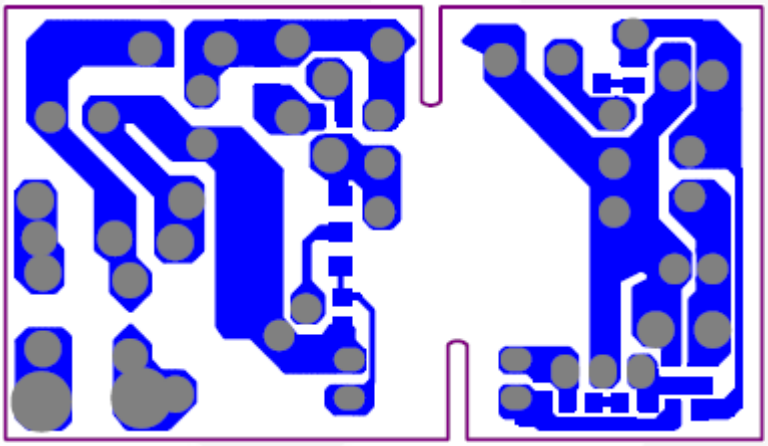

Figure 3. Bottom Layer Pattern

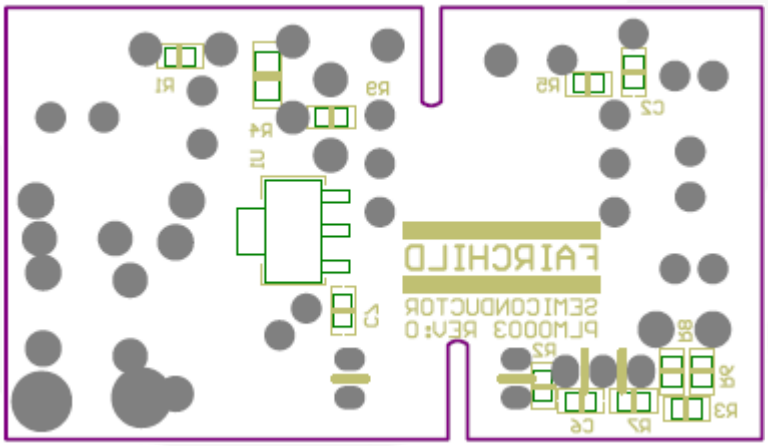

Figure 4. Bottom Overlay Silk Screen

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4. Function Test Report

Test Model	FEBFSQ500L_H257v1
Test Date	June.23, 2008
Test Temperature	Ambient
Test Equipment	AC source: 6800 AC POWER SOURCE Electronic load: Chroma 63030 Power meter: WT210 Oscilloscope: LeCory 24Xs
Test Items	1 Input Current 2 Input Wattage at No-Load Condition 3 Burst Mode Test 4 Soft-Start Test 5 Turn-On Delay Test 6 DC Output Rising Time 7 Line and Load Regulation 8 Efficiency 9 Output Ripple and Noise 10 Step Load Response 11 Over-Current Protection 12 Hold-Up Time 13 Short Circuit Protection 14 Maximum Duty Ratio 15 Power Off 16 Over-Temperature Protection (OTP) 17 Voltage Stress of Drain and Secondary Rectifier 18 EMI Waveforms 19 Surge Test 20 ESD Test

4.1. Input Current

4.1.1. Test Condition

Measure the AC input current at maximum loading.

Table 2. Test Result

Input Voltage	Input Current
85V_{AC} / 60Hz	57.62mA
264V_{AC} / 50Hz	35.73mA

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4.2. Input Wattage at No-Load Condition

4.2.1. Test Condition

Measure the input wattage and output voltage at no load.

Table 3. Test Result

Input Voltage	Input Wattage	Output Voltage	Specification
85V_{AC} / 60Hz	0.094W	5.224V	< 0.25W
120V_{AC} / 60Hz	0.116W	5.224V	
230V_{AC} / 50Hz	0.209W	5.224V	
264V_{AC} / 50Hz	0.242W	5.224V	

4.3. Burst Mode Test

4.3.1. Test Condition

Measure the waveform and frequency in Burst Mode at no load.

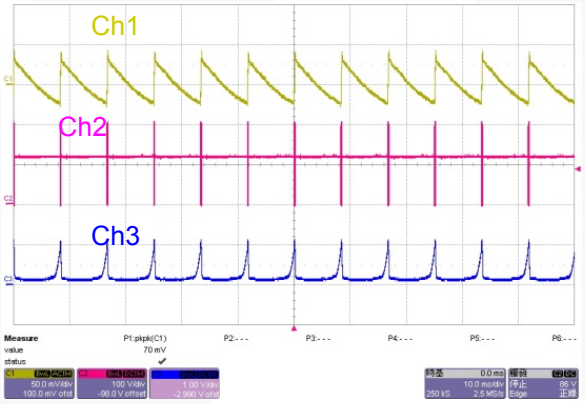

Figure 5. 85V_{AC} / 60Hz at No Load (Ch 1: Vo, Ch 2: V_{DS}, Ch 3: V_{FB})

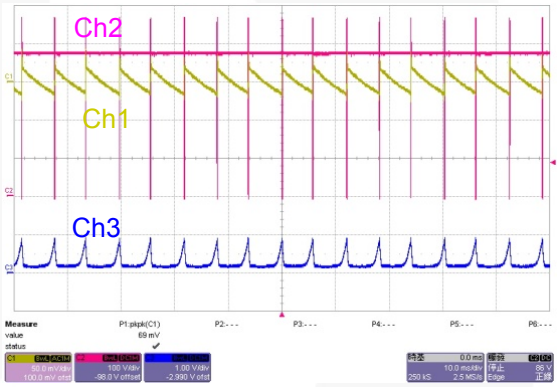

Figure 6. 264V_{AC} / 50Hz at No Load (Ch 1: Vo, Ch 2: V_{DS}, Ch 3: V_{FB})

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4.4. Soft-Start Test

4.4.1. Test Condition

Measure the soft-start waveform at maximum load with ambient, after short, after OTP.

Table 4. Test Result

Input Voltage	Soft-Start Time
120V_{AC} / 60Hz	14ms Under
240V_{AC} / 50Hz	14ms Under

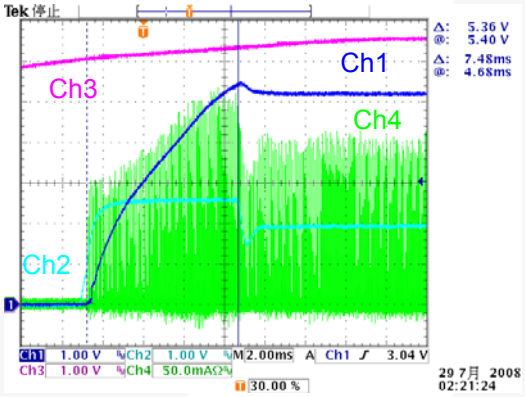

Figure 7. 120V_{AC} / 60Hz at Max. Load, Ambient (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

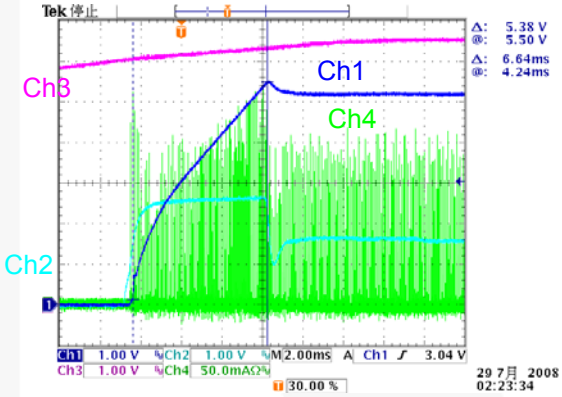

Figure 8. 240V_{AC} / 50Hz at Max. Load, Ambient (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

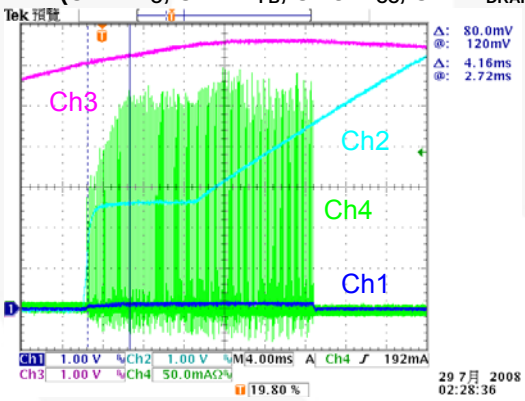

Figure 9. 120V_{AC} / 60Hz at Max. Load, After Short (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

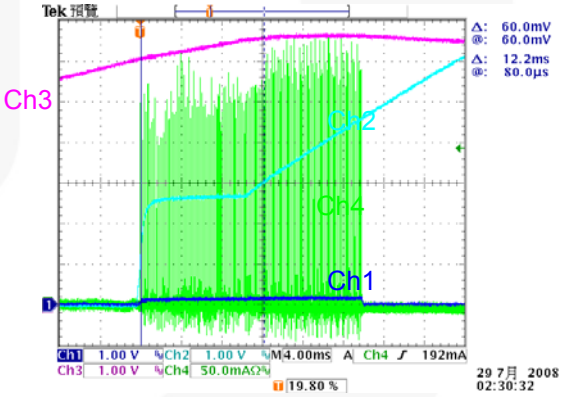

Figure 10. 240V_{AC} / 50Hz at Max. Load, After Short (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

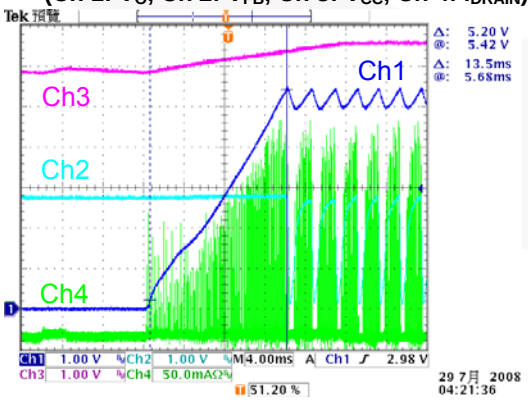

Figure 11. 120V_{AC} / 60Hz at Max. Load, After OTP (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

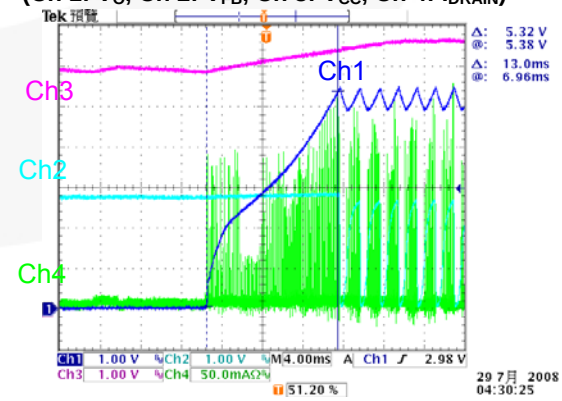

Figure 12. 240V_{AC} / 50Hz at Max. Load, After OTP (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

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4.5. Turn-On Delay Test

4.5.1. Test Condition

Set the output at maximum loading. Measure the interval between AC plug-in and stable output.

Table 5. Test Result

Input Voltage	Maximum Load
85V_{AC} / 60Hz	89.60ms
264V_{AC} / 50Hz	99.08ms

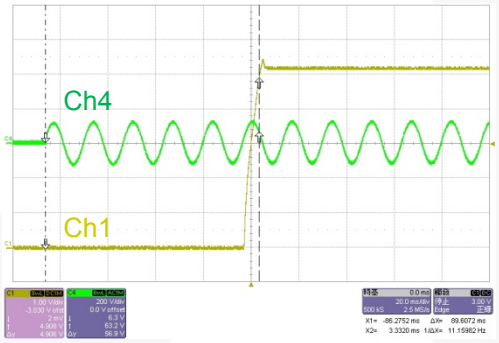

Figure 13. 85V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 4: V_{AC})

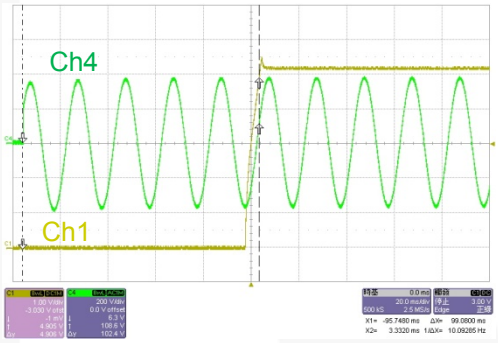

Figure 14. 264V_{AC} / 50Hz at Max. Load (Ch 1: V_O, Ch 4: V_{AC})

4.6. DC Output Rising Time

4.6.1. Test Condition

Set output at maximum loading and no loading. Measure the time interval between 10% and 90% of output voltage during startup.

Table 6. Test Result

Input Voltage	Maximum Load	No Load	Specification
85V_{AC} / 60Hz	5.26ms	4.04ms	< 20ms
264V_{AC} / 50Hz	5.05ms	3.63ms	

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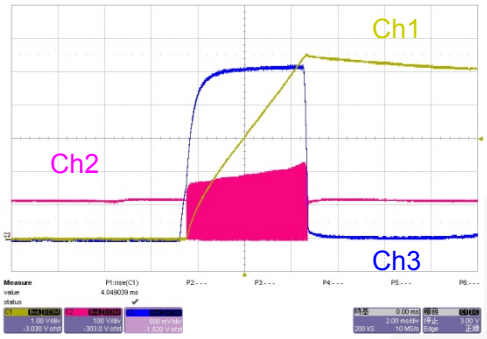

Figure 15. 85V_{AC} / 60Hz at No Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

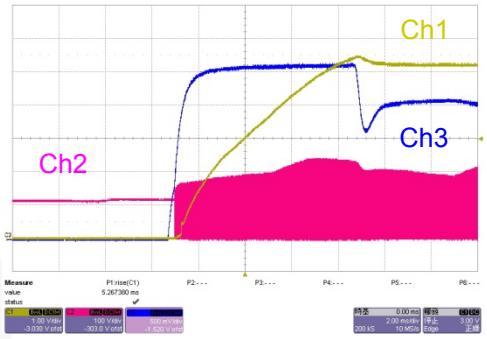

Figure 16. 85V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

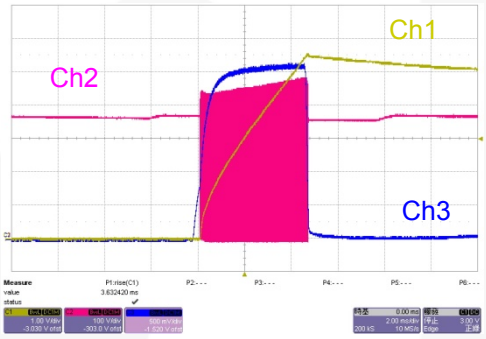

Figure 17. 264V_{AC} / 50Hz at No Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

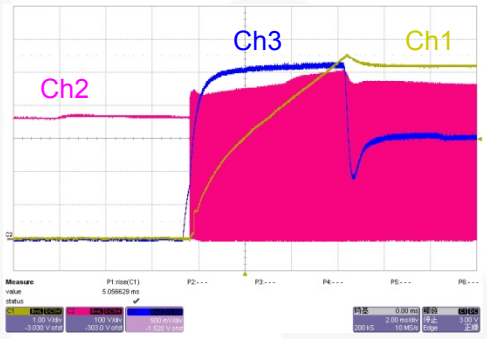

Figure 18. 264V_{AC} / 50Hz at Max. Load (Ch 1: V_O, Ch 2: V_{DS}, Ch 3: V_{FB})

4.7. Line and Load Regulation

4.7.1. Test Condition

Measure line and load regulation according to Table 7 (with output cable).

Table 7. Test Result

Input Voltage	Output Voltage at Max. Load	Output Voltage at Min. Load	Load Regulation
85V_{AC} / 60Hz	5.224V	5.224V	0%
115V_{AC} / 60Hz	5.224V	5.224V	0%
132V_{AC} / 60Hz	5.224V	5.224V	0%
180V_{AC} / 50Hz	5.224V	5.224V	0%
230V_{AC} / 50Hz	5.224V	5.224V	0%
264V_{AC} / 50Hz	5.224V	5.224V	0%
Line Regulation	0%	0%	

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4.8. Efficiency

4.8.1. Test Condition

Output at maximum load.

Table 8. Test Result

Input Voltage	Input Wattage	Output Wattage	Efficiency
85V_{AC} / 60Hz	3.17W	2.09W	65.93%
120V_{AC} / 60Hz	3.15W	2.09W	66.34%
230V_{AC} / 50Hz	3.691W	2.09W	56.62%
264V_{AC} / 50Hz	3.933W	2.09W	53.14%

Table 9. Test Result

	Efficiency				
Input Voltage	**25% Load**	**50% Load**	**75% Load**	**100% Load**	**Average**
115V_{AC} / 60Hz	55.31%	58.88%	64.43%	66.22%	61.21%
230V_{AC} / 50Hz	43.01%	46.97%	50.96%	56.62%	49.41%

4.9. Output Ripple and Noise

4.9.1. Test Condition

Ripple and noise are measured by using a 20MHz-bandwidth limited oscilloscope with a 10µF capacitor paralleled with a high-frequency 0.1µF capacitor across each output.

Table 10. Test Result

Input Voltage	Maximum Load	Minimum Load
85V_{AC} / 60Hz	16mV	69mV
120V_{AC} / 60Hz	19mV	69mV
240V_{AC} / 50Hz	16mV	53mV
264V_{AC} / 50Hz	16mV	50mV

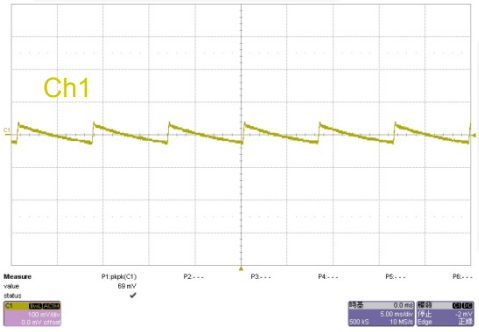

Figure 19. 85V_{AC} / 60Hz at No Load (Ch 1: V_O)

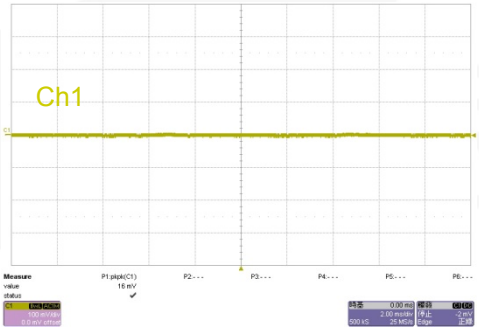

Figure 20. 85V_{AC} / 60Hz at Max. Load (Ch 1: V_O)

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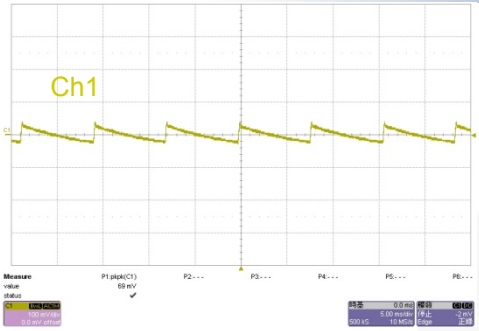

Figure 21. 120V_{AC} / 60Hz at No Load (Ch 1: V_O)

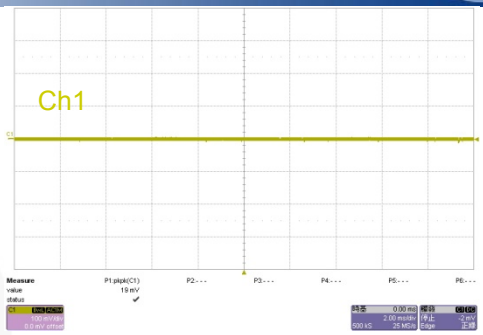

Figure 22. 120V_{AC} / 60Hz at Max. Load (Ch 1: V_O)

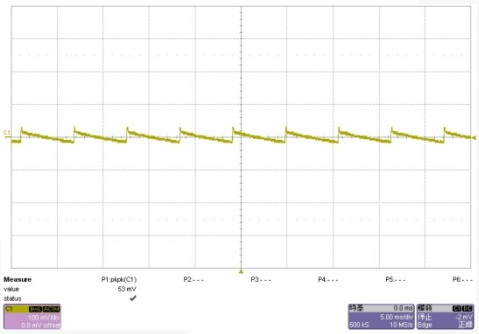

Figure 23. 240V_{AC} / 50Hz at No Load (Ch 1: V_O)

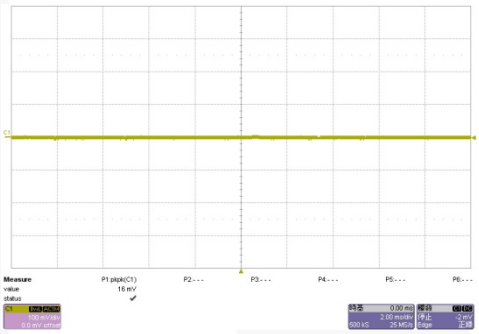

Figure 24. 240V_{AC} / 50Hz at Max. Load (Ch 1: V_O)

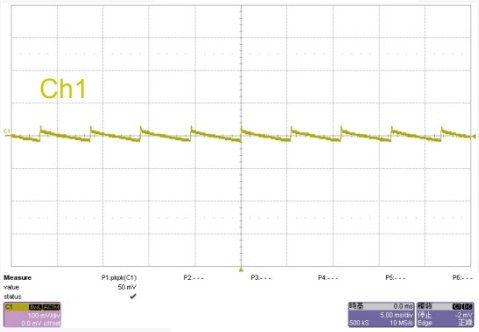

Figure 25. 264V_{AC} / 50Hz at No Load (Ch 1: V_O)

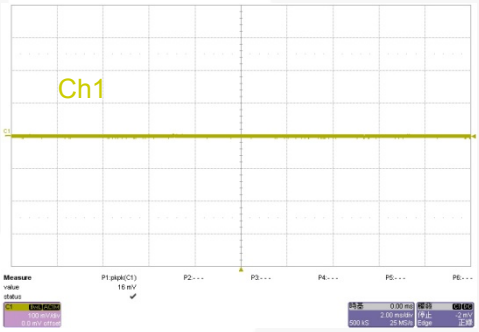

Figure 26. 264V_{AC} / 50Hz at Max. Load (Ch 1: V_O)

4.10. Step Load Response

4.10.1. Test Condition

Dynamic loading (20%~80% of the full load, 5ms duty cycle, 2.5A/µs rise/fall time).

Table 11. Test Result (20%~80% of the Full Load)

Input Voltage	Overshoot	Undershoot
85V_{AC} / 60Hz	70mV	53mV
264V_{AC} / 50Hz	61mV	119mV

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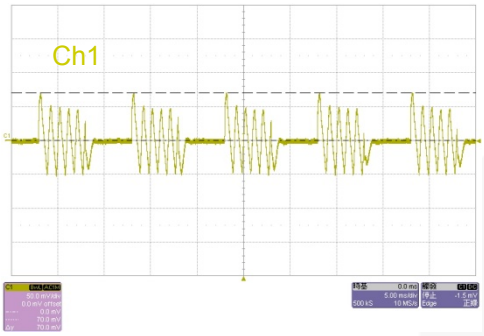

Figure 27. 85V_{AC} / 60Hz (Ch 1: V_O)

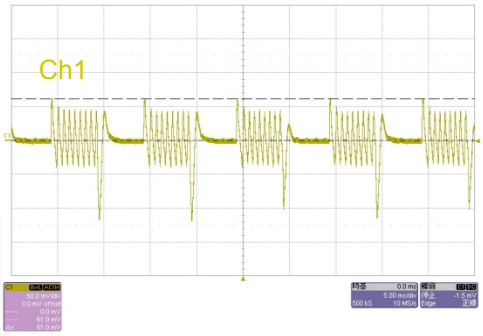

Figure 28. 264V_{AC} / 50Hz (Ch 1: V_O)

4.11. Over-Current Protection

4.11.1. Test Condition

Increase output loading gradually and measure the maximum output power.

Table 12. Test Result

Input Voltage	Output Current
85V_{AC} / 60Hz	0.611A
120V_{AC} / 60Hz	0.650A
240V_{AC} / 50Hz	0.836A
264V_{AC} / 50Hz	0.881A

4.12. Hold-up Time

4.12.1. Test Condition

Set output at maximum load. Measure the time interval between AC off and output voltage falling to the lower limit of the rated value. The AC waveform should be off at zero phase.

Table 13. Test Result

Input Voltage	Hold-up Time
85V_{AC} / 60Hz	8.49ms
115V_{AC} / 60Hz	18.64ms
230V_{AC} / 50Hz	77.27ms
264V_{AC} / 50Hz	101.41ms

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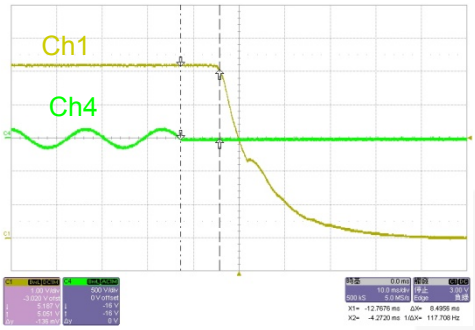

Figure 29. 85V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 4:V_{AC})

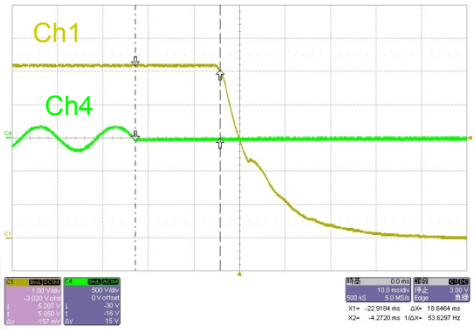

Figure 30. 115V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 4:V_{AC})

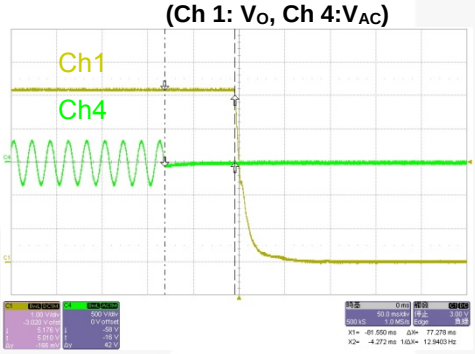

Figure 31. 230V_{AC} / 50Hz at No Load (Ch 1: V_O, Ch 4:V_{AC})

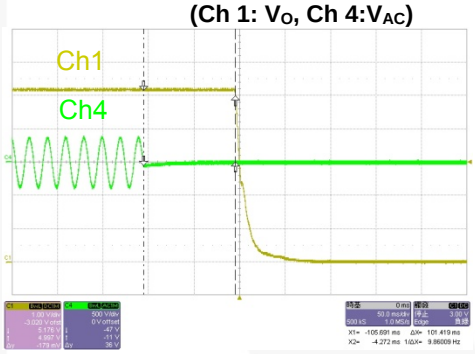

Figure 32. 264V_{AC} / 50Hz at Max. Load (Ch 1: V_O, Ch 4:V_{AC})

4.13. Short Circuit Protection

4.13.1. Test Condition

Short the output of the power supply. The power supply should enter "Auto Restart Mode" protection with less than 2W input voltage.

Table 14. Test Result

Input Voltage	Input Wattage at Maximum Load	Input Wattage at Minimum Load	Specification
120V_{AC} / 60Hz	0.574W	0.572W	Pin < 2W
240V_{AC} / 50Hz	0.82W	0.824W	

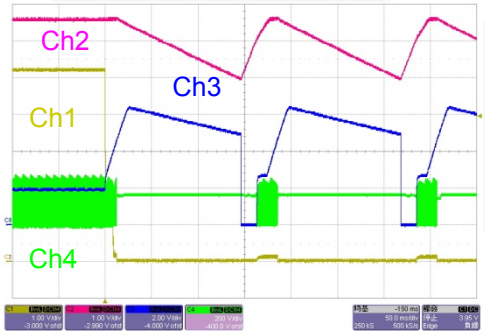

Figure 33. 120V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

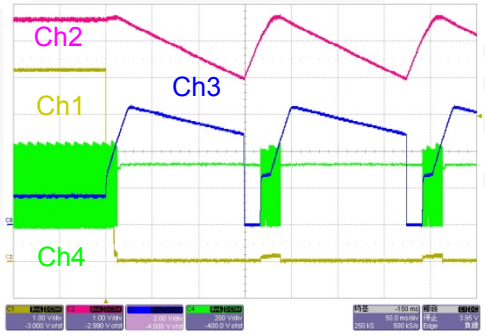

Figure 34. 240V_{AC} / 50Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

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4.14. Maximum Duty Ratio

4.14.1. Test Condition

Set the output at maximum loading. Decrease the input voltage with 5VAC step. Verify the FB voltage is under overload state (between 2.7~4V). Measure the maximum duty and waveform.

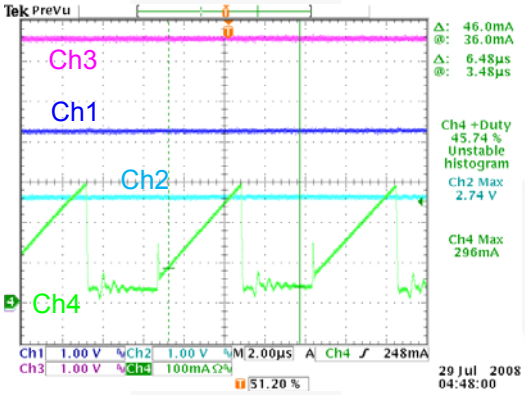

Figure 35. 50V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 2: V_{FB}, Ch 3: V_{CC}, Ch 4: I_{DRAIN})

4.15. Power Off

4.15.1. Test Condition

Set the output at the maximum load. Remove power.

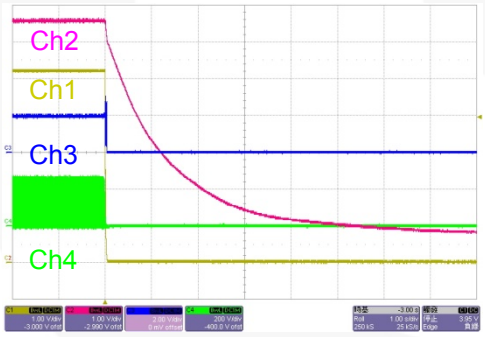

Figure 36. 120V_{AC} / 60Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

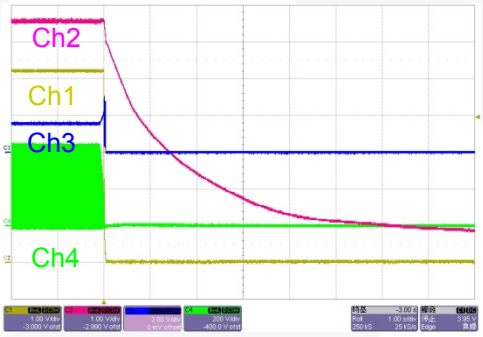

Figure 37. 240V_{AC} / 50Hz at Max. Load (Ch 1: V_O, Ch 2: V_{CC}, Ch 3: V_{FB}, Ch 4:V_{DS})

4.16. Over-Temperature Protection (OTP)

4.16.1. Test Condition

Set the output at maximum loading. Heat the IC with a heatgun, measure the waveform to enable the OTP, and disable the OTP.

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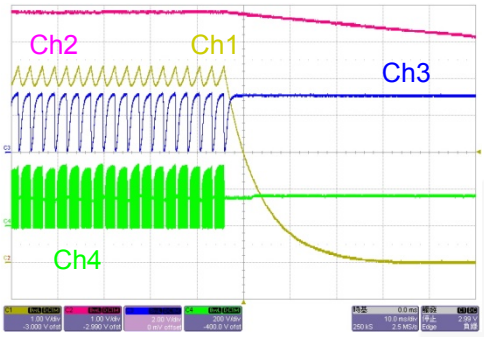

Figure 38. 120V_{AC} / 60Hz at Max. Load, Enable (Ch 1: V_O, Ch 2: V_{CC}. Ch 3: V_{FB}, Ch 4: V_{DS})

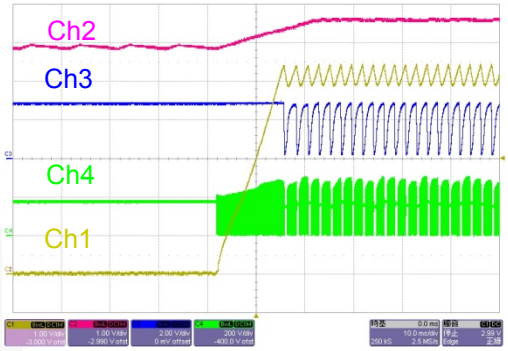

Figure 39. 120V_{AC} / 60Hz at Max. Load, Disable (Ch 1: V_O, Ch 2: V_{CC}. Ch 3: V_{FB}, Ch 4: V_{DS})

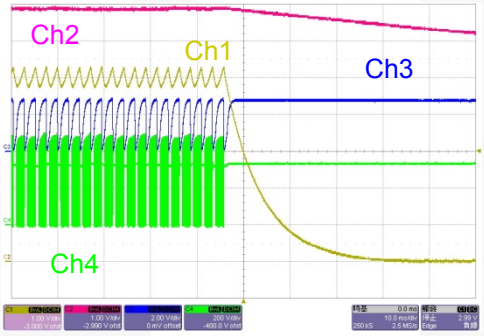

Figure 40. 240V_{AC} / 50Hz at Max. Load, Enable (Ch 1: V_O, Ch 2: V_{FB}. Ch 3: V_{CC}, Ch 4:V_{DS})

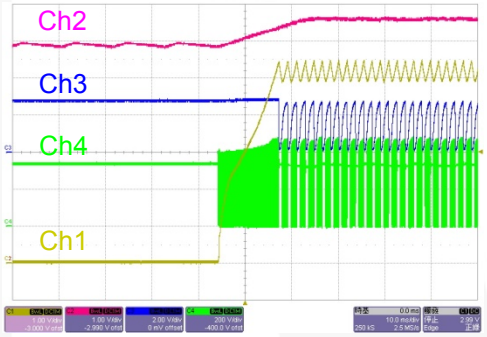

Figure 41. 240V_{AC} / 50Hz at Max.Load, Disable (Ch 1: V_O, Ch 2: V_{FB}. Ch 3: V_{CC}, Ch 4:V_{DS})

4.17. Voltage Stress of Drain and Secondary Rectifier

4.17.1. Test Condition

Measure the voltage stress of drain and secondary rectifiers under conditions specified in the table below.

4.17.2. Test Result

	Stress On MOSFET	Rating	Stress On Output Rectifier	Rating
85V_{AC} / 60Hz, Maximum Load	231V	600V	19.4V	60V
85V_{AC} / 60Hz, Maximum Load, Startup	234V		18.8V	
85V_{AC} / 60Hz, Maximum Load, Output Short	212V		13.8V	
264V_{AC} / 50Hz, Maximum Load	500V		41.3V	
264V_{AC} / 50Hz, Maximum Load, Startup	496V		41.3V	
264V_{AC} / 50Hz, Maximum Load, Output Short	471V		35.6V	
264V_{AC} / 50Hz, Maximum Load, Turns Off	494V		41.3V	

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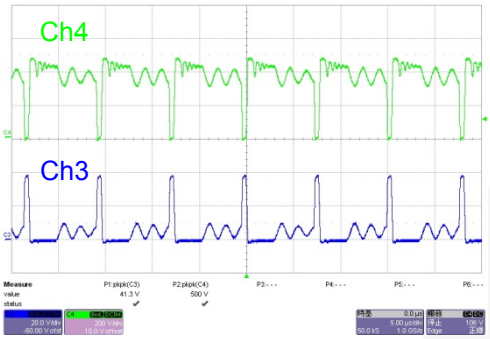

Figure 42. 264V$_{AC}$ / 50Hz at Max. Load, Operating (Ch 3: V$_{ak_rectifier}$, Ch 4:V$_{DS_MOS}$)

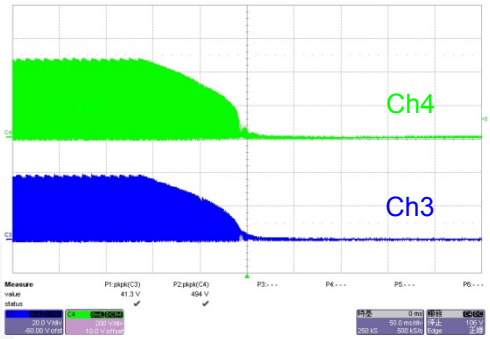

Figure 43. 264V$_{AC}$ / 50Hz at Max. Load, Power Off (Ch 3: V$_{ak_rectifier}$, Ch 4:V$_{DS_MOS}$)

4.18. EMI Waveforms

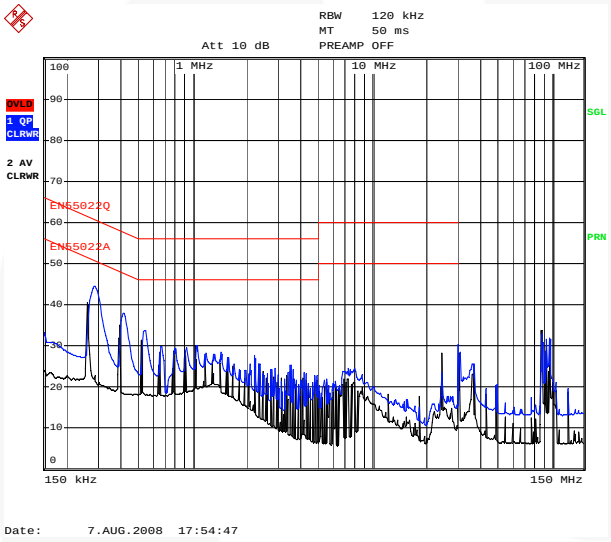

Figure 44. Conduction-Line at 115V$_{AC}$

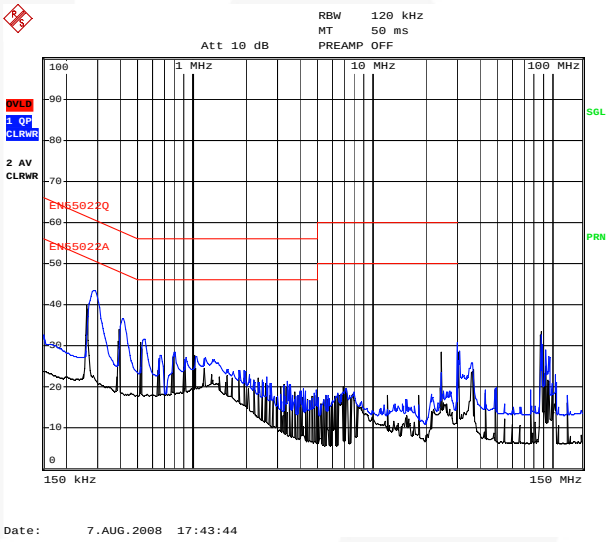

Figure 45. Conduction-Neutral at 115V$_{AC}$

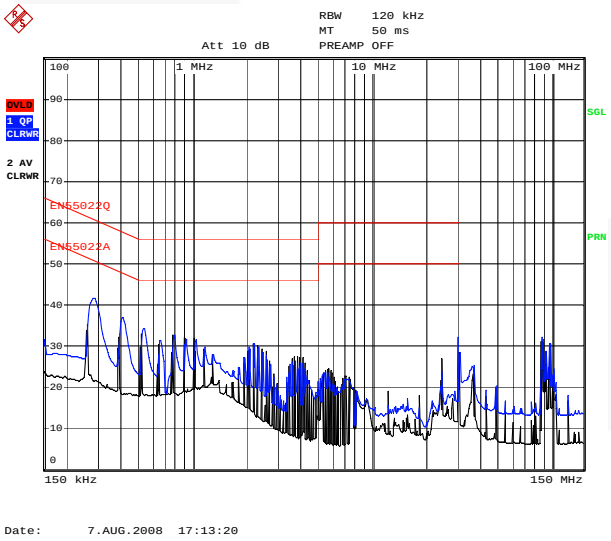

Figure 46. Conduction-Line at 230V$_{AC}$

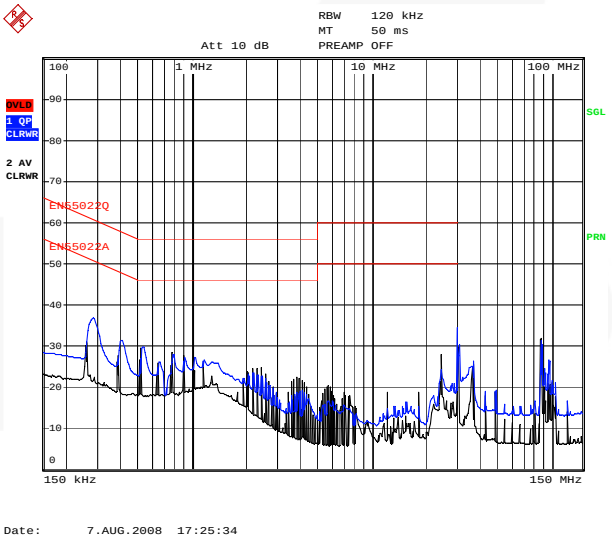

Figure 47. Conduction-Neutral at 230V$_{AC}$

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4.19. Surge Test

Mode	Polarity	Phase	Voltage	Condition
L-PE	±	0°	4.4KV	Pass
	±	90°		Pass
	±	180°		Pass
	±	270°		Pass
N-PE	±	0°	4.4KV	Pass
	±	90°		Pass
	±	180°		Pass
	±	270°		Pass

4.20. ESD Test

Air Discharge (16.5KV)		Contact Discharge (8.8KV)	
Pass	Pass	Pass	Pass

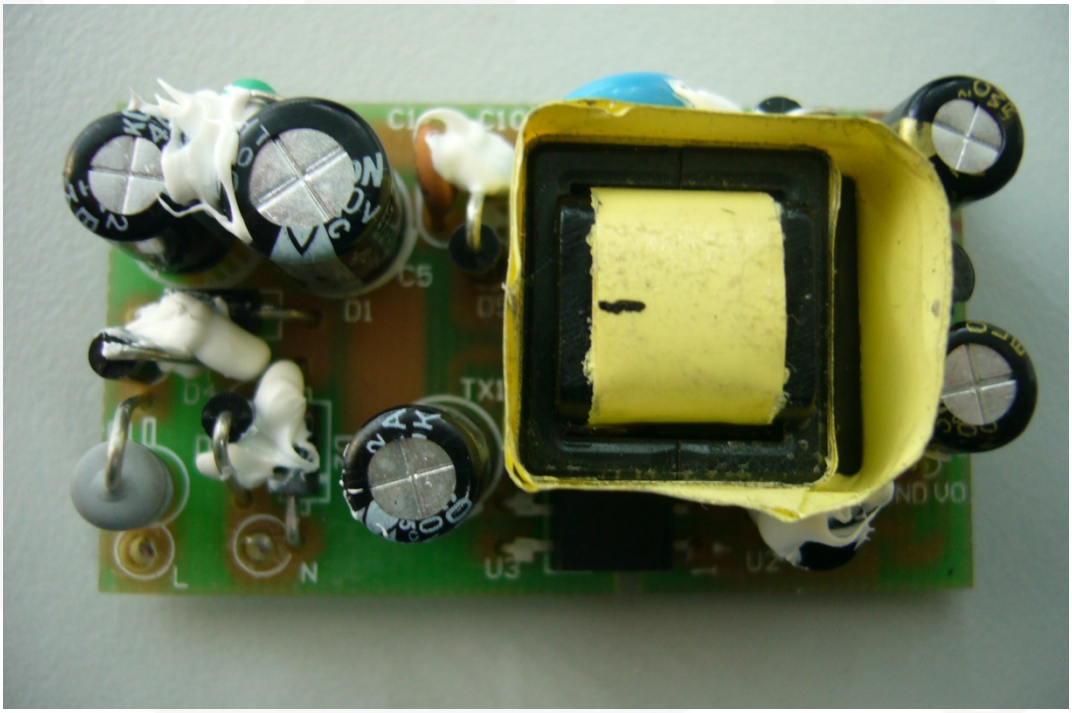

Figure 48. ESD Test Setup

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5. Schematic

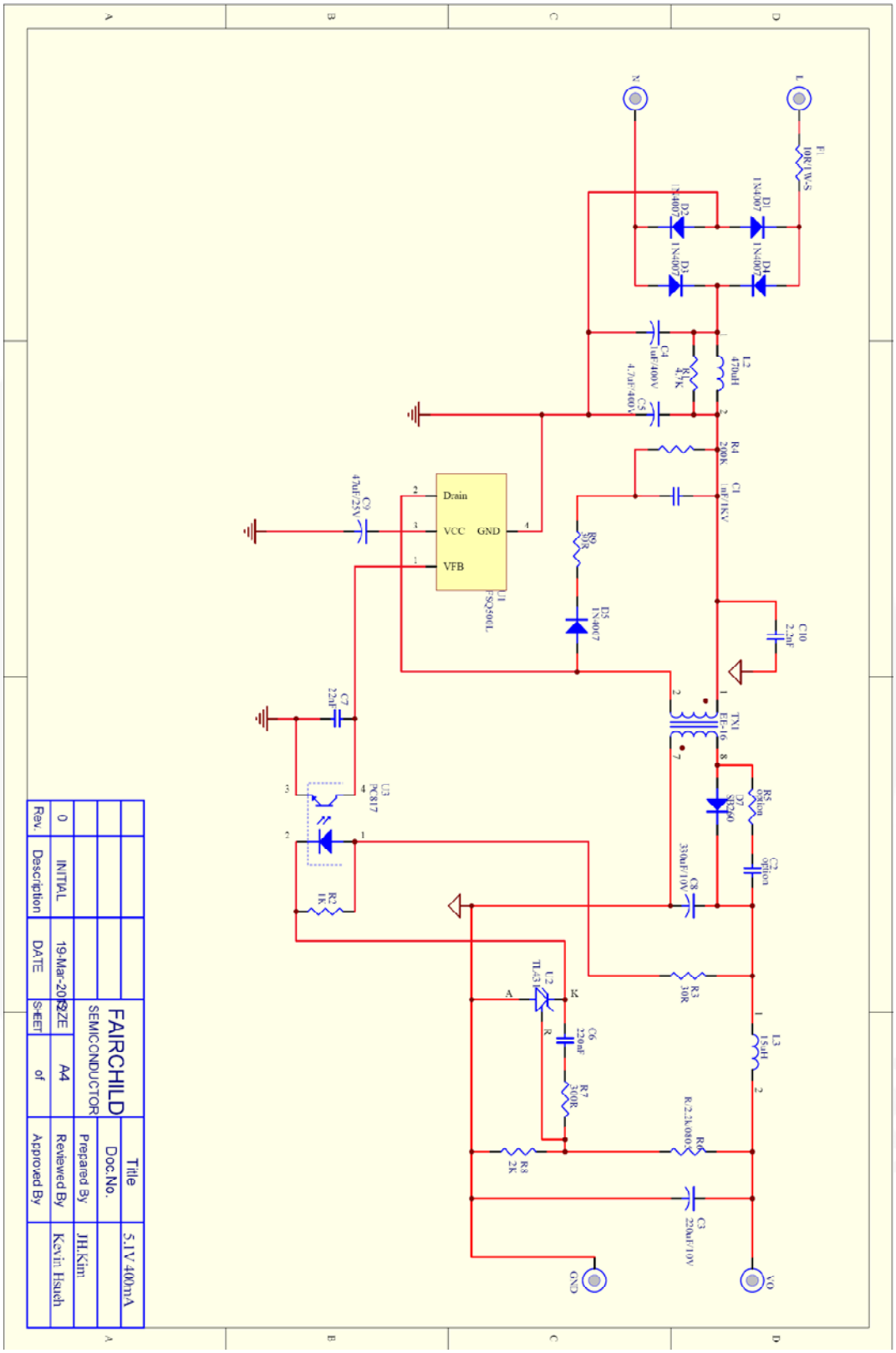

Figure 49. Schematic

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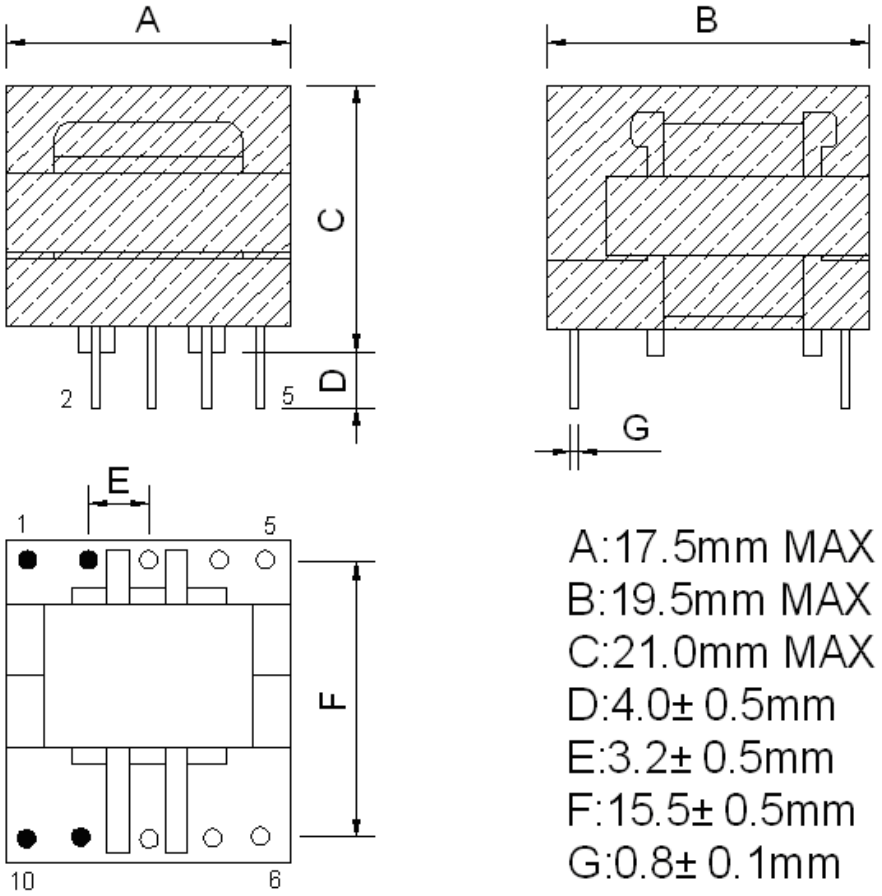
6. Transformer Specification

Customer				P/N:	TRN-0246
DATE	08/12/2008	Version	A	Page	1/3

1.Dimension:



A:17.5mm MAX
B:19.5mm MAX
C:21.0mm MAX
D:4.0± 0.5mm
E:3.2± 0.5mm
F:15.5± 0.5mm
G:0.8± 0.1mm

Note:
1 .Pin3.4.5.6.7.8.removed

UNIT	m/m	DRAWN	CHECK	TITLE	TRANS
TEL	(02)2215-8302	Ci wun Chen	Guo long Huang	IDENT N O.	TRN-0246
FAX	(02)2215-8293	SEN HUEI INDUSTRIAL CO.,LTD.		D W G N O.	

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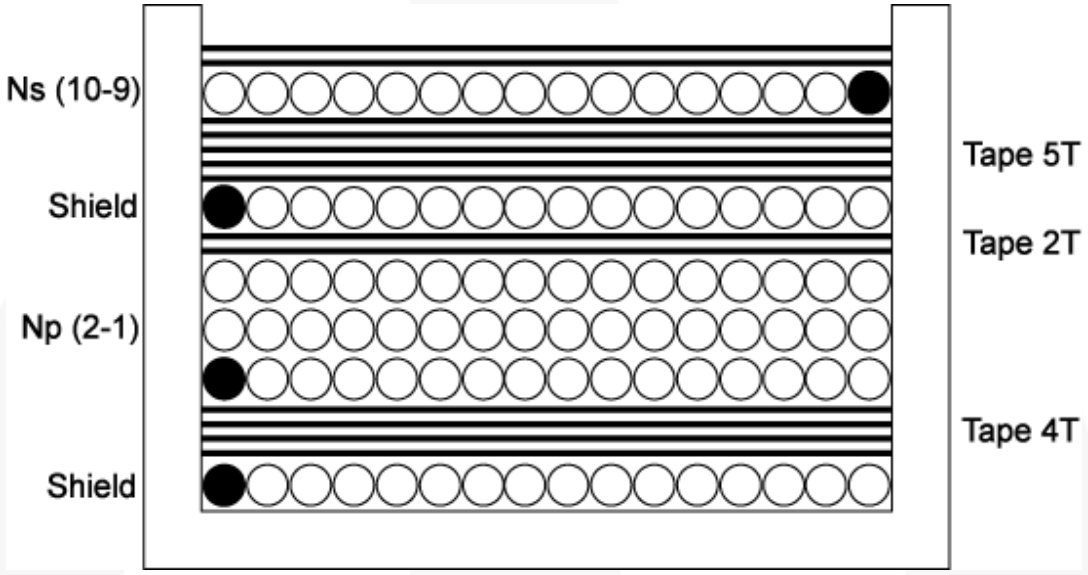
DATE	08/12/2008	Version	A	Page	2/3

2.Schematic:



NO	TERMINAL		WIRE	T_S	INSULATION	BARRIER	
	S	F			T_S		S
w1	1	x	0.15*1	46	4		
w2	2	1	0.2*1	104	2		
w3	1	x	0.15*1	46	5		
w4	10	9	TEX-E 0.4*1	9	2		
			CORE ROUNDING TAPE		3		

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3.Electrial Specification:

3.1 Inductance test： at 100KHz ,1V

P(2-1)： 800μH ±5%

3.2 DC Resistance test at 25°C

P(2-1)：xx Ω Max. (not fixed)

P(10-9)：xx Ω Max. (not fixed)

3.3 Hi-pot test：

AC 3.0K V /60Hz/5mA hi-pot for one minute between pri to sec.
AC 1.5K V /60Hz/5mA hi-pot for one minute between pri to core.
AC 1.5K V /60Hz/5mA hi-pot for one minute between sec to core.

3.4 Insulation test：

The insulation resistance is between pri to sec and windings to core measured by DC 500V, must Be over 100MΩ.

3.5 Terminal strength：

1.0Kg on terminals for 30 seconds, test the breakdown.

UNIT	m/m	DRAWN	CHECK	TITLE	TRANS
TEL	(02)2215-8302	Ci wun Chen	Guo long Huang	IDENT N O.	TRN-0246
FAX	(02)2215-8293	SEN HUEI INDUSTRIAL CO.,LTD.		D W G N O.	
No.26-1, Lane 128, Sec. 2, Singnan Rd., Jhonghe City, Taipei County 235, Taiwan					

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7. Bill of Materials

Item Number	Part Reference	Part Number	Quantity	Description (Manufacturer)
1	F1	TAPING	1	Metal-Oxide Resistor 1W-S 10Ω ±5%
2	R3 R9	REEL	2	SMD Resistor 0805 30Ω ±5%
3	R7	REEL	1	SMD Resistor 0805 300Ω ±5%
4	R2	REEL	1	SMD Resistor 0805 1KΩ ±1%
5	R8	REEL	1	SMD Resistor 0805 2KΩ ±1%
6	R6	REEL	1	SMD Resistor 0805 2K2Ω ±1%
7	R1	REEL	1	SMD Resistor 0805 4K7Ω ±1%
8	R4	REEL	1	SMD Resistor 1206 200KΩ ±5%
9	C5	8*11	1	Electrolytic Capacitor 4.7μF 400V 105°C
10	C9	6*11	1	Electrolytic Capacitor 47μF 50V 105°C
11	C4	6*11	1	Electrolytic Capacitor 1μ 400V 105°C
12	C8	6.3*11 LEK (Low ESR)	1	Electrolytic Capacitor 330μF/10V 105°C
13	C3	(Low ESR) ky10/220-L	1	Electrolytic Capacitor 220μF/16V 105°C
14	C1	Z5V	1	Ceramic Capacitor 102P 1KV +80/-20%
15	C10	9.4*3.6	1	Y2 Capacitor 222P 250V ±20%
16	C7	REEL	1	MLCC 0805 ±10% 223P 50V
17	C6	REEL	1	MLCC 0805 ±10% 224P 50V
18	L2	EC36-471K	1	Fixed Inductors 470μH ±10%
19	L3	DR475C 15μH	1	Inductor TRN0235
20	TX1	EE16,L=800μH,4PIN	1	TRN0246 Transformer
21	D1, D2, D3, D4, D5	1N4007	5	Diode 1A/1000V DIP
22	D7	SB260	1	Schottky Diode 2A/600V DO-15
23	U1		1	SMD IC FSQ500L
24	U2	TO92	1	REGULATOR TL431ACZ-AP ±1% (Fairchild Semiconductor)
25	U3		1	IC PC817 DIP
26	PCS		1	PCB PLM-0003 REV0

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8. Revision History

Rev.	Date	Description
1.0.0		Change User Guide EVB number from FEB257_001 to FEBFSQ500L_H257v1
1.0.1	3/6/12	Formatting & Editing pass by Tech Docs prior to posting

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