

### STEVAL-IME003V1

# STEVAL-IME003V1 demonstration board based on the STHV748 high voltage pulser

Data brief

#### **Features**

- 4-channel outputs: high voltage and low voltage BNC connectors
- Load simulator using signal equivalent circuits
- Possibility to set up own load simulator
- 16 preset waveforms
- USB connector to connect STM32 with PC and supply power to it
- 4 MB serial Flash memory to host FPGA code and waveforms
- Memory expansion connector to add external serial Flash
- Connectors to supply high voltage and low voltage to the STHV748 output stage
- LEDs to monitor the power management stage
- Human machine interface to select, start and stop the generation of the preset waveforms
- 25 LEDs to monitor board behavior
- RoHS compliant

#### **Description**

The STEVAL-IME003V1 demonstration board is designed around the STHV748 4-channel high voltage pulser, a state-of-the-art device designed for ultrasound imaging applications.

The output waveforms can be displayed directly on an oscilloscope by connecting the scope probe to the relative BNCs. 16 preset waveforms are available to test the HV pulser under varying conditions.



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Schematic diagrams STEVAL-IME003V1

## 1 Schematic diagrams

Figure 1. STEVAL-IME003V1 hierarchical blocks **⊣** ∯ +VFPGA\_IO\_3V3 USB\_DISCONNECT STM32\_FLASH\_BLK BOARD\_POWER MCU\_3V3 MCU\_3V3 STM32\_FLASH



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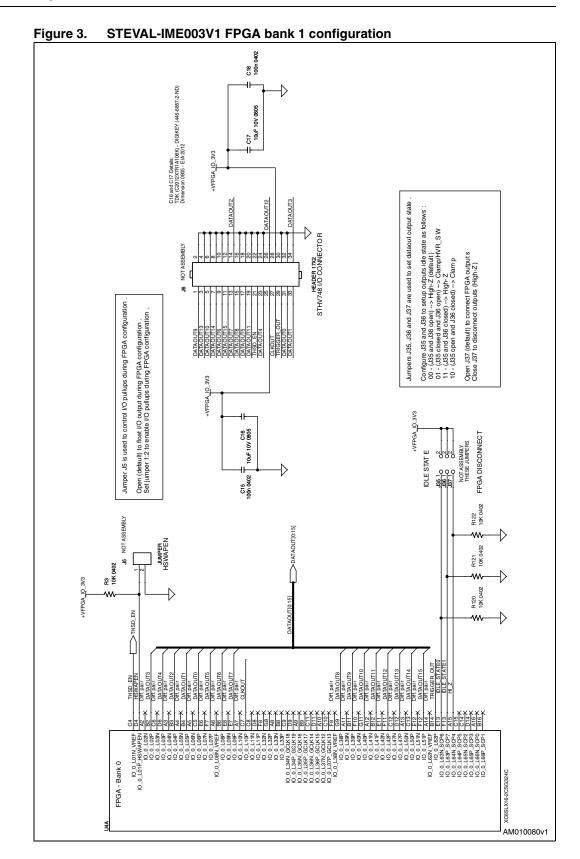
HIGH VOLTAGE J2 Details T RS 2X(193-0564) Phoenix Contact (Mfg Code MKDS 1.5/2-5.08) J3 Details: AS (193-0570) FIS (193-0570) FIS (193-0570) (Mfg Code MKDS 1.5/3-5.08) LOW POWER HIGH VOLTAGE Phoenix Contact (Mfg Code MKDS 1.5/3-5.08) SHELD SHIELD HVM1 GND VDDP GND VDDM DVDD HVP1 HVP0 GND Μ Η ^ 강 GND\_ (193-0570)ಪ 22000n 16V C1, C2, C9, C10 Details: GND POWER Digikey (445-5217-2-ND) - TDK (CKG57NX7S2A226M) Package 6.5mm x 5.5 mm Power STHV748 Power Management C4, C5, C6 Details: Digikey (445-1436-2-ND) - TDK (C3225X5R1C226M) Package 1210 - EIA 3225 GND\_POWER 2 16V HVM 22000n 100V 2000n 100V GND GND\_POWER  $\aleph$ 9 낊 22000n 16V ဗ 100 හ  $^{\circ}$ 22000n 16V →+VFPGA\_CORE\_1V2 22000n 100V 22000n 100V S DVDD A VDDM 2 ± 5 ≥ 5 HV MV H ►MCU\_3V3 C14 Detail TDK (C2012X7R1A106K) - DIGIKEY (445-6857-2-ND) Dimension 0805 - EIA 2012 VUSB\_DISCONNECT VUSB\_DM VUSB\_DP W R124 L1 Detail TDK (VLF4012AT-2R2M1R5) - RS (614-3147) MCC Kingbright KP2012SURC RS: 466-3829 Farnell: 8529930 LED 0805 FB/Vo SΝ Power Management GND 5 USB\_DISCONNECT FLASH\_3V3 C8 Details: DigiKey (478-2552-2-ND) - AVX (TACL225M006XTA ) Package 0603 క్ర Ä C7 Details: Digikey (445-4998-2-ND) - TDK (C1005X5R0J105K) Package 0402 Ш C13 4u7 6.3V D1 D4 6DP USB ON U1 SOTT323-6L 7 PED RED Grd 3.3V D3 3.3V D2 D28 C12 and C13 Detail TDK (C1608X5R0J475K) - Digikey (445-5178-2-ND) Dimension 0603 - EIA 1608 R90 56R ON\_1b COM\_1b ON\_2b USBDP 1 DISCONNECT 음 담 USB\_3V3 10 0<sup>2</sup>
NOT ASSEMBLY C8 2.2uF 6.3V RS (515-1995) Molex (54819-0572) ₹ J4 Details Phoenix Contact (Mfg Code MPT 0.5/2-2.54) RS (220-4260) ON\_1a C12 4u7 6.3V LDS3985M33R ON\_2a COM\_1a USB\_miniB EXT\_3V3 OND GND SHELL SHELL SHELL SHELL SHELL VBUS DM DP SW1 Details: SW1 MR RS 711-8329 KNITTER-SWITCH (MMS228T) L O GND nc გ <u>4</u> 1 HNI 3 BYPS 2 Z ⋝ FLASH\_3V3 3V3 Connector Ε₹ USB\_3V3 EXT\_3V3 USB\_5V 2 ± ∏ AM010079v1

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Figure 2. STEVAL-IME003V1 FPGA bank 0 configuration

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Schematic diagrams STEVAL-IME003V1





#11 W 36R 0402 € ≩ **PUSHBUTTONS** C23 100nF CTRL LED C28 100nF 020 10 F C19 100nF PDN 66MHZ EXTERNAL OSCILLATOR PERIPHERRAL MODULE (PMOD) 8 8 C26 10uF 10V 0805 BACKUP OF U5 MCU\_FPGA\_OSC\_EN FPGA USER I/O AM010081v1

Figure 4. STEVAL-IME003V1 FPGA bank 2 configuration

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Figure 5. STEVAL-IME003V1 FPGA bank 3 configuration R39 NA 0402 R40 NA 0402 MCU\_FPGA\_INIT\_B MCU\_FPGA\_MODE1 . R18 2K430402 DNP R22 2K43 0402 MCA A PEGA When FPGA\_INIT\_B (bidirectional open-drain) is Low the configuration memory foldered:
When held Len, the start of configuration is delayed.
When good guidence, a Low on this output indicables that a configuration dat a renor has coordined. C34 100nF ₩ 2X7R1A106K) - DIGIKEY 0805 - EIA 2012 R21 2K43 0402 DNP R17 2K430402 C33 10uF 10V 0805 Place R38 close to the FPGA device SPI FLASH CTRL SIGNALS FPGA CONFIGURATION 33R2 0402 SZ # R16 10K 0402 H38 CON10 R127 EXT SPI FLASH Place D29 close to J10 9 SPI EXTERNAL PROGRAMMING HEADER TEST POINT | O 2 LON NO CAPMASO | O 2 LON FPGA - Bank 2

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Figure 6. STEVAL-IME003V1 FPGA bank 3 configuration

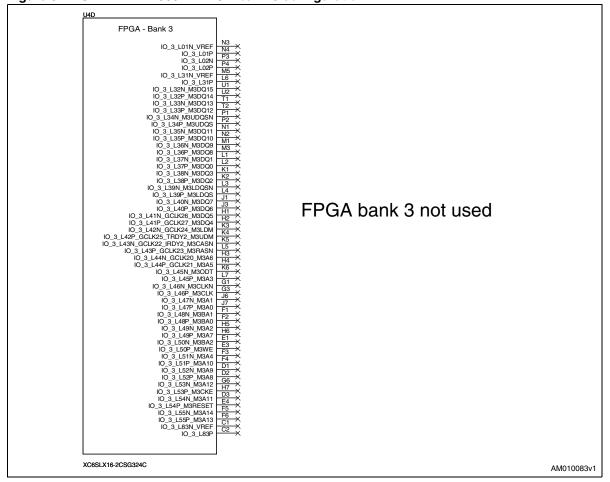


Figure 7. STEVAL-IME003V1 FPGA power and configuration C43 0.22uF 6.3V 0402 C54 0.22uF 6.3V 0402 C61 0.22uF 6.3V 0402 C69 0.22uF 6.3V 0402 C72 0.22uF 6.3V 0402 C36, C37, C38, C41, C42, C52, C53, C59, C60, C67, C68 Detail s TDK (C1608X5R0.475K) - Digikey (445-5178-2-ND) Dimension 0603 - ElA 1608 C42 4.7uF 6.3V 0603 CS3 4.7uF 6.3V 0603 O80 4.7uF 6.3V 0603 022uF 6.3V 0402 C71 = 022uF 6.3V 0402 C56 022uF 6.3V 0402 C49 022uF 6 C41 = 4.7uF 6.3V 0603 C52 4.7uF 6.3V 0603 C59 4.7uF 6.3V 0603 C63 0.22uF 6.3V 0402 C55 = 0.22uF 6.3V 0402 C70 0.22uF 6.3V 0402 C48 0.22uF 6 C40 100uF 6.3V 1206 C58 100uF 6.3V 1206 C51 100uF 6.3V 1206 C66 100uF 6.3V 1206 C35, C40, C51, C58, C66 Details Murata (GRM31CR60J107ME39L) - Digikey (490-4539-1-ND) Dimension 1206 - EIA 3216 C39 0.22uF 6.3V 0402 C47 0.22uF 6.3V 0402 C38 4.7uF 6.3V 0603 C46 0.22uF 6.3V 0402 R51 56R D23 GREEN C37 4.7uF 6.3V 0603  $\Omega$ C45 0 22uF 6.3V 0402 +VFPGA\_IO\_3V3 +VFPGA\_CORE\_1V2 FPGA\_DONE R52 330 0402 C36 4.7uF 6.3V 0603 C44 022uF 6.3V 0402 C35 100uF 6.3V 1206 P13 V2 V17 A17 B18 D16 D15 To be plac near U3 C73 100nF R42 49R 0402 R41 49R 0402 R50 10K 0402 P46 10K 0402 R49 10K 0402 SUSPEND & CMPCS\_B D22 STTH102A 100nF () FPGA JTA G J11 NOT ASSEMBLY RST1 FPGA PROG **FPGA JTAG** PROGRAM B RS (378-6527) To be placed near U6 AM010084v1



J16, J17, J22, J23, J25, J26, J29 and J30 Detail Tyco Electronics (1-1537482-0) - RS (420-5401) CZ7, C30, C111, C112 Detail Digitsy (490-1482-2401) Murata (GRM188R72A2714A010) D1, D2, D3, D4, D5, D6, D7, D8 diode DFLS1200 rs-code 708-2334 J16, J17, J22, J23, J25, J26, J29 and J30 Details Tyco Electronics (1-1337482-0) - RS (420-5401) 10k 759 100 1 1<u>5</u>₹ 20p 0805 POINT C75 ᄩᄚᆛ S S O O STHV748 XDCR\_C EZS J15 EZS J16 EZS J19 EZS J19 EZS J21 HVOUT\_D IN1\_D IN2\_D IN2\_C 220n LVQJT\_C IN3 D IN3\_C VDDP VDDM 11828 GNDPW GNDPW **⊕**≌ XDCR\_D XDCR\_C LVOUT\_D LVOUT\_C D31 KDFLS1200 D33 VDFLS1200 LVOUT\_B D35 PDFLS1200 D38 KDFLS1200 XDCR\_B C78 220g C108 GNDPW LVQJT\_A VDDP IN3\_B IN2\_B IN1\_B 17 ≱ HVM1\_A HWM1\_B XDCR\_B 20p 0805 –**⊕**≅ % . 75 100 1861 C114 80 C102 ล็ 11.0g ă N/A C110 H<sub>0</sub>8≸ £≸ -₩-NA NA NA THSD\_EN THSD\_EN AM010050v1

Figure 8. STEVAL-IME003V1 configuration of the STHV748

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**OSCILLATOR** FLASH READY PB4 JNTRST PB3 JTDO PA15 JTDI PA14 JTCK PA13 JTMS 10k 4 10k -₩-JTAG/SWD MCU Use J38 to enable/disable power for SPI flash device. J38 must be open when using external spi flash devic connecto J10. Default value closed. INT SPI FLASH 200 C123 FLASH DISABLE R128 OPTIONAL FPGA CONFIGURATION SIGNAL S DQ0 C C nS nW/Vpp/DQ2 nHOLD/DQ3 P64 ₩ 216 1001 1 £₩7 **OPTIONAL FPGA I/O** SPI FLASH FLASH\_DQ0 FLASH\_C FLASH\_nS FLASH\_nS FLASH\_DQ2 FLASH\_DQ3 AM010051v1

Figure 9. STEVAL-IME003V1 configuration of the STM32

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STEVAL-IME003V1 Revision history

## 2 Revision history

Table 1. Document revision history

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 11-Aug-2011 | 1        | Initial release. |

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