P-Channel 2.5-V (G-S) MOSFET

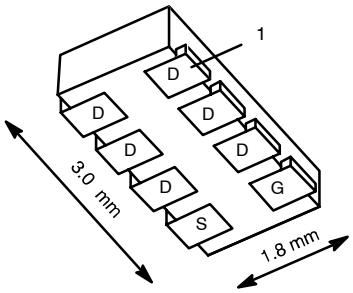
PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
−20	0.055 @ V_{GS} = −4.5 V	−5.3	11
	0.06 @ V_{GS} = −3.6 V	−5.1	
	0.083 @ V_{GS} = −2.5 V	−4.3	

FEATURES

- TrenchFET® Power MOSFET
- 2.5-V Rated

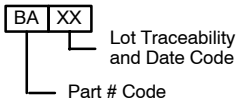
Pb-free Available

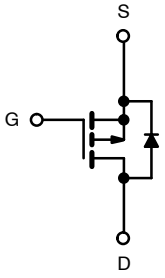
1206-8 ChipFET®



Bottom View

Marking Code





P-Channel MOSFET

Ordering Information: Si5441DC
Si5441DC-T1—E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	−20		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	−5.3	−3.9	A
	T_A = 85°C		−3.8	−2.8	
Pulsed Drain Current		I_{DM}	−20		
Continuous Source Current[a]		I_S	−2.1	−1.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	1.3	W
	T_A = 85°C		1.3	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	40	50	°C/W
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	20	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

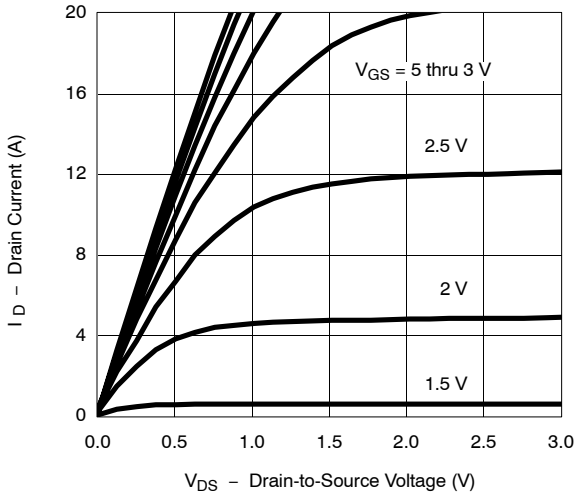
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.6		−1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −20 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −20 V, V_{GS} = 0 V, T_J = 85°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −3.9 A		0.046	0.055	Ω
		V_{GS} = −3.6 V, I_D = −3.7 A		0.050	0.06	
		V_{GS} = −2.5 V, I_D = −3.1 A		0.070	0.083	
Forward Transconductance[a]	g_{fs}	V_{DS} = −10 V, I_D = −3.9 A		12		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.1 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −10 V, V_{GS} = −4.5 V, I_D = −3.9 A		11	22	nC
Gate-Source Charge	Q_{gs}			3.0		
Gate-Drain Charge	Q_{gd}			2.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −10 V, R_L = 10 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_g = 6 Ω		20	30	ns
Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			65	100	
Fall Time	t_f			45	70	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.1 A, di/dt = 100 A/μs		30	60	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

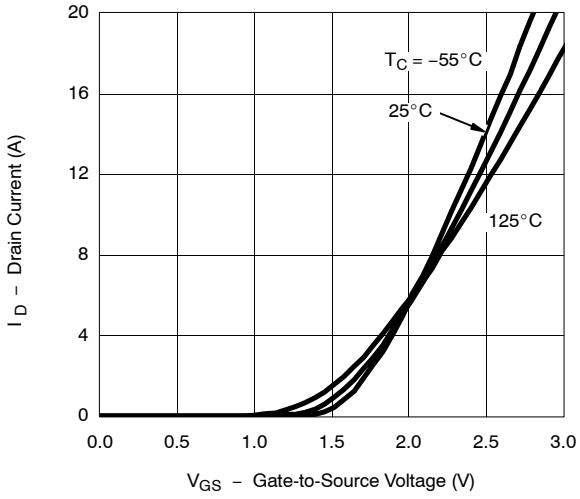
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

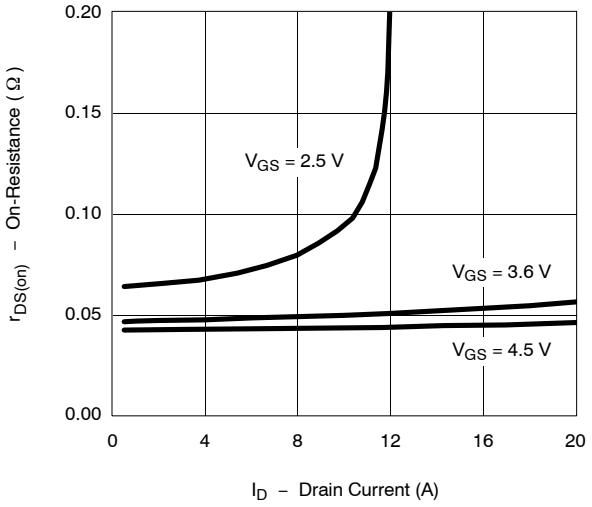


Transfer Characteristics

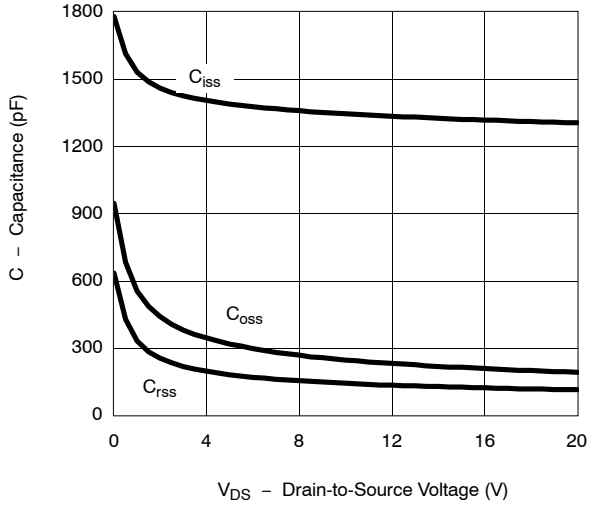


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

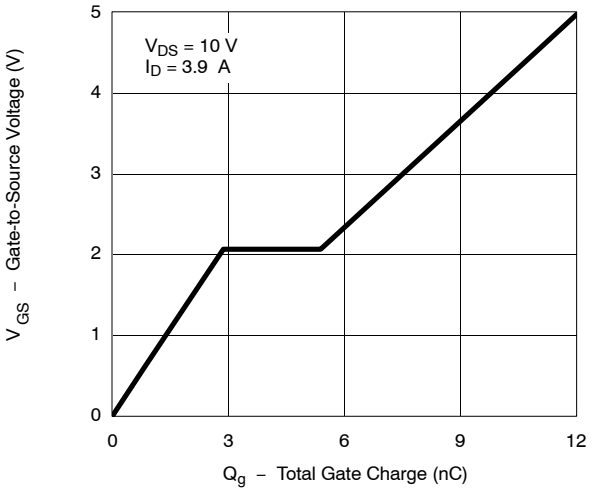
On-Resistance vs. Drain Current



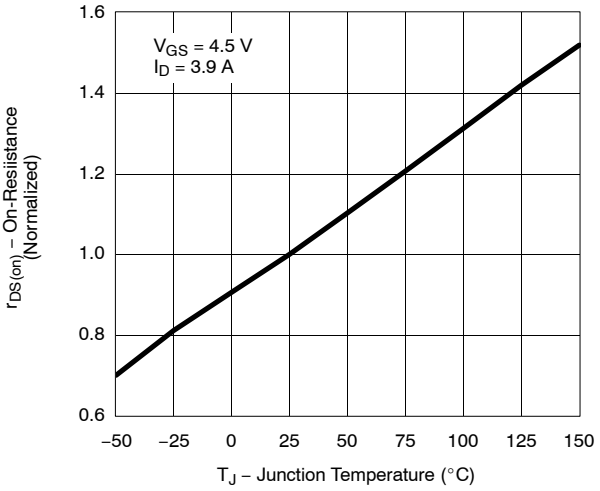
Capacitance



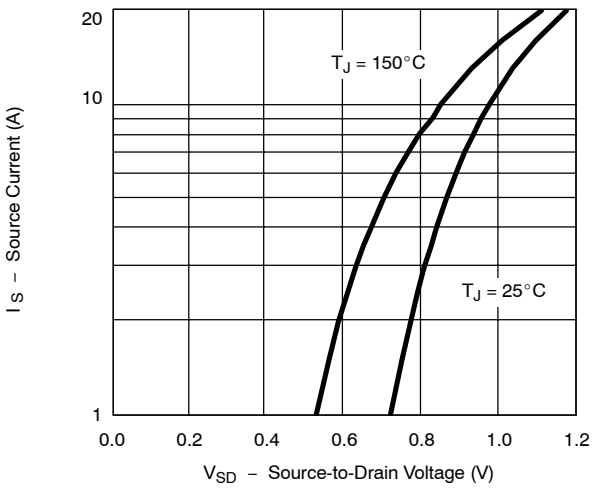
Gate Charge



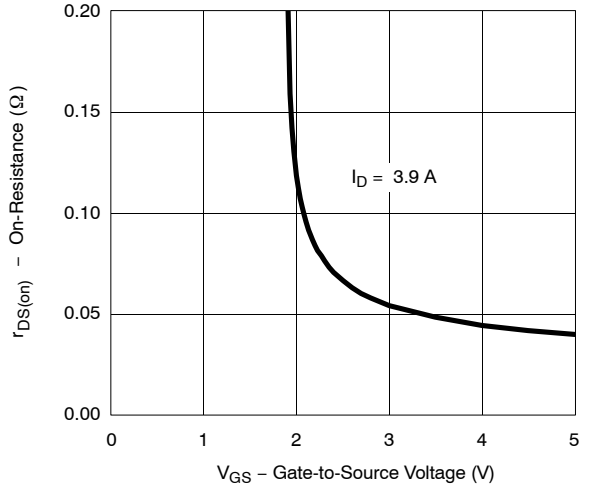
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

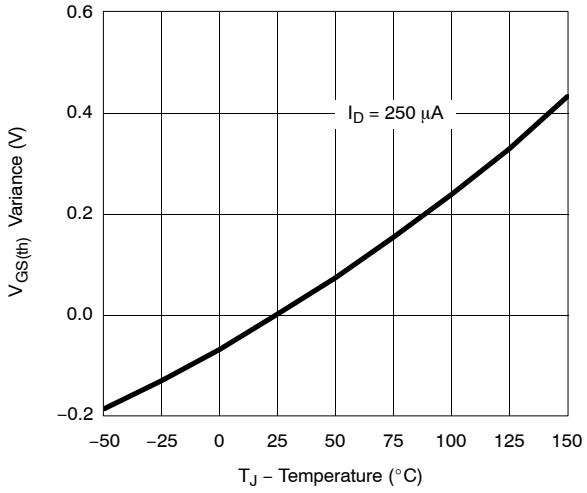


On-Resistance vs. Gate-to-Source Voltage

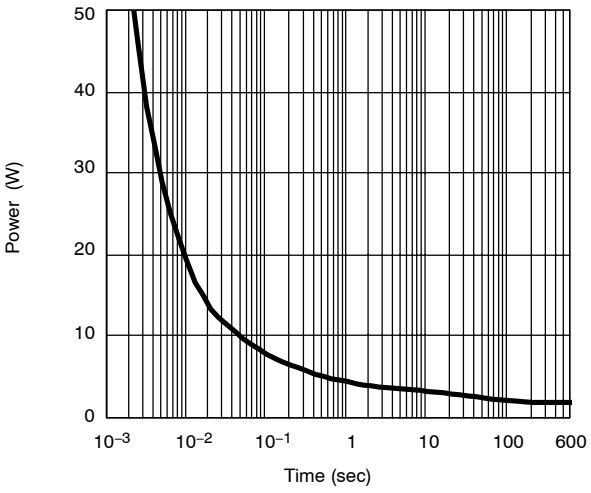


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

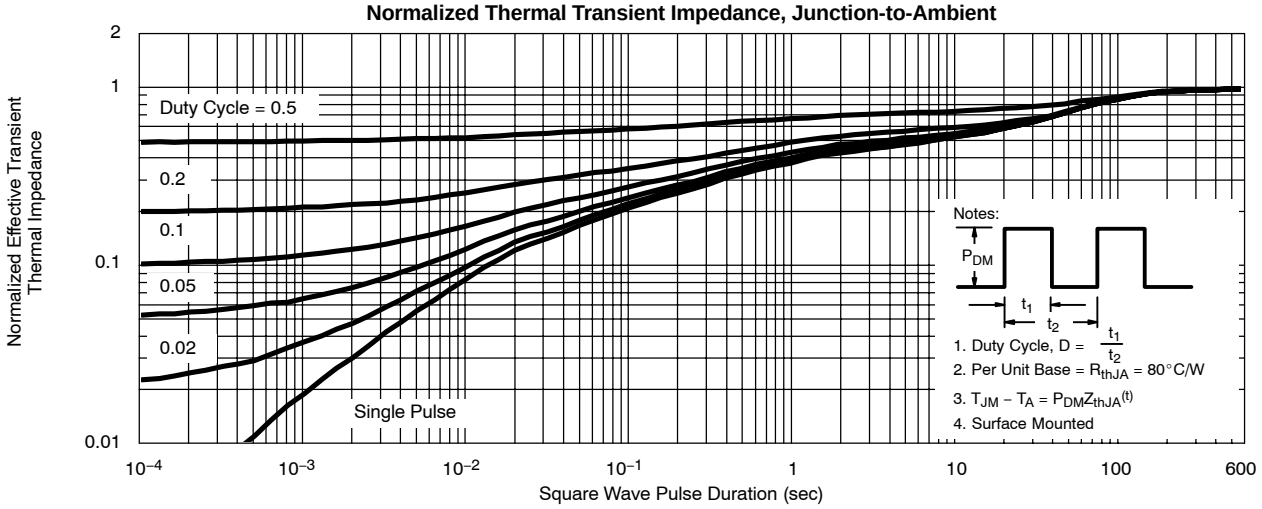
Threshold Voltage



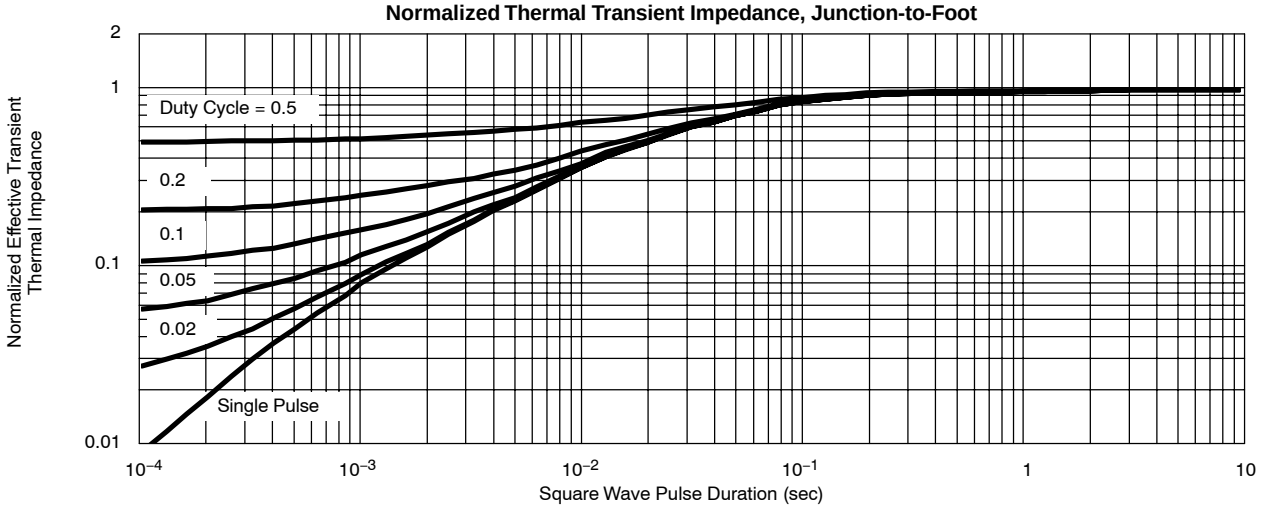
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71055.

Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.