AFBR-0544Z Evaluation Kit for the AFBR-5972Z Fiber Optic Transceiver

Application Note 5532

Evaluation Board

The AFBR-0544Z evaluation board gives the system designer a convenient means to evalute the performance of the Avago AFBR-5972Z fiber optic transceiver module, as well as future compatible products.

As shown in Figure 1, the evaluation board is mounted with an AFBR-5972Z module, four SMA connectors for differential input/output signals, a 2-pin header for measuring RF differential signals using a differential probe, and three 2 mm jacks for the 3.3 V supply voltage and signal detect (SD).

This application note describes the evaluation printed circuit board (PCB), the test equipment, and the methods for evaluating optical and electrical characteristics of the the AFBR-5972Z transceiver module.

Figure 1. Evaluation board for the AFBR-5972Z transceiver module

Application Note Outline

1. Evaluation kit
2. Evaluation PCB description
3. Electro-optical test configurations
4. Evaluation board schematic and bill of materials (BOM)

1. Evaluation kit

The AFBR-0544Z evaluation kit includes:

(a) Evaluation board with AFBR-5972Z module, four SMA connectors, 2-pin header and three 2 mm jack connectors and electronic components mounted on bottom side of PCB

(b) 1 m simplex POF cable (NA = 0.5)
- P/No. HFBR-RNS001Z

(c) AFBR-4526Z duplex connector for AFBR-5972Z

(d) 1 m POF, with two AFBR-4526Z duplex connectors
- P/No. HFBR-RSD001Z
(To demonstrate only the mechanical properties of the duplex connector)

Not included in the evaluation kit are:

(a) 3.3 V DC power supply and power supply cables

(b) Digitial multimeter

(c) MPI 1632C Digital Data Analyzer (Pattern generator)

(d) SDA 600A serial data analyzer (Oscilloscope)

(e) Femto (O/E) converter

(f) Differential probe

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2. Evaluation Board Description

The evaluation board schematic is shown in Figure 2. The transmitter is AC coupled and LVDS compatible as well as LVPECL compatible (Circuit diagram shown in application note - AN 5523), and the receiver is AC coupled and LVPECL compatible as well as LVPECL compatible (Circuit diagram shown in application note). The signal detect (SD) pin is LVPECL compatible The thick PCB trace between the SMA connector and the input/output pins of AFBR-5972Z represents a 50 Ω transmission line. The top- and bottom-sides of the evalution PCB are shown in Figure 3(a) and 3(b) respectively.

The evaluation board is a two-layer PCB designed for 125 Mbit/s. The transceiver differential lines are placed below the ground plane (top side) to ensure a low inductance signal return path and continuous impedance along the trace. The ground plane under/around the transceiver helps the tranceiver dissipate thermal energy. A 1.57 mm PCB thickness is used so that the AFBR-5972Z mounting clip can be fitted properly. For best transceiver performance, the decoupling capacitor and ferrite bead should be placed as close as possible to the tranceiver supply voltage, as shown in Figure 3(b).

Table 1 describes the input/output interface.The input/output interface is shown on the top side of the evaluation board.

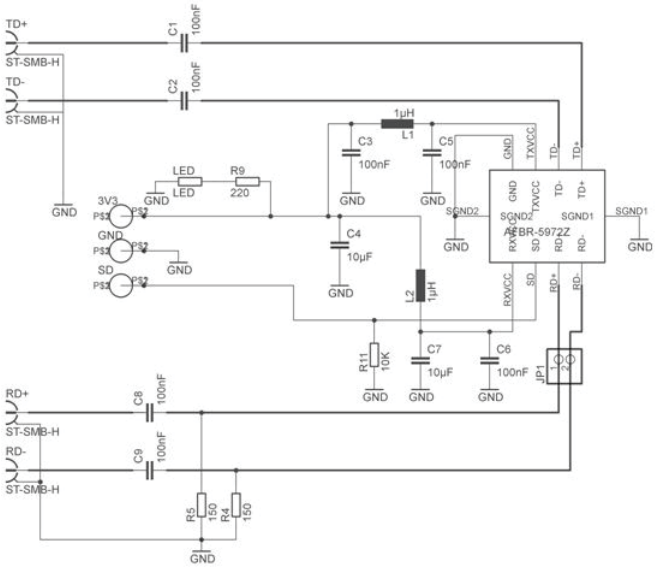

Figure 2. Schematic of the AFBR-0544Z evaluation board

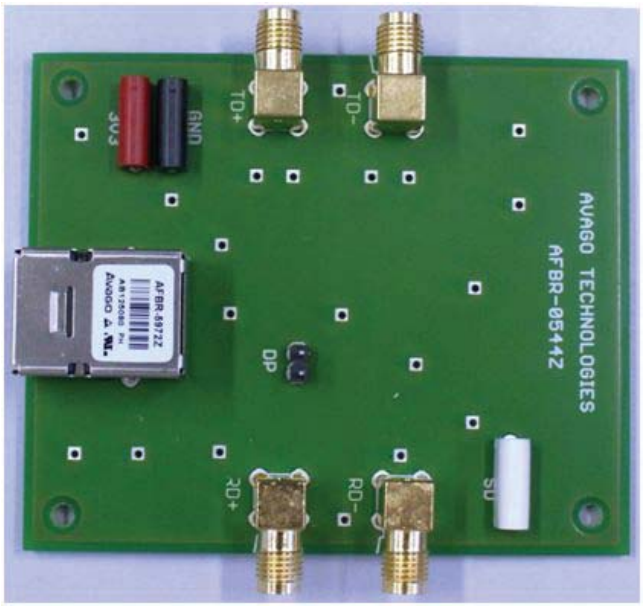

Figure 3(a). Top side of the AFBR-0544Z evaluation board

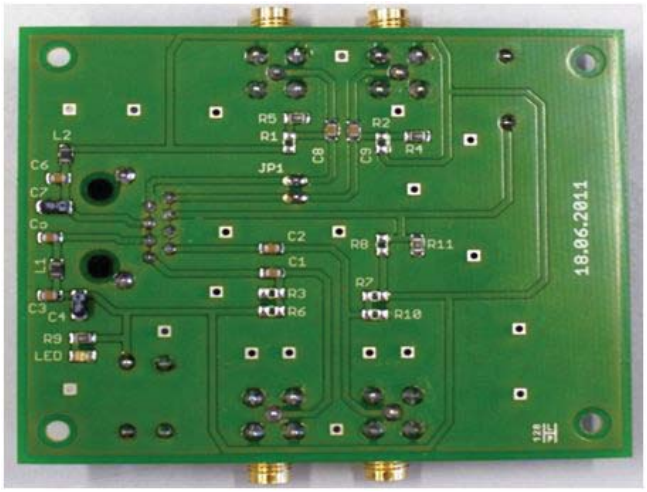

Figure 3(b). Bottom side of the AFBR-0544Z evaluation board

Table 1. Input/output description

Name	Description	Signal Level
TD+	Differential transmitter inputs	LVDS, LVPECL
TD-		
RD+	Differential receiver outputs	LVPECL
RD-		
SD	Signal detect	
DP	Differential receiver output signal for differential probe measurement	
3V3	Transmitter and receiver power supply	3.3 V
GND	Transmitter and receiver ground	GND

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3. Electro-Optical Test Configuration

The two basic test configurations for evaluating the AFBR-5972Z module are shown in Figure 4 (transmitter) and Figure 5 (receiver). The transceiver module can be characterized for optical/electrical characteristics such as eye diagram, rise and fall time, jitter, and current consumption. Low loss and matched equal length RF cables should be used to connect the TD+/- and RD+/- signals to the test equipment. The current consumption measurement is for the whole transceiver, transmitter and receiver.

Transmitter Measurement Configuration

Figure 4 shows the transmitter measurement configuration. The transmitter characteristics can be tested for light optical power (LOP), rise and fall time, and jitter performance, including the eye diagram measurement. In this configuration, the receiver section is not used; however, it is recommended that RD+ and RD- be terminated with 50 Ω matched loads. It is also recommended that a low loss and equal length RF cable can be used to connect TD+ and TD- to the test equipment.

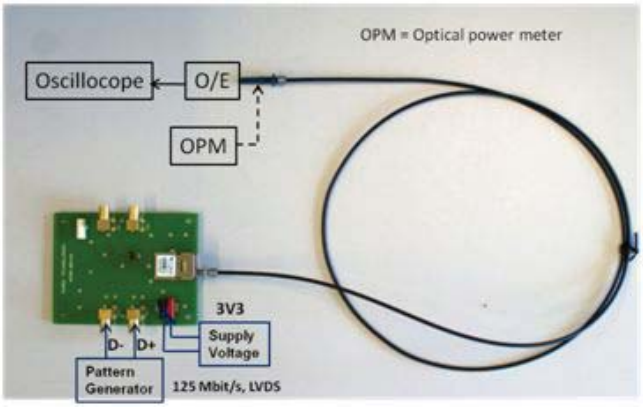

Figure 4. Transmitter measurement setup configuration

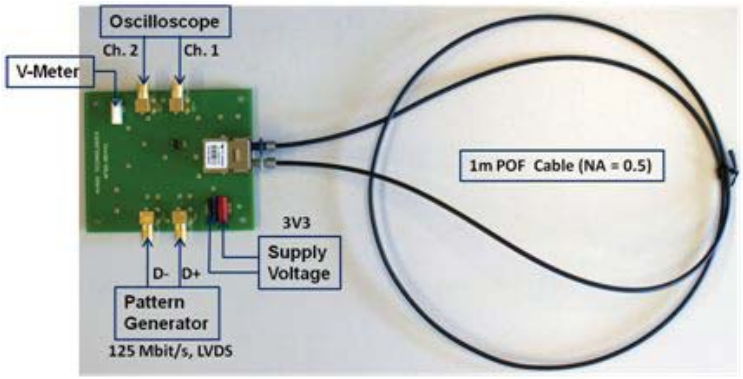

Figure 5. Receiver measurement setup configuration

Receiver Configuration

Figure 5 shows the receiver measurement configuration. The 1 m POF cable, which is provided with the evaluation kit, is used to obtain a transmission link between transmitter and receiver. The gray simplex connector is connected to the transmitter, and the blue simplex connector is connected to the receiver. The receiver characteristics can be tested for current consumption, rise and fall time, and jitter performance, including an eye diagram measurement.

Results

The measurements are carried out using the configuration shown in Figure 4 and Figure 5. The pattern generator is set to a PRBS 2^7-1 pattern and data rate of 125 Mbit/s with LVDS compatible differential signals. The transmitter light optical power (LOP), measured with an optical power meter (OPM) at 650 nm, was -5.57 dBm with a current consumption of 78 mA @ 3.3 V supply voltage.

Figure 6 shows the transmitter eye diagram after the optical-to-electrical converter block.

Figure 7 shows the receiver eye diagram measured with the differential probe at DP, as shown in Figure 3(a). The current consumption is 79 mA. The SD voltage is 1.63 V with no optical input and 2.33 V with an optical signal.

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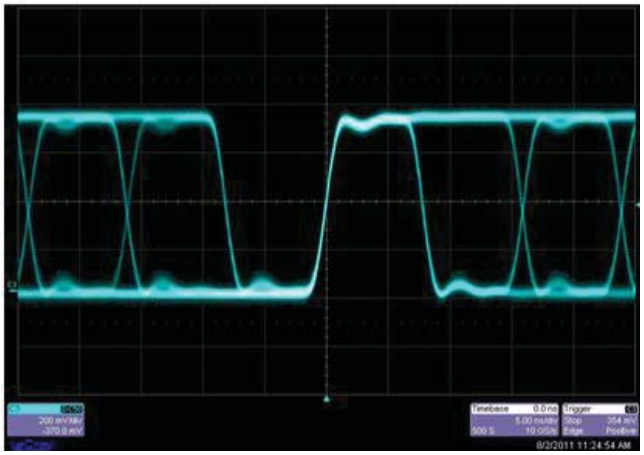

Figure 6. Transmitter eye diagram

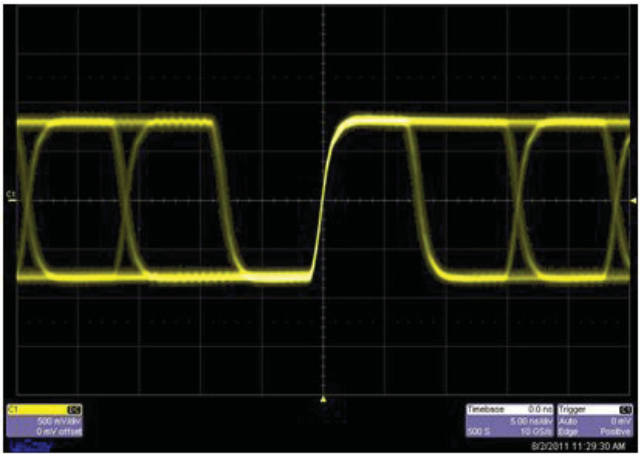

Figure 7. Receiver eye diagram

4. Evaluation Board Schematic and Bill of Material (BOM)

The AFBR-0544Z evaluation board electrical schematic is shown in Figure 2, and the bill of materials (BOM) is given in Table 2.

Resistors R1, R2, R3, R6, R7, R8 and R10 are not populated on the evaluation board. If they are populated and R4, R5, and R11 are changed to 82 Ω, then an AC coupled LVPECL compatible configuration results, as shown in Figure 8.

Table 2. AFBR-0544Z bill of materials

Component	Type	Value	Footprint	Comments
3V3	Jack, 2 mm			Red
GND	Jack, 2 mm			Black
SD	Jack, 2 mm			White
R1, R2, R6, R7, R8	SMD Resistor	130	R0805	Not populated
R3, R10	SMD Resistor	82	R0805	Not populated
R4, R5	SMD Resistor	150	R0805	
R9	SMD Resistor	220	R0805	
R11	SMD Resistor	10 kΩ	R0805	
C1, C2, C3, C5, C6, C8, C9	SMD Capacitor	100 nF	C0805	
C4, C7	SMD Capacitor	10 µF	C1206	Tantalum
JP1	Pin header		1X02	
L1, L2	SMD Inductor	1 µH	L0805	
LED	SMD LED		R0805	Green
TD+, TD-, RD+, RD-	ST-SMB			Farnell, part no. 1608609
AFBR-5972Z	Module		Datasheet AFBR-5972Z	

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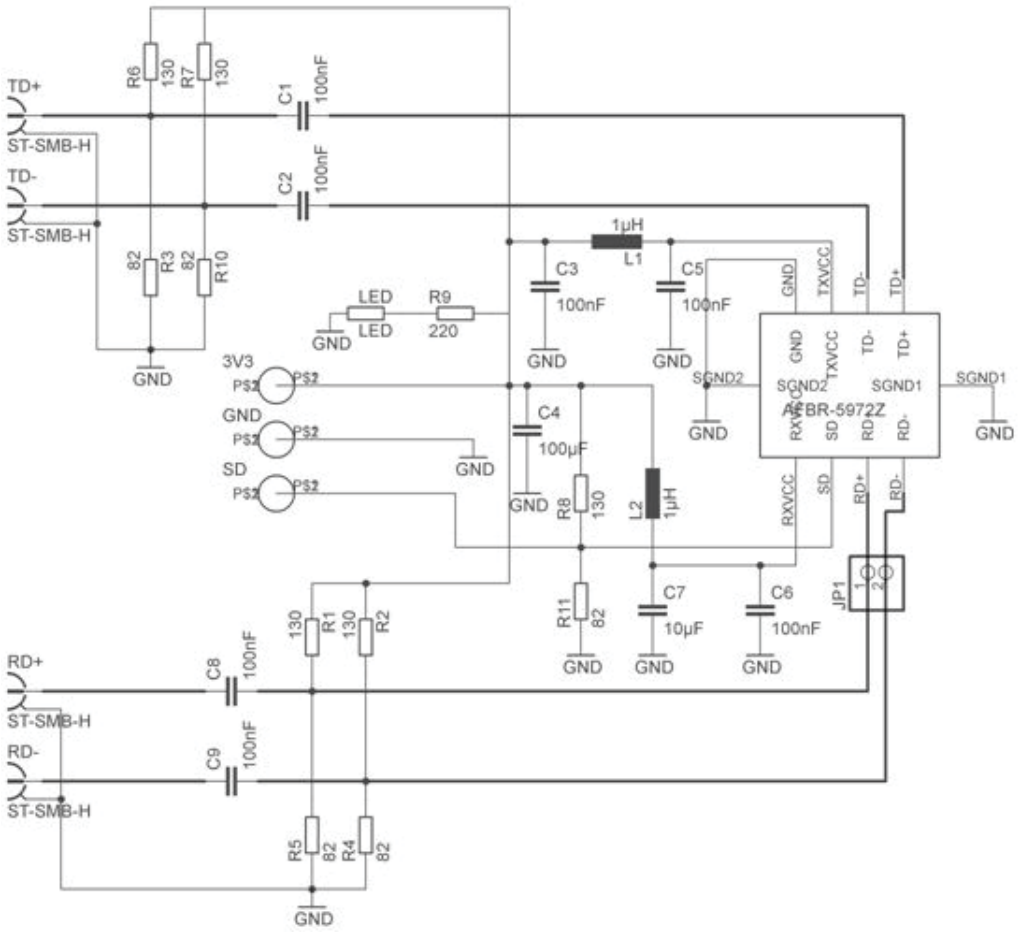

Figure 8. AC coupled LVPECL configuration

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