

N- and P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
N-Channel	12	0.235 at V _{GS} = 4.5 V	1.3
		0.280 at V _{GS} = 2.5 V	1.2
		0.340 at V _{GS} = 1.8 V	1.0
P-Channel	- 12	0.535 at V _{GS} = - 4.5 V	- 0.86
		0.880 at V _{GS} = - 2.5 V	- 0.67
		1.26 at V _{GS} = - 1.8 V	- 0.56

FEATURES

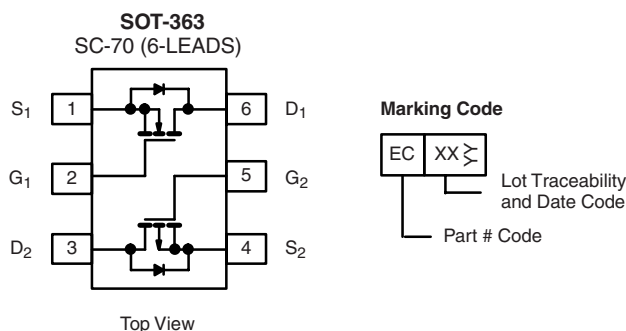
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Thermally Enhanced SC-70 Package
- Fast Switching to Minimize Gate and Switching Losses
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Baseband dc-to-dc Converter Switch for Portable Electronics



Ordering Information: Si1557DH-T1-E3 (Lead (Pb)-free)
Si1557DH-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel		P-Channel		Unit
			5 s	Steady State	5 s	Steady State	
Drain-Source Voltage		V _{DS}	12		- 12		V
Gate-Source Voltage		V _{GS}	± 8				
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	1.3	1.2	- 0.86	- 0.77	A
	T _A = 85 °C		0.9	0.8	- 0.62	- 0.55	
Pulsed Drain Current		I _{DM}	3		- 2		
Continuous Source Current (Diode Conduction) ^a		I _S	0.5	0.39	- 0.5	- 0.39	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	0.6	0.47	0.6	0.47	W
	T _A = 85 °C		0.3	0.25	0.3	0.25	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	170	210	°C/W
		220	265	
Maximum Junction-to-Foot (Drain)	R _{thJF}	105	125	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 100 μA	N-Ch	0.45		1	V	
		V _{DS} = V _{GS} , I _D = - 100 μA	P-Ch	- 0.45		1		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V	N-Ch P-Ch			± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 9.6 V, V _{GS} = 0 V	N-Ch			1	μA	
		V _{DS} = - 9.6 V, V _{GS} = 0 V	P-Ch			- 1		
		V _{DS} = 9.6 V, V _{GS} = 0 V, T _J = 85 °C	N-Ch			5		
		V _{DS} = - 9.6 V, V _{GS} = 0 V, T _J = 85 °C	P-Ch			- 5		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	3			A	
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 2				
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1.2 A	N-Ch		0.195	0.235	Ω	
		V _{GS} = - 4.5 V, I _D = - 0.77 A	P-Ch		0.445	0.535		
		V _{GS} = 2.5 V, I _D = 1.0 A	N-Ch		0.230	0.280		
		V _{GS} = - 2.5 V, I _D = - 0.6 A	P-Ch		0.735	0.880		
		V _{GS} = 1.8 V, I _D = 0.2 A	N-Ch		0.284	0.340		
		V _{GS} = - 1.8 V, I _D = - 0.2 A	P-Ch		1.05	1.26		
Forward Transconductance ^a	g _{fs}	V _{DS} = 5 V, I _D = 1.2 A	N-Ch		0.8		S	
		V _{DS} = - 5 V, I _D = - 0.77 A	P-Ch		1.2			
Diode Forward Voltage ^a	V _{SD}	I _S = 0.39 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V	
		I _S = - 0.39 A, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2		
Dynamic ^b								
Total Gate Charge	Q _g	N-Channel V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 1.2 A	N-Ch P-Ch		0.8 1.1	1.2 1.8	nC	
Gate-Source Charge	Q _{gs}		N-Ch P-Ch		0.15 0.3			
Gate-Drain Charge	Q _{gd}	P-Channel V _{DS} = - 6 V, V _{GS} = - 4.5 V, I _D = - 0.1 A	N-Ch P-Ch		0.20 0.25			
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 6 V, R _L = 12 Ω I _D ≅ 0.5 A, V _{GEN} = 4.5 V, R _g = 6 Ω	N-Ch P-Ch		15 17	25 25	ns	
Rise Time	t _r		N-Ch P-Ch		25 30	40 45		
Turn-Off Delay Time	t _{d(off)}		P-Channel V _{DD} = - 6 V, R _L = 12 Ω	N-Ch P-Ch		25 15		40 25
Fall Time	t _f		I _D ≅ - 0.5 A, V _{GEN} = - 4.5 V, R _g = 6 Ω	N-Ch P-Ch		10 10		15 15
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 0.39 A, dI/dt = 100 A/μs	N-Ch		20	40		
		I _F = - 0.39 A, dI/dt = 100 A/μs	P-Ch		25	40		

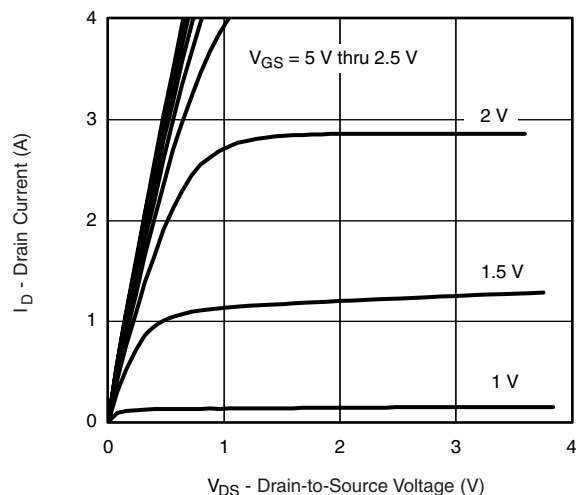
Notes:

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

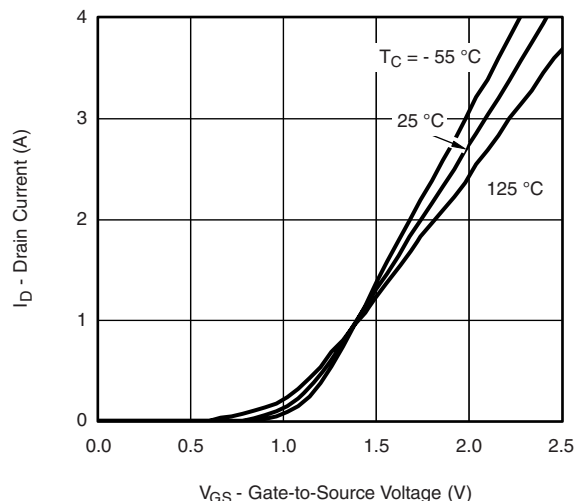
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

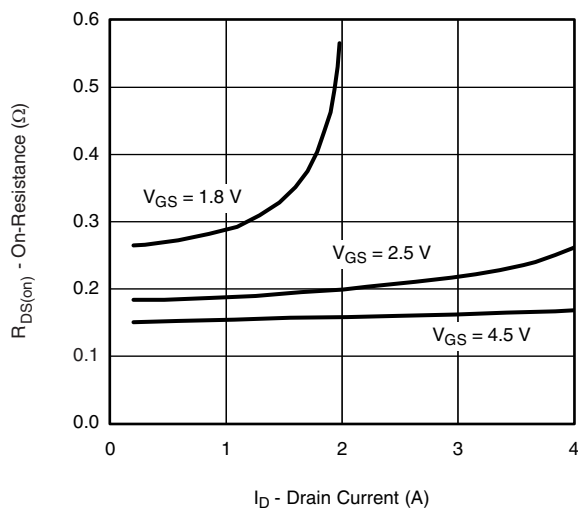
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



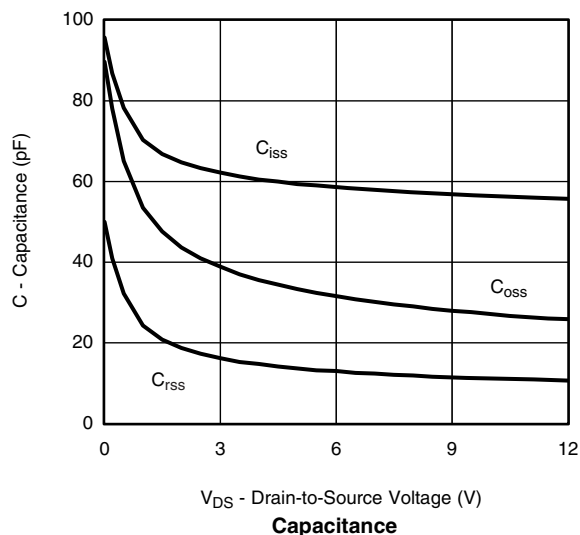
Output Characteristics



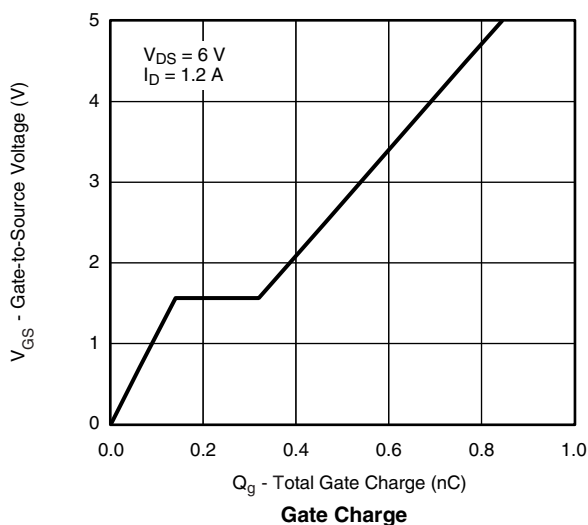
Transfer Characteristics



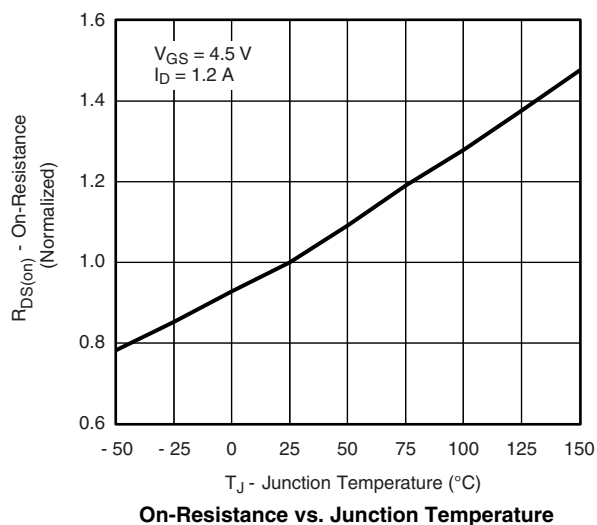
On-Resistance vs. Drain Current



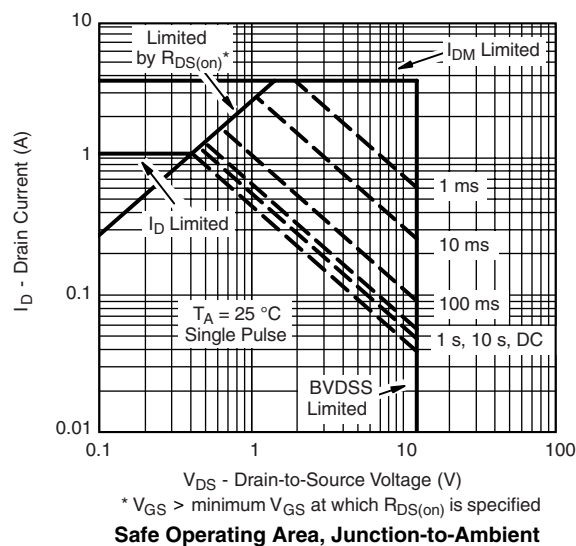
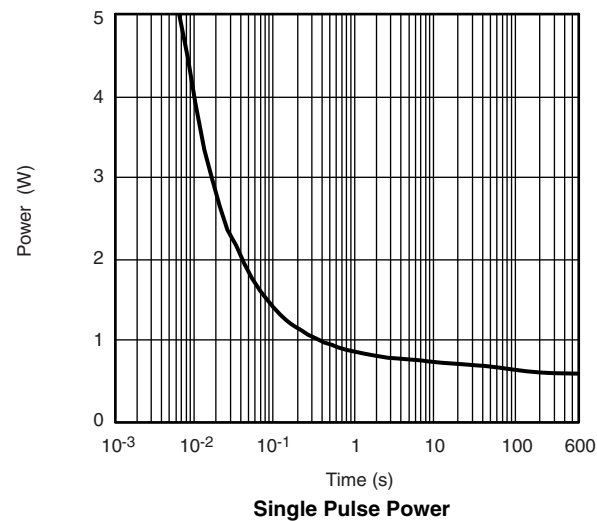
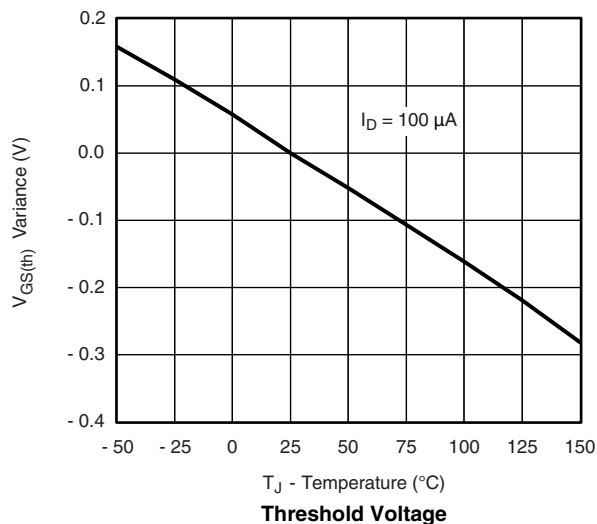
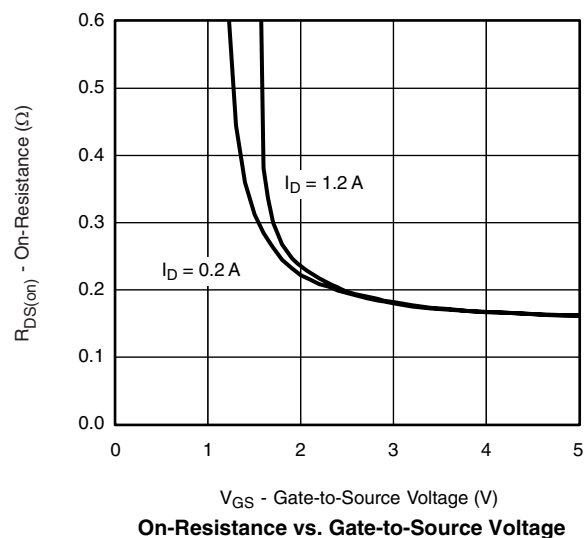
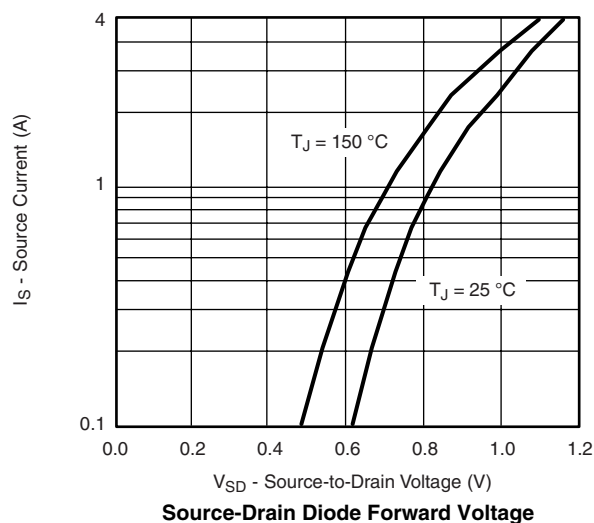
Capacitance



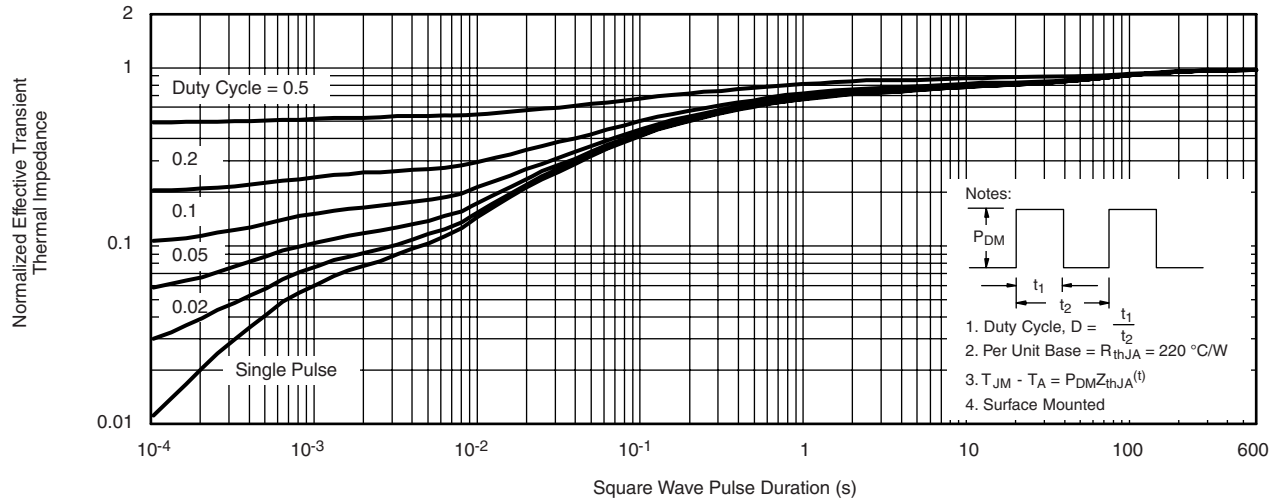
Gate Charge



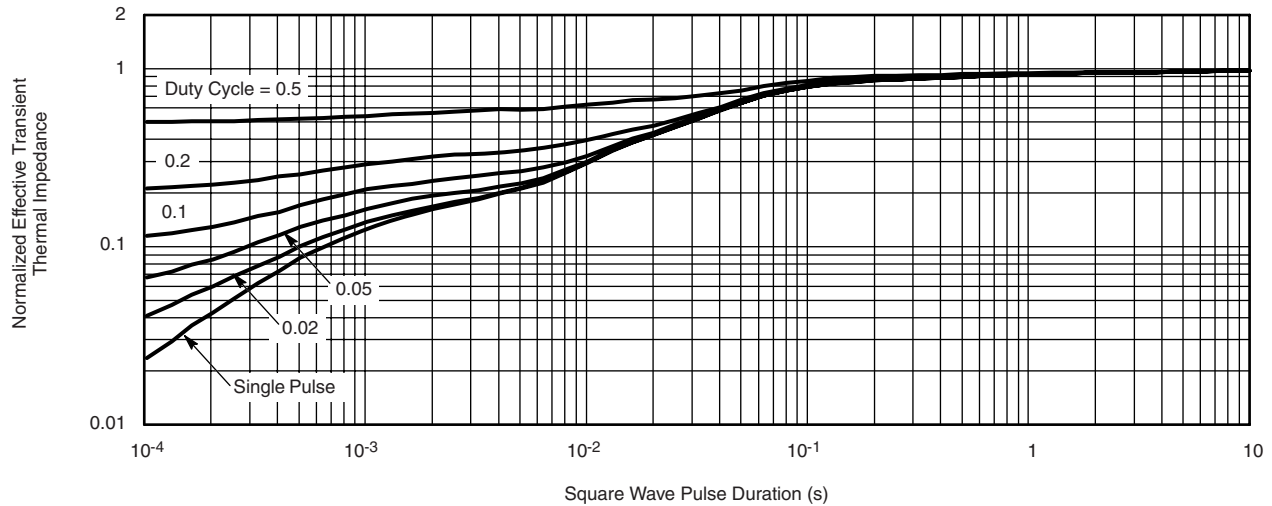
On-Resistance vs. Junction Temperature

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

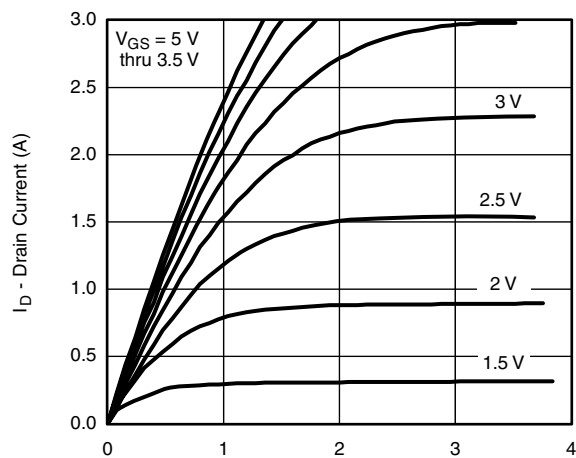
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



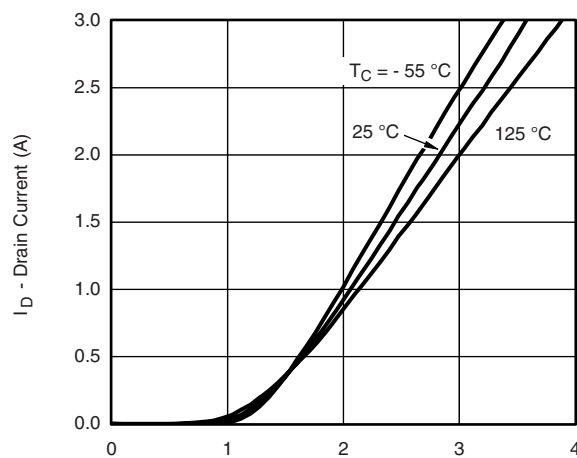
Normalized Thermal Transient Impedance, Junction-to-Ambient



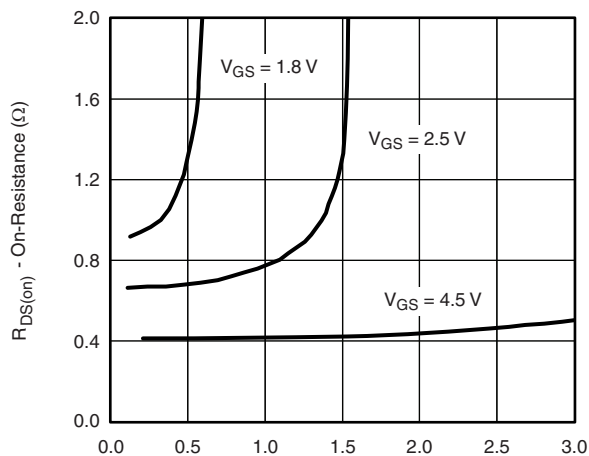
Normalized Thermal Transient Impedance, Junction-to-Foot

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

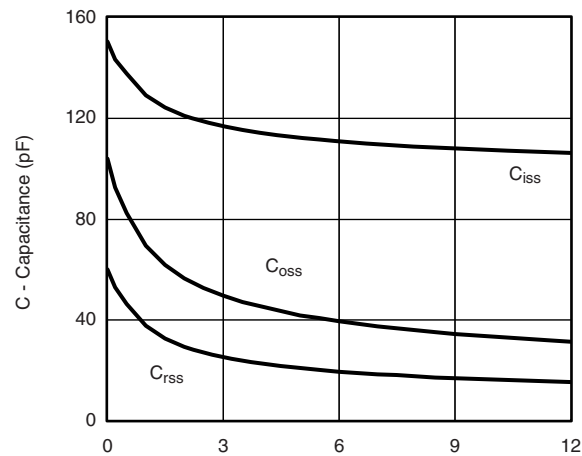
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



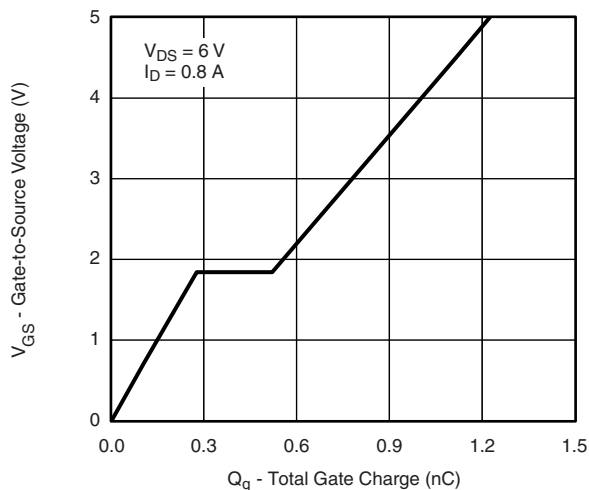
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



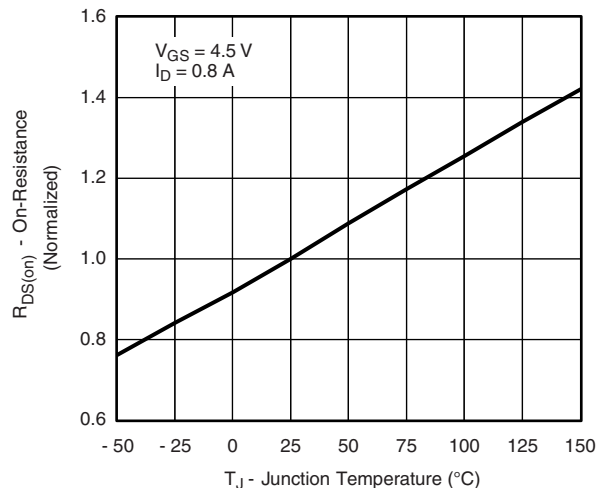
I_D - Drain Current (A)
On-Resistance vs. Drain Current



V_{DS} - Drain-to-Source Voltage (V)
Capacitance

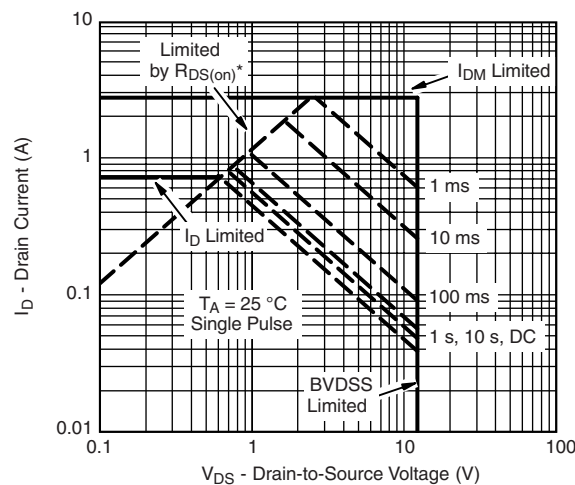
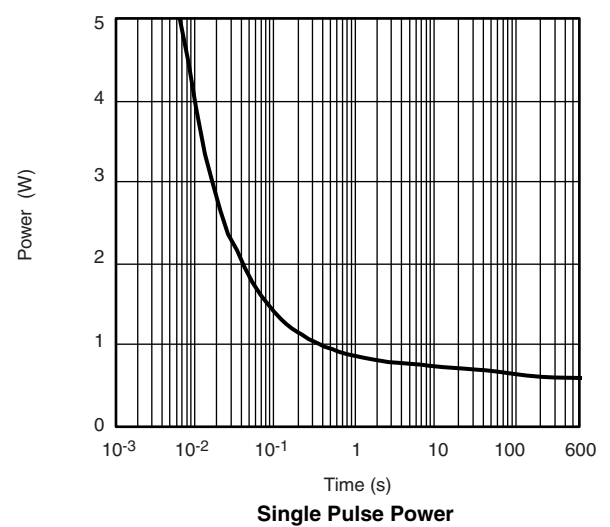
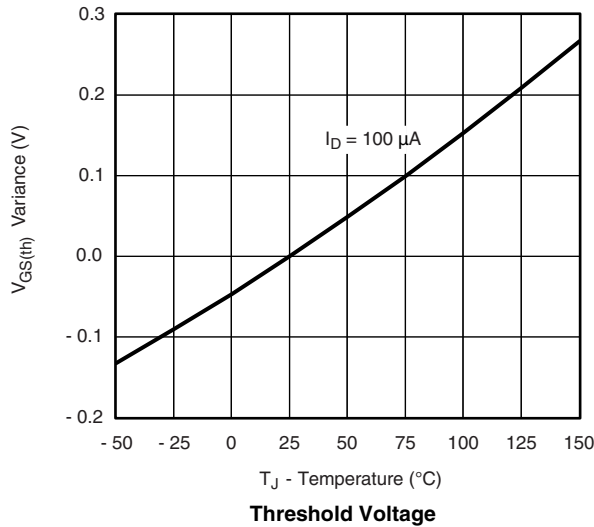
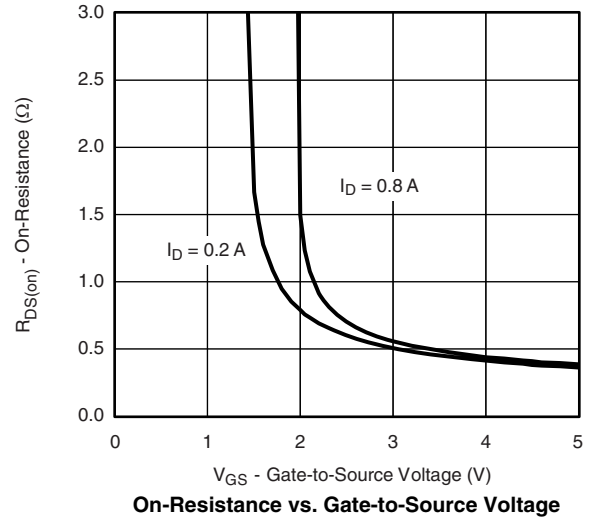
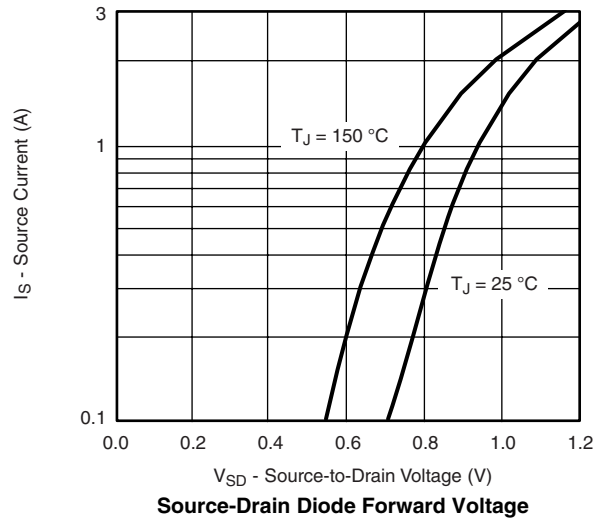


Q_g - Total Gate Charge (nC)
Gate Charge



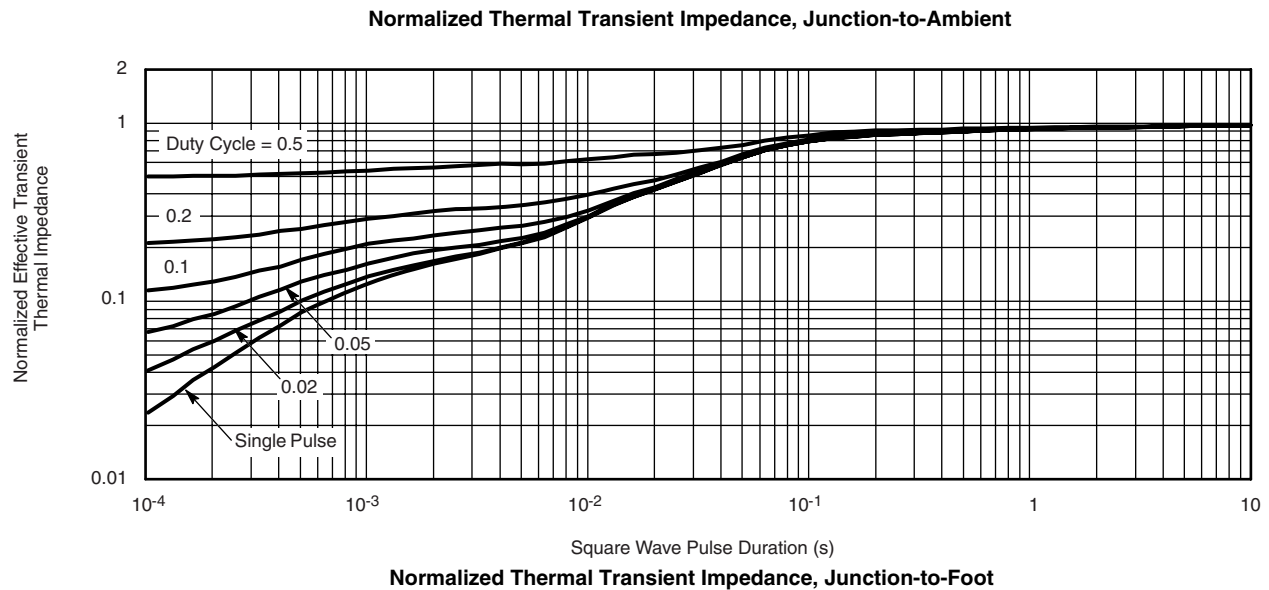
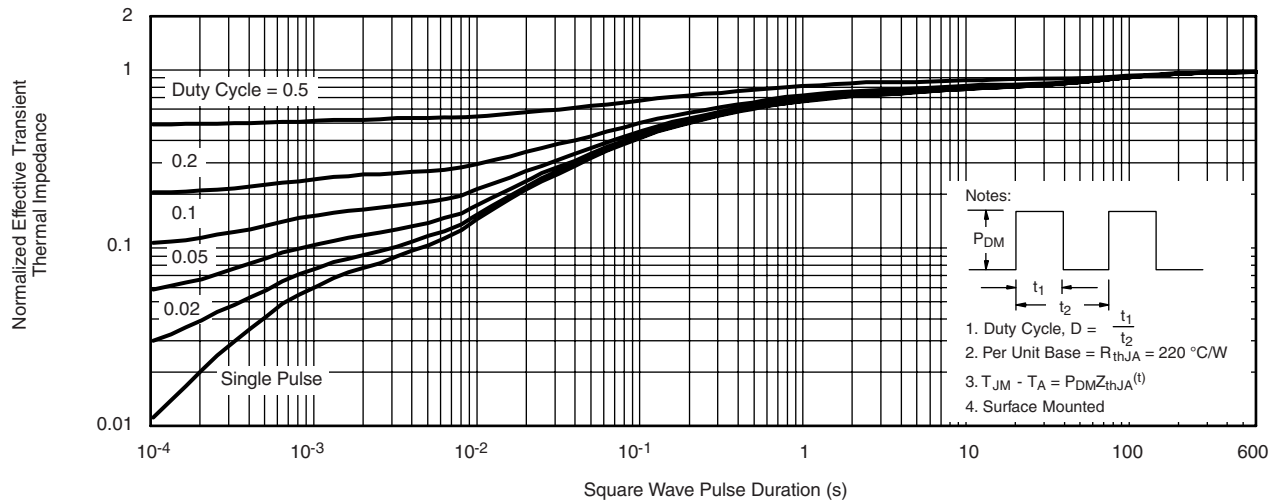
T_J - Junction Temperature ($^{\circ}\text{C}$)
On-Resistance vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



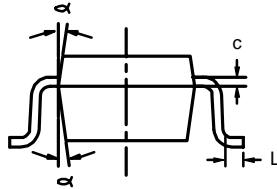
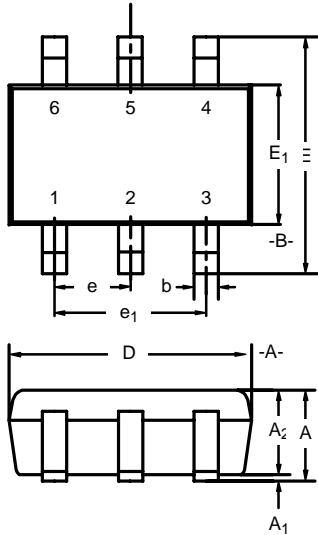
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71944.

SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	—	1.10	0.035	—	0.043
A ₁	—	—	0.10	—	—	0.004
A ₂	0.80	—	1.00	0.031	—	0.039
b	0.15	—	0.30	0.006	—	0.012
c	0.10	—	0.25	0.004	—	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5550

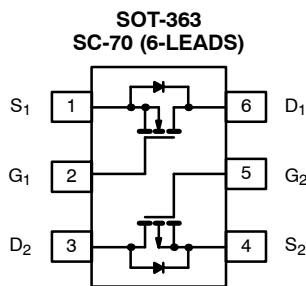
Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.



Top View
FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (<http://www.vishay.com/doc?71154>)

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

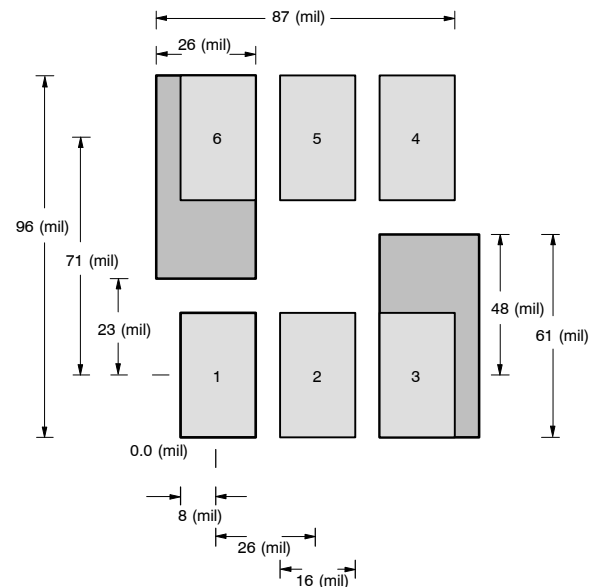


FIGURE 2. SC-70 (6 leads) Dual

EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch² PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

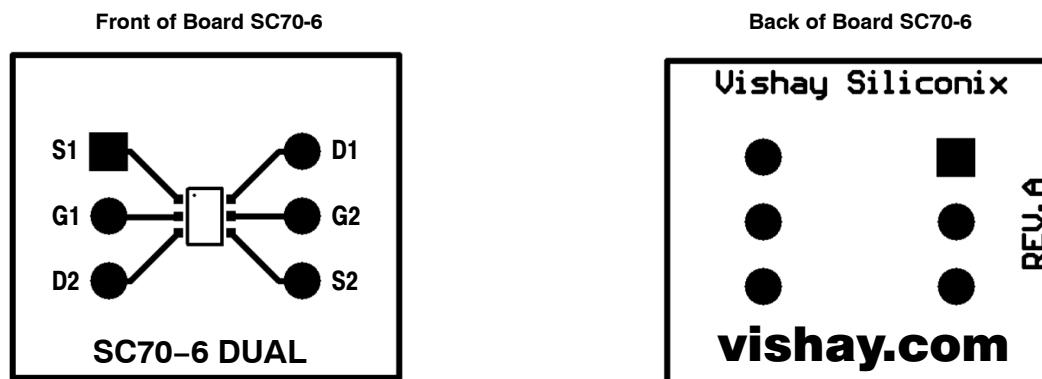


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the “foot” is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

Power Dissipation

The typical $R_{\theta JA}$ for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch² FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

Alloy 42 Leadframe

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
$P_D = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{413^{\circ}\text{C/W}}$	$P_D = \frac{150^{\circ}\text{C} - 60^{\circ}\text{C}}{413^{\circ}\text{C/W}}$
$P_D = 303 \text{ mW}$	$P_D = 218 \text{ mW}$

COOPER LEADFRAME

Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$
$P_D = \frac{150^{\circ}\text{C} - 25^{\circ}\text{C}}{224^{\circ}\text{C/W}}$	$P_D = \frac{150^{\circ}\text{C} - 60^{\circ}\text{C}}{224^{\circ}\text{C/W}}$
$P_D = 558 \text{ mW}$	$P_D = 402 \text{ mW}$

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R_{\theta JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

LITTLE FOOT 6-PIN SC-70

	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board (see Figure 3).	518°C/W	344°C/W
2) Industry standard 1-inch ² PCB with maximum copper both sides.	413°C/W	224°C/W

The results indicate that designers can reduce thermal resistance (θ_{JA}) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch² PCB area.

The Dual copper leadframe versions have the following suffix:

Dual: Si19xxEDH
 Compl.: Si15xxEDH

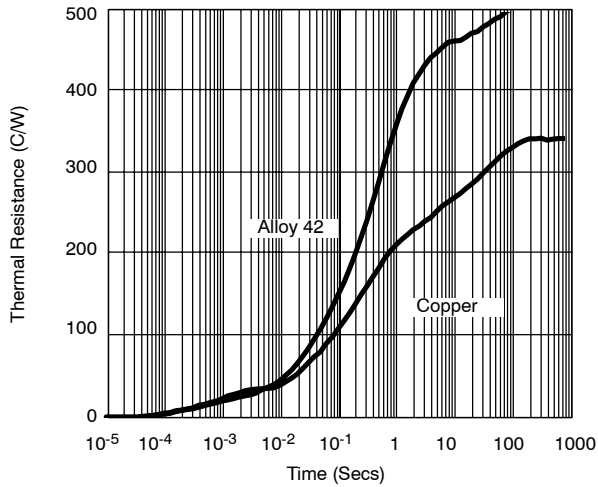


FIGURE 4. Dual SC70-6 Thermal Performance on EVB

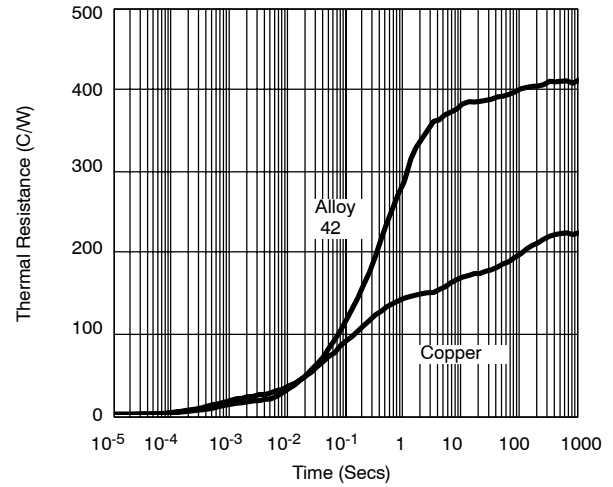
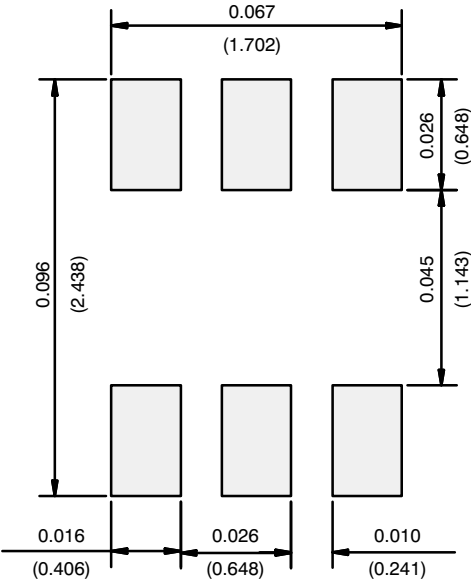


FIGURE 5. Dual SC70-6 Comparison on 1-inch² PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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