Quick start ADC1610S series (F1 or F2 versions)

Demonstration board for ADC1610S series

Rev. 5 — January 2011

Quick start

Document information

Info	Content
Keywords	PCB2131-1, Demonstration board, ADC, Converter
Abstract	This document describes how to use the demonstration board for the analog-to-digital converter ADC1610Sseries.

Overview





Revision history

Rev	Date	Description
1	20081001	Initial version.
2	20090518	Update
3	20090610	Add SPI software description.
4	20100519	Add HSDC extension module acquisition system description.
5	20110120	Update with latest software tool.

1. Overview of the ADC1610S demo board 1.1 ADC1610S F1 series (CMOS digital outputs) Figure below presents the connections to measure ADC1610S.



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1.3 Power supply

The board is powered either with a 3 V_{DC} and 1.8/3 V_{DC} power supplies or a 5V DC adaptor.

Table 1	. Power supply	
Name	Function	View
J8	2.1 Jack connector – 5VDC Change ST9 and ST10 position accordingly	J10 / J11 J8
J10	+3V green connector – Power supply 3 V_{DC}	
J11	Change ST9 and ST10 position accordingly CMOS version +1.8V green connector – Power supply 1.8 V _{DC} LVDS DDR version +3V green connector – Power supply 1.8 V _{DC}	
TP1	GND test point	
TP2	GND test point	

1.4 Input signals (IN, CLK)

The input clock signal can be either a sine wave or a LVCMOS signal.

To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

, where M is an odd number of period and N is the number of samples.

Table 2.	Input signals
Name	Function
J1	IN connector – Analog input signal (50 Ω matching)

- J2 CLKP connector Single ended clock input signal (50 Ω matching), with a transformer.
- J3 CLKM connector Grounded on that demoboard



1.5 Output signals in CMOS version (D0 to D15, DAV, OTR)

The digital output signal is available in binary, 2's complement or gray format. A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

View

Table 3. Output signals

Name	Function	View
J6	Array connector – ADC digital output (D0 to D15), OTR and Data Valid (DAV)	- J6

1.6 Output signals in LVDS DDR version

The digital output signal is available in binary, 2's complement or gray format. A Data Valid Output clock (DAV) is provided by the device for the data acquisition.

Table 4. Output signals

Name	Function	View
J7	Samtec QTH connector – ADC digital output (D0 to D15) and Data Valid (DAV)	

1.7 SPI Mode

The ADC1610S can be **controlled** either by a Serial Peripheral Interface (SPI) or by PIN.

Table 5. SPI Interface

Name	Function	View
J12	USB connector – SPI interface	

1.8 SPI program

For more details on how to control device with SPI, refer to section 3.3.

2. HSDC extension module: acquisition board

The figure 4 shows an overview of the extension module HSDC-EXTMOD01/DB acquisition board:



The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH_060_02 P2 connector).

The board brief specification is shown below:

- 32 MB memory size for acquisition pattern;
- 2 16-bit channels CMOS up to 200 MHz;
- 16-bit LVDS DDR input data stream up to 320 MHz;
- On-board or external reference for signal generation.

In this section the specific requirement for the use with ADC1610S demo-board will be shown.

For more details on the HSDC-EXTMOD01/DB, please contact <u>dataconverter-</u> <u>support@nxp.com</u>.

2.1 HSDC extension module: hardware initialization

Before using the generation board, make sure that you connect the USB cable **prior to** the supply.

When USB and power cable are connected, the HSDC-EXTMOD will light 3 red LEDs.

The green LED close to the PLL is only when it is locked (see section 3.3).

The red LED close to FPGA reports normal behavior when flashing $\frac{1}{4}$ on, $\frac{3}{4}$ off. Any other flashing behavior reports a failure at initialization (see section 3.3).

2.2 HSDC extension module: CMOS connector description

The <u>figure 5</u> shows a brief description of the hardware connection on the HE14 connector.

For proper use of the acquisition board, make sure that resistor R86 (0 Ω) is connected while R84 is removed.



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3. Combo 1610S and HSDC extension module

3.1 ADC1610S setup CMOS outputs

The <u>figure 24</u> below shows an overview of the whole system ADC1610S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1610S demo-board:





The <u>figure 24</u> below shows an overview of the whole system ADC1610S+HSDC extension module with CMOS outputs configuration for which connection is straightforward, together with a supply extension module (release A) for the ADC1610S demo-board:



Quick start

3.3 ADC Software tool

Run the application "SW_ADC_1_r02.exe". This application will allow:

- the user to control features on our high speed ADC through the SPI interface available on any ADC1610S series;
- As well as performing any online data acquisition to evaluate the performances of the ADC1610S series.

At start-up, the program will detect any board connected to your system and display information as can be seen on following window:

Detrice detected; Notice 10012 ACC - Functional Register: ACC - Read Register: Tools Acquisition Tools Sendering: Sendering: Fired fa: F	Copyright NKP semiconductors 2010	REFRESH Stop acquisition before any action. NXP HSDC ADC acquisition softw	vare	3 Stop acquisition be	QUIT efore any action.
Number of sangle: State Delay ADC0 Data stream: Image: Construction of sangle: Autocode Image: Construction of sangle: Image: Construction of sangle: Autocode Image: Construction of sangle: Image: Construction of sangle: Autocode Image: Construction of sangle: Image: Construction of sangle: Autocode Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Construction of sangle: Image: Cons	Device detected; ADC15105125 Resolution 16 Sampling rate Fs (max. 125 Mpps) 122.88 Tinput frequency Fin (max. 600 MHz) 5	ADC - Functional Registers ADC - Load Registers Tools Acquisition Acquisition Fin and Fis are: Fixed its: Fis coherent (Hs) Select window type: Orderent PF: 122.844-922-66 Store to Rie Line Header Results Rie S	Info	ax. 255 trials)	
Openos Description Openos Instructuration Openos Instructuration </th <th>Number of samples 65536 🗸</th> <th>FFT Spectrum Reorganized Signal Universitäted Signal Hatogram Autoscale</th> <th>1</th> <th>405 11</th> <th></th>	Number of samples 65536 🗸	FFT Spectrum Reorganized Signal Universitäted Signal Hatogram Autoscale	1	405 11	
OLIDS Oligon Frequency Skot Skot INITIALIZATION Image: State of the s	⊙ CMOS	1	ADC Digitized signal	ADC Ur	ut
April Labor 0.073 dBFS NTIALIZATION 0 0 0.073 dBFS Output log 0 0 0 dBFS SR 70.02 dBFS Divisit ADELSISS found 0 0 0 dBFS SR 70.02 dBFS Divisit ADELSISS found 0 0 0 dBFS SR 70.02 dBFS Divisit ADELSISS found 0 0 0 dBFS dBFS dBFS Divisit ADELSISS found 0 0 dBFS dBFS dBFS Divisit ADELSISS found 0 0 dBFS dBFS dBFS Divisit ADELSISS found 0 dBFS dBFS dBFS dBFS dBFS Divisit	OLVDS	20*	Frequency	5.000 MH	17
Are set times SAVE SETTINGS Single Set Set Set Set Set Set Set Set Set Se		0-	Amplitude	-0.973 dBF	FS
Instruction System TO 02 dbc Output log 90 <td< td=""><td></td><td>HIZ</td><td>ADC AC parameters</td><td></td><td></td></td<>		HIZ	ADC AC parameters		
A SNR 70.99 def5 Corpus log 0	~	-20 -	SNR	70.02 dBo	c
INITIALIZATION Image: mail of the second secon	(4)		SNR	70.99 dBF	FS
SAVE SETTINGS SAVE SETTINGS Lumph lag Lumph lag Lumph lag Lumph lag Lumph lag Lumph lag Mode Lumph lag Mode Lumph lag Mode State		-40	SINAD	69.83 dBo	c
Cupul log PPD 84.15 dbc HEDC-EXTINCS found SPDR 84.15 dbc Device ADC: INSUITION 10 to instance PPD 84.15 dbc SAVE SETTINGS SMM SETTINGS SMM SETTINGS SMM SETTINGS	INITIALIZATION	(P)	ENOB	11.31 bits	5
SAVE SETURICS SAVE SETURICS Code seture	Output log		SFDR	84.15 dBd	c
Devise ADCLISITE is found Production	LICEC EXTROD Swedt	H3	SFDR	85.13 dBF	FS
HEDC-ExtMOD is initiated -100- -120- -120- -140- -140- -140- 0 -100- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- -140- 0 -100- -140- 0 0 0	Device ADC1610S125 found	2 100 H2 H4	THD	-83.51 dBo	c
SAVE SETTINGS SAVE SETTINGS Land Land Land Land Land Land Land Land	HSDC-EXTMOD is initialized!		ADC Harmonics		
-120- -120- <td< td=""><td></td><td></td><td>H2</td><td>-101.443 dBo</td><td>c</td></td<>			H2	-101.443 dBo	c
-140- -115- -115- -115- -115- -115- 120- -115- 120- -115- 120- -115- 120- -115- 120- -115- 120-		-120 -	H3	-85.127 dBo	c
-140- -160- -150- -150- -150- -150- -151- -1		ditter disconstances (1) is an exclusion of the second state of the second state of the second	H4	-101.987 dBo	c
Application			HS	-94.528 dBo	c
SAVE SETTINGS SM 10M 15M 20M 25M 30M 35M 30M Max 62009 codes Max 62009 codes			H6	-115.425 dBd	<u>c</u>
0 SM 10M 15M 20M 2SM 30M 3SM 30A4 Prequency (Hz) Max 62099 codes Max 62099 codes Max 02099 codes		-160 - 1 1 1 1 1 1 1 1	ADC Code excursion		
SAVE SETTINGS Max 62099 codes		0 5M 10M 15M 20M 25M 30M 35M 38.4M	Min	3472 coc	des
L Pl and 32784.38 codes	SAVE SETTINGS	Frequency (Hz)	Max	62099 coc	des
	SITUAL	+ 💌 🕪	Mean	32784.38 coo	des
DESTORE SETTINGS	PESTOPE SETTINGS				

①: "NXP Banner Button" will display your default internet browser to the NXP data converter home page;

②: "REFRESH" allows you to poll your system for any hardware change. It will reset any board connected to your system;

③: "QUIT" allows you quit the application;

④: "INITIALIZATION" allow you to initialize the HSDC-EXTMOD board prior to any acquisition task.

In the example above, the HSDC-EXTMOD has been detected, as well as ADC1610S125.

At this moment, make sure that 4 LEDs are visible on the HSDC-EXTMOD (2 close to power plug, 1 for USB and 1 close to FPGA).

The "Info" page gives more details on the current hardware configuration for the HSDC-EXTMOD board:

SW_ADC_1			
copyright NoP semiconductors 2010	REFRESH	HSDC ADC acquisition software	QUIT
Device detected; ADC/16/03/13 C Resolution 35 122.88 Input frequency Fin (max. 125 Mpp) 122.88 Input frequency Fin (max. 500 MHz) 5 Data stream 0 Data stream 0	ADC - Functional Registers ADC - Read Registers ADC - L HSDC-EXTMOD serial number: 272 . software version HSDC software version is 2.0. dll version HSDC-EXTMOD version is 3. HSDC-EXTMOD version is 3.	ead Registers Tools Acquisition Info +3.3Y CLK +3.3Y VIO edge. PLL LMK03001 locked	
Fig 8. SW_ADC_1	r02: "Info" page		

The HSDC-EXTMOD is not yet initialized, so the embedded PLL (LMK03001 in this example) is not locked. Initialization is only required for acquisition purpose.

3.3.1 ADC SPI programming Functional Registers page

opyright NXP semiconductors 2010	REFRESH NXP HSDC ADC a	acquisition software
Device detected: ADC16105125 Resolution 16 Simpling rate Fs (max. 125 Maps) 122.89 Juput frequency Fin (max. 600 MHz)	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tr ADC16105125 SPI registers access	ools Acquisition Info Reset and Operating Mode SW EST OP, MODE normal (power-up)
IS Number of samples 65336 ℃ Data stream OCMO5 UVD5	Input Clock SE_SEL DIFF/SE CLUMIN DUFF/SE CLUMIN DOF DIFF/SE CLUMIN DUFB/SE CLUMIN DOF DIFF/SE CLUMIN DUFB/SE	Internal Reference INTREF_EN OdB (FS=2V) Utput Data Standard UtDS/CMOS UTBUF_OUTBUS_SWAP DATA_FORMAT offset bmary Cffset
INITIALIZATION Output log HSDC-EXTMOD found Device ADCISIDSIS found HSDC-EXTMOD found	DAVINV DAV PHASE output clock shifted (shead) by 5/16Tck. Test Pattern TESTPAT_SEL Off CMOS Output	DIG_OFFSET -22 -20 -10 0 10 20 31 Patt OTR FASTOTR FASTOTR PASTOTR_DET -20.55 dB √ LVDS DDR ofP 182
SAVE SETTINGS	DAV DRV DATA DRV very high T high T	DAVE_VEN DAVE DATAL DATALVEN DATAL BIT_OVEN VISE LUDS_INTER no internal termination T to device

The page displays all SPI registers for ADC1610S series:

Perform any settings and then click on the "Send data to device" button to update the device registers.

3.3.2 ADC SPI programming Read Registers page

This page can be used to read all registers by clicking on the "Read all registers" button and will display the result in the table below:

pyright NXP semiconductors 2010	REFRESH	NXP HSDC ADC acquisition softw	vare		QU	IT
ADC16105125	ADC - Functional Registers ADC - Read Re ADC1610S125 SPI read registers	gisters ADC - Load Registers Tools Acquisition I	Register page	Address	Usha	
ampling rate Fs (max, 125 Msps)			Repaired mention mode	riddress .	Value	
nput frequency Fin (max. 600 MHz)	Read all r	agisters	Clock		1	
· · · · · · · · · · · · · · · · · · ·			Internal reference	8	0	-
lumber of samples			Input buffer	10	3	
65536 🔽	Save register	read to file	Output data standard	11	0	-
	Data saved to file:		Output clock	12	9	
() LVDS	C:\test.txt		Offset	13	0	
			Test pattern 1	14	.0	
			Test pattern 2	15	0	1
			Test pattern 3	16	×0	
HSDC-EXTMOD found! Device ADC16105125 found!			Fast OTR	17	0	
HSDC-EXTMOD is initialized!			CMOS output	20	E	1
			LVDS DDR O/P 1	21	×0	1
			LVDS DDR O/P 2	22	×0	1
			(i	0	0	
SAVE SETTINGS			,			

When all registers have been read, it is possible to save the data to a text file. The settings are saved in a table-like format as shown below:

Table 6.	Typical	saving	on	text	file
----------	---------	--------	----	------	------

Content of file is shown as table format

Column 1	Column 2
Address	Value
05	00
06	01
08	00
10	03
11	00
12	09
13	00
14	00
15	00
16	00
17	00

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Column 1	Column 2
20	0e
21	00
22	00

Note that all data are saved in hexadecimal format.

Click on the "Save registers read to file" button to select the file to store data to. Make sure that you store your file with ".txt" extension, this will allow you to re-use the file on the "ADC - Load Registers" page.

3.3.3 ADC SPI programming Load Registers page

This page allows downloading configuration data to the device registers:

copyright NKP semiconductors 2010	REFRESH	HSDC ADC acquisition softwa	re		QU	IT
Device detected: ADC16105125 C Resolution 16	ADC - Functional Registers ADC - Read Registers ADC - Lo ADC16105125 SPI load registers Load data from text file (".txt"):	ad Registers Tools Acquisition Infr	A Register name	Address	Value	ŕ
Sampling rate Fs (max. 125 Msps)	C:\test.txt		Reset and operating mode	5	0	^
Input frequency Fin (max. 600 MHz)	1		Clock	6	1	1
	(2)		Internal reference	8	0	1
Number of samples	Load data		Input buffer	10	3	1
Data stream			Output data standard	11	0	1
O CMOS	(3)		Output clock	12	9	1
	download done!		Offset	13	×0	1
			Test pattern 1	14	0	1
			Test pattern 2	15	20	1
Output log			Test pattern 3	16	×0	1
HSDC-EXTMOD found Device ADC1610S125 found!			Fast OTR	17	0	1
PSDC=EXTWOD IS Initialized?			CMOS output	20	E	1
			UVDS DDR O/P 1	21	0	1
			LVDS DDR O/P 2	22	0	1
SAVE SETTINGS			J.	0	0	~

It is not necessary to have a file that has the whole set of registers listed. The only restriction is regarding the formatting of the file as given in <u>section 3.3.2</u>.

Note: this page cannot be used to download data saved during the comparison process.

To download settings onto device registers, follow the procedure below:

- Browse to select your file (button ①);
- Click on "Load data" button².

A message on field ③ and a progress bar will inform about the status of the operation until message "download done!" is seen. The table ④ is updated with the current values downloaded at the fly as can be seen on <u>figure 13</u>.

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3.3.4 Tools page

This page allows the user to calculate the coherent frequencies values involved of the acquisition process. It gives an indication where the 6 first harmonics are located in the Nyquist zone.

Enter your analog and sampling frequencies in field^①. Indicate the number of samples to be acquired^②, as well as the fixed parameter for the coherency calculation (Fs in our example above^③). Press "UPDATE GRAPH" to look at the frequency plan, it gives also the real Fin frequency (Refer to <u>appendix A.1</u> for more details on coherency calculation):



Note: The level of the harmonics shown does not reproduce the behavior of the ADC; they are only given as indication for location.

3.3.5 Acquisition page

copyright NKP semiconductors 2010	REFRESH NXP HSDC ADC acquisition softwar Step acquisition before any action.	ire	Stop acquisiti	QUIT
Device detected:	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquisition In	5		
ADC16105125				
Resolution	Acquisition	`		
16	Pin and Ps are: Pixed is: Ps conerent (Hz)	ET automation (1/10 /ma	2000 March	
Sampling rate Fs (max. 125 Msps)	Coherent Fin 122304642E #6	interaging Site (inte	0., 200 (10)	
122.88	Distance Dis			
Input frequency Fin (max. 600 MHz)	Store to file Line Header			
) (JIS				0-1
	Kepuis ne ja			
	6			
Number of samples	STUP Display ADCU			
(2)	FFT Spectrum Reorganized Signal Unreconstructed Signal Histogram Autoscale		0	
Data stream			(7)	
O CMOS		Item	ADL	Unit
OLVDS 3	20-	ADC Digitized signal	E 000	Millo
	0-	Amplitude	-0.973	dBES
	HI	ADC AC parameters	0.570	
	-20 -	SNR	70.02	dBc
		SNR	70.99	dBFS
INITIALIZATION	-40-	SINAD	69.83	dBc
	면 -60-	ENOB	11.31	bits
Output log	ў на	SEDR	84.15 er 12	dBc
HSDC-EXTMOD found	5 -00- H5	THD	-83 51	dBc
HSDC-EKTMOD is initialized!		ADC Harmonics	00101	
		H2	-101.443	dBc
	-120-	H3	-85.127	dBc
	والمعجر بالمالة بالمالية المترابط بالتلافية بمتعر أنتها فتعلموا بترجيع أأأله والمتراجع	H4	-101.987	dBc
		HS	-94.528	dBc
		H6 ADC Code suspension	-115.425	dBc
	0 5M 10M 15M 20M 25M 30M 35M 38.4M	Mo.	3472	rodes
	Frequency (Hz)	Max	62099	codes
SAVE SETTINGS	the General state	Mean	32784.38	codes
DECEMPTOR CENTRAL				
RESTURE SETTINGS			_	
	·			

This page will acquire data to evaluate the high dynamic performance of the device:

Before proceeding to any acquisition, the user needs to do the following entries:

- the sampling frequency Fs: 122.88 Msps in our example (field ①);
- the input frequency Fin: 5 MHz in our example (field ①);
- the number of samples to be acquired 65536 in our example (field 2);
- indicate whether it is CMOS or LVDS DDR (field ③);
- Press the "INITIALIZATION" button ④. It will initialized the HSDC-EXTMOD board:
 - FPGA is ready (red LED is flashing ¼ on and ¾ off) ;
 - PLL embedded is locked (green LED is on);
- indicate whether Fin or Fs are coherent or not (field (5)):
 - if signals are coherent, selected which Fin or Fs are fixed for the calculation (see <u>appendix</u> <u>A.1</u>);
 - If signals are not coherent, select the window for FFT processing to apply (the Blackman window gives better results).
- Press the "ACQUIRE" button (6) to display the results from the FFT processing. The results fields (7) will be updated automatically.
- press "STOP" ⑦ button to stop acquisition;
- field [®] allows to do FFT averaging over up to 255 trials, suitable for small signal analysis;
- Field ⁽¹⁾ allows storing dynamic results to text file. Click on the check box, enter a header as a comment and browse to indicate where to store data file. <u>Table 7</u> shows how data are stored:

Со	Content of file is shown as table format															
	Name	Fin	Fs	Vin	ENOB	SINAD_C	SNR_C	SNR_FS	SFDR_C	SFDR_FS	THD	H2	НЗ	H4	H5	H6
		(MHz)	(MHz)	(dBFS)	-	(dBc)	(dBc)	(dBFS)	(dBc)	(dBFS)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)	(dBc)
	ADC1610S test															
	ADC0	5.00	122.88	-0.96	11.28	69.79	69.67	70.75	84.62	85.58	-85.27	-104.62	-100.12	-103.67	-86.57	-112.7

Table 7. Dynamic results as stored in a text file

Note that while acquisition is running, any other action (ADC SPI programming, quit or refresh) is not possible. Stop acquisition first before proceeding to any other task.

3.3.5.1 FFT spectrum

The first graph to be displayed is the FFT spectrum of the digital pattern acquired:



Press the "Autoscale" button to display the whole content.

3.3.5.2 Reorganized signal

The reorganized signal displays the reconstructed sine wave from coherency calculation corresponding to 1 period of the input signal:

copyright NXP semiconductors 2010	REFRESH Stop acquisition before any action.	NXP HSDC ADC acquisition	software	Stop acquisitio	QUIT on before any action.
Device delacted: ADC(5105125 Resolution 16 Sumpling rate Fs (max. 125 Mips) 122.48 Input Respansive Fin (max. 600 MHs) 5	ADC - Functional Registers ACQUISITION Fin and Fs are: In one ocherent Store to file: Registers Fixed Is: Fr coherent (H Fin and Fs are: Store to file: Registers Fixed Is: Fr coherent (H Fin and Fs are: Fin and Fs	ADC - Load Registers Tools Acquist	on Info	ax. 255 trials	:)
Number of samples	STOP Display FFT Spectrum Reorganized Signal Unrecom	ADC0	de l		
Carpor			Item	ADC	Unit
OWDS	65000 -		ADC Digitized signal		
100005	£0000 -		Frequency	5.000	MHz
			Amplitude	-0.952	dBFS
	55000 -		ADC AC parameters		
	50000 -		SNR	70.04	dBc
			SNR	70.99	dBFS
	+5000 -		SINAD	69.93	dBc
INITIALIZATION	40000 -		ENOB	11.32	bits
Output las	2 35000 -	/	SFDR	87.65	dBc
Outputing			SFDR	88.61	dBFS
HSDC-EXTMOD found! Device ADC1610S125 found!	< 3000 -	\backslash	THD	-86.24	dBc
HSDC-EXTMOD is initialized	25000 -	\land	ADC Harmonics		
	20000 -	//	H2	-104.958	dBc
	15000 -		H3	-88.605	dBc
			H4	-105.529	dBc
	10000 -		HS	-93.307	dBc
	5000 -		H6	-114.819	dBc
	0-		ADC Code excursion		
	0 10000 20000 3000	0 40000 50000 60000 700	00 Min	3404	codes
		Code	Max	62168	codes
SAVE SETTINGS		*1./0728 v	Mean	32782.96	codes
			21		0.0000000
RESTORE SETTINGS					
	Street				

Press the "Autoscale" button to display the whole content.

3.3.5.3 Unreconstructed signal

The unreconstructed signal displays the unreconstructed sine wave corresponding to the whole number of period being acquired following the coherency rule:

	Stop acquisition before any action.		DC acquisition softw	are	Stop acquisit	Q ion before an	UIT iy action.
evice detected: ADC 16 105 125 solution 16 impling rate Fs (max, 125 Msps) 22.88 put frequency: Fin (max, 600 MHz) 5	ADC - Functional Registers ADC - Rea ADC - Guidition Fin and Fa are: Cocherent In on coherent Store to file Line Header Results file &	d Registers ADC - Load Register coharent (Hc) Select winds 22.866-92E+6 No win	Tools Acquisition Ir	fo	ax. 255 trial	s)	
umber of samples 65536 🗸	STOP FFT Spectrum Reorganized Signal	Display ADC0	gram Autoscale	Item	ADC	Unit	
⊙ CMOS	65000			ADC Digitized signal	ADC	Unic	
OLVDS	85000			Frequency	5.000	MHz	
	60000			Amplitude	-0.954	dBFS	
	55000 -			ADC AC parameters			
	50000 -			SNR	69.86	dBc	
	45000 -			SNR	70.82	dBFS	
				SINAD	69.76	dBc	
	40000 -			ENOB	11.30	bits	
utput log	골 35000 -			SFDR	85.99	dBc	
ISDC-EXTMOD found!	Ê 30000 -			SFDR	86.94	dBFS	
Device ADC1610S125 found!	25000 -			THD	-86.16	dBc	
HSDC-EXTMOD is initialized!	20000			ADC Harmonics		10	
	2000 -			12	-102.821	dBC	
	15000			113	-102 145	dRc	
	10000			HS	-102.145	dBc	
	5000 -			H6	-113,985	dBc	
		و الای کا		ADC Code excursion			
	0 10000 200	00 30000 40000 500	10 60000 70000	Min	3404	codes	
		Code		Max	62163	codes	
SAVE SETTINGS			LITE M	Mean	32781.79	codes	
		7		A presenter and			
DECEMPT OF STREET, OF ST							

Press the "Autoscale" button to display the whole content.

Use the zoom tool to observe in more details all the captured data.

3.3.5.4 Histogram

The histogram graph shows the distribution of output codes. This graph shows which code is present and if there is any missing code in the conversion range:

pyright NXP semiconductors 2010	REFRESH NXP HSDC ADC acquisition software Stop acquisition before any action.	:	Stop acquisiti	on before a	UIT ny action.
Actis Los I25 C Actis Los I25 C seculution 16 ampling rate Fs (max. 125 Mps) 122.08 mpdt Reguency Fin (max. 600 MHz) 5	ADC - Functional Registers ADC - Read Registers ADC - Load Registers Tools Acquisition Info Acquisition Fin and F3 are: Fixed is: F5 coherent (Hz) Select window type: Coherent Fin Coherent Fin Select window Type: No window Type: No window Type: Readle FFI Select window type: No window Type: Readle FFI Readle FFI	Faveraging 10 (ma	x. 255 triał	5)	
Number of samples 65536 🗢 Data stream	STOP Display ADC0 FFT Spectrum Reorganized Signal Unreconstructed Signal Histogram Autoscale	Item	ADC	Unit	
⊙ CMOS	45	ADC Digitized signal		and in case of	
OLVDS		Frequency	5.000	MHz	
	40-	Amplitude	-0.954	dBFS	
		ADC AC parameters			
	35 -	SNR	69.94	dBc	
		SNR	70.90	dBFS	
INITIALIZATION	30 -	SINAD	69.84	dBc	
		ENOB	11.31	bits	
Dutput log		SFDR	86.27	dBc	
HSDC-EXTMOD found!	<u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u><u></u></u>	SFDR	87.23	dBFS	
Device ADC1610S125 found!	0 **	THD	-86.07	dBc	
HSDC-EXTMOD is initialized!	15 -	ADL Harmonics	100.040	10-	
		12	-102.045 OF 244	dbc	
		по На	-95.244	dBc	
		нс	-88.033	dBc	
		H6	-113 884	dBc	
		ADE Code excursion	110/001	doc	
	0 10000 20000 30000 40000 50000 60000 70000	Min	3407	rodes	
	Code	Max	62155	codes	
SAVE SETTINGS	1.(四) 10	Mean	32781.83	codes	

Press the "Autoscale" button to display the whole content.

The table shows the range of output codes.

3.3.6 Info page

copyright NKP semiconductors 2010	NXP HSDC ADC acquisition software	
Device detected; ACCUM 5123 C Resolution 12240 12240 12240 1	ADC - Load Register Tools Acquisition Trife) +3.39 CLK +3.39 VID ⑤ m rising edge. PLL UN03001 looked ⑥	

This page will give practical information related to software and hardware settings:

The information visible on this page is:

- board serial number ①;
- HSDC software release number 2;
- HSDC-EXTMOD dll version 3;
- HSDC-EXTMOD vhdl version @;
- HSDC-EXTMOD supply status (5);
- HSDC-EXTMOD clock capability and status version 6;
- HSDC-EXTMOD memory capability .

4. Appendix A.1: coherency calculation

The coherency relies on the fact that clock and analog input signal are synchronized and the first and last samples being captured are adjoining samples: it ensures a continuous digitized time process for the FFT processing.

To achieve this, one has to

 $\frac{F_{in}}{F_s} = \frac{M}{N}$ follow the equation:

Where M is an odd integer equal to the number of periods being acquired and N the number of samples acquired.

With Fin, Fs and N known, M has to be chosen such that it follows the equation above. To do this iterative calculation, one has to decide whether Fin or Fs is fixed.

To illustrate this process, let's consider our current example with Fin = 5 MHz, Fs = 122.88Msps and N = 65536 samples acquired:

- if Fin is fixed, this leads to M = 2667 periods of input signal to be acquired and a real sampling frequency to be Fs = 122.864642 MHz;
- If Fs is fixed, this leads to M = 2667 periods of input signal to be acquired and a real input frequency to be Fin = 5.000625 MHz.

Those values needs to be programmed in the signal generator and clock generator before capture is done, otherwise the FFT calculation will lead to a non-coherent result as shown below:



The numbers given for SNR, SFDR are completely wrong if coherency is not respected.

5. Notes

For any question, feel free to contact us at the following e-mail <u>dataconverter-support@nxp.com</u>.

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