78M6610+PSU

Energy Measurement Processor for Single-Phase Power-Supply Units

DESCRIPTION

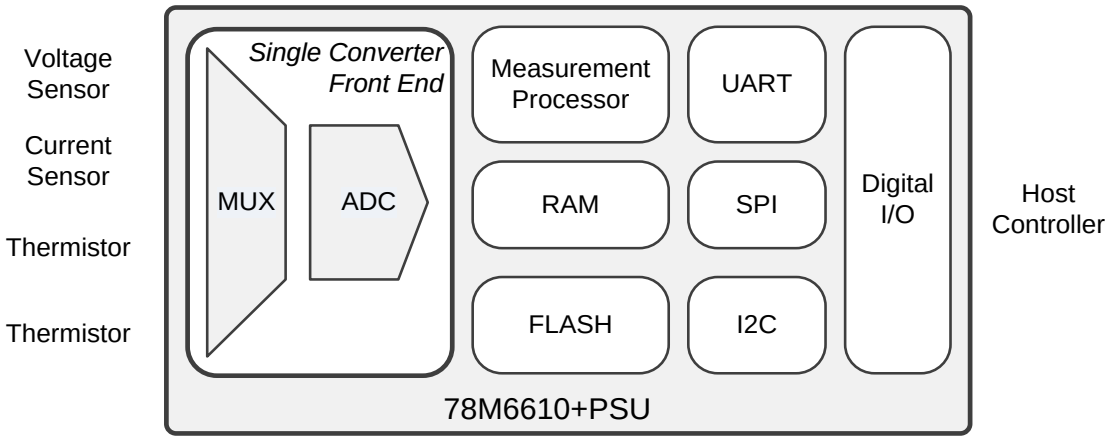
The 78M6610+PSU is a single-core energy measurement processor for single-phase power supplies. It is designed specifically for real-time monitoring at the input of AC/DC power converters used in data centers and IT server rooms. It is available in either a 24-pin QFN or 16-pin TSSOP package for optimal space savings.

The 78M6610+PSU provides four analog inputs (two differential and two single ended) for interfacing to voltage, current, and two optional temperature sensors. Scaled voltages from the sensors are fed to the single converter front-end utilizing a high-resolution delta-sigma converter. An embedded 24-bit energy measurement processor (EMP) and firmware performs all the necessary computation, compensation, and data formatting for accurate, real-time reporting to the host. With integrated flash memory, the 78M6610+PSU is a completely autonomous solution capable of storing nonvolatile data such as calibration coefficients and input configuration settings.

The 78M6610+PSU is designed to interface to the host processor via the UART interface. Alternatively, SPI or I^2C may also be used. Supported current sensors include Current Transformers (CT) and Resistive Shunts.

FEATURES

- Delta-sigma ADC with precision voltage reference
- Internal or external oscillator timing reference
- SPI, I^2C, or UART interface options with configurable I/O pins for alarm signaling, address pins, or user control
- 24-bit energy measurement processor (EMP) with integrated firmware and flash memory provides the user with:
  - o True RMS calculations for current, voltage, line frequency, real power, reactive power, apparent power, and power factor
  - o Compensation for ambient temperature, sensor tolerances, offsets, and EMI filter components
  - o Real-time data accumulation based on an integer number of AC cycles
  - o Quick calibration routines for manufacturability
  - o Up to two voltage inputs for optional connection to thermal sensors



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1 On-Chip Resources Overview

The 78M6610+PSU integrates all the functional hardware blocks required to embed solid-state AC power and energy measurement. Included on the device are:

- Accurate oscillator and clock management logic
- Power-on reset, watchdog timer, and reset circuitry
- High-accuracy Analog Front End (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor (EMP)
- RAM and flash memory
- Communication interfaces
- Multipurpose Digital I/O

Figure 1 shows a block diagram of the device. A detailed description of various functional blocks follows.

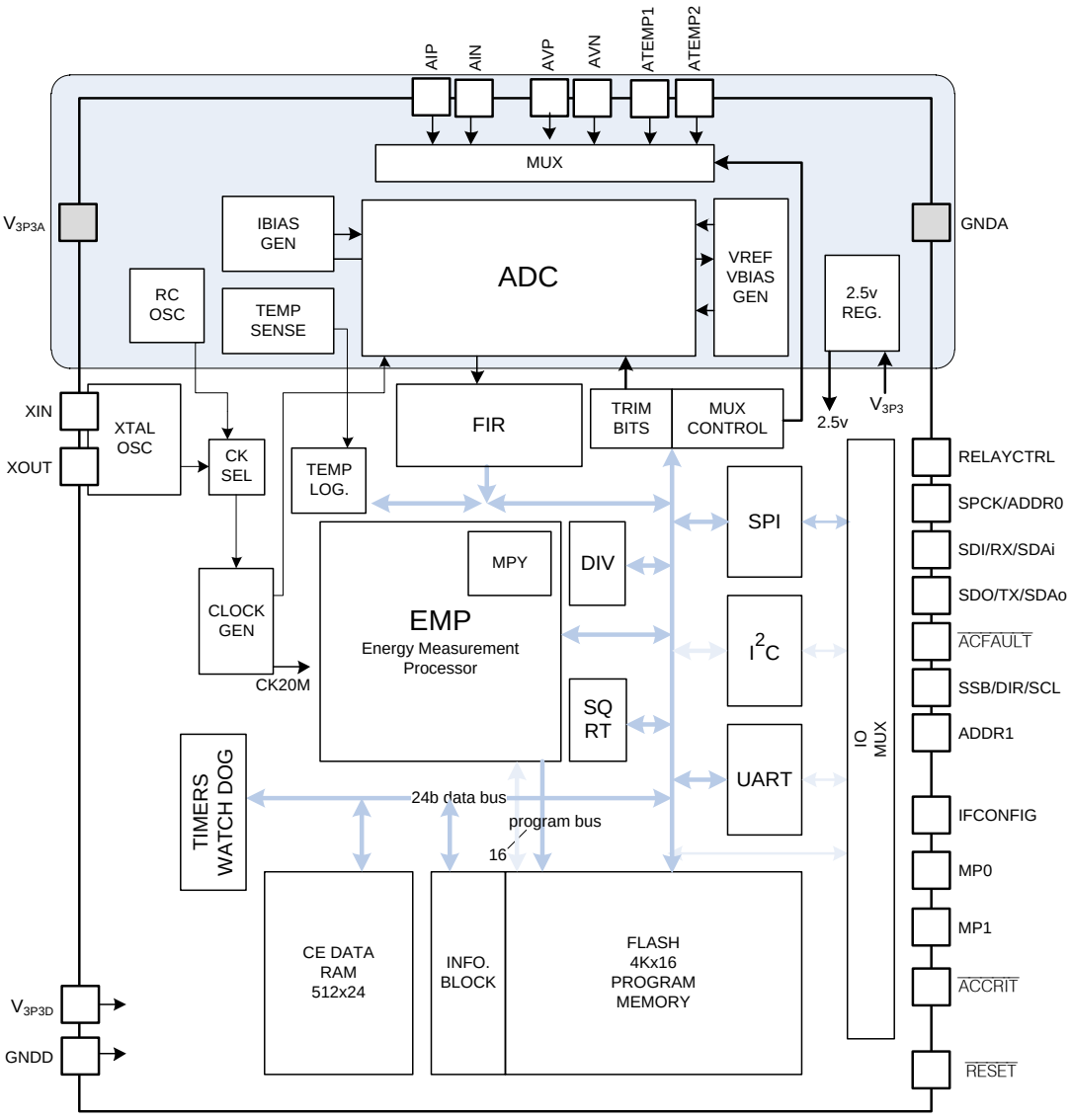


Figure 1: IC Functional Block Diagram

1.1 Clock Management

The 78M6610+PSU can be clocked by either the trimmed internal RC oscillator or by oscillator circuitry that relies on an external crystal. The 78M6610+PSU hardware automatically handles the clock sources logic and distributes the clock to the rest of the device.

Upon reset or power-on, the 78M6610+PSU will automatically select the external clock, if available, after 1024 clock cycles of the internal oscillator, allowing the external crystal adequate time to start-up. After power-on or during run-time, the 78M6610+PSU will automatically switch to the internal oscillator in the event of a failure with the external oscillator (or crystal not mounted). This condition is also monitored by the processor and available to the user in the ALARMS register.

The internal RC oscillator is trimmed and temperature compensated. It provides an accurate clock source, however for applications requiring highest line frequency accuracy, the use of an external crystal is recommended (only available in the 24-pin QFN package).

The 78M6610+PSU external clock circuitry requires a 20.000 MHz crystal. The circuitry includes two 18pF ceramic capacitors. Figure 2 shows the typical connection of the external crystal. This oscillator is self biasing and therefore an external resistor should NOT be connected across the crystal.

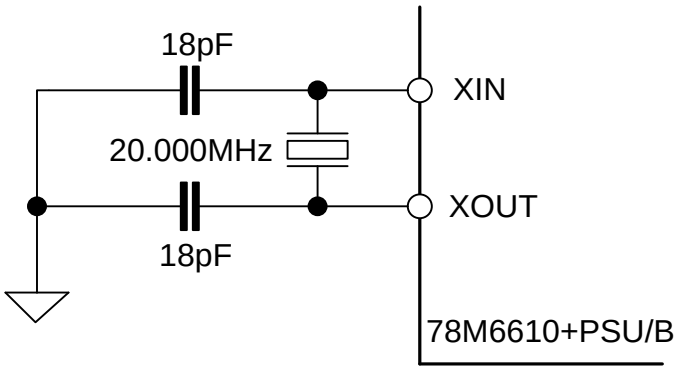


Figure 2: XTAL Connection

Alternatively, an external clock signal can be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

If the external crystal is not utilized (not mounted), the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

1.2 Power-On Reset, WD Timer, and Reset Circuitry

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

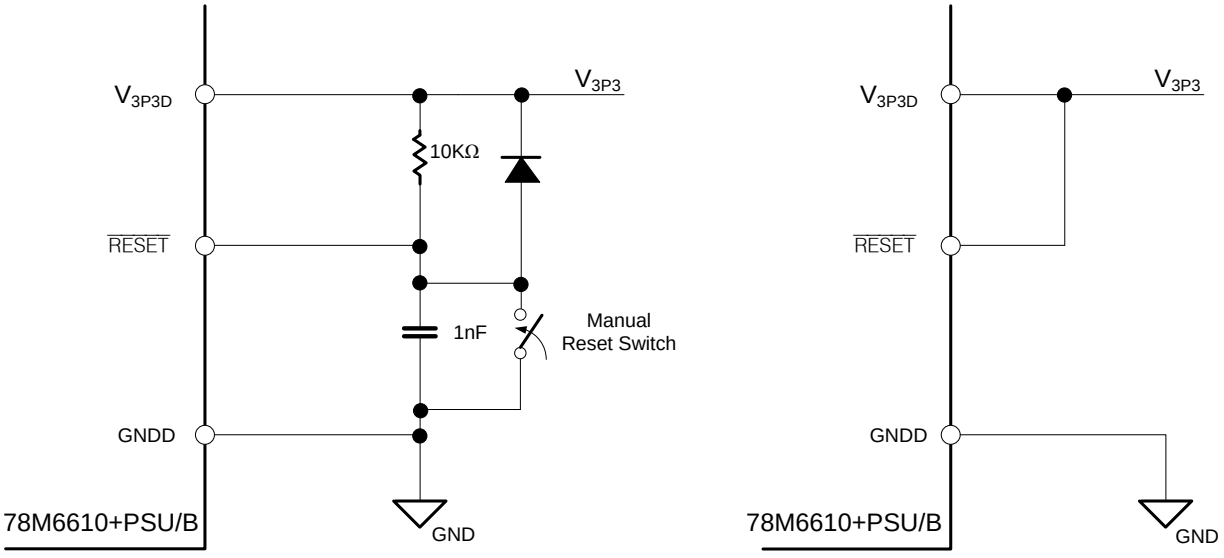
External Reset Pin (**$\overline{\text{RESET}}$** Pin)

The 24-pin QFN package provides a dedicated reset (**$\overline{\text{RESET}}$**) pin. In addition to the internal sources, a reset can be forced by applying a low level to the **$\overline{\text{RESET}}$** pin.

If the **$\overline{\text{RESET}}$** pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until **$\overline{\text{RESET}}$** has been held low for at least 1 µs.

Once initiated, the reset mode persists until the **$\overline{\text{RESET}}$** is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

If not used, the **$\overline{\text{RESET}}$** pin can be connected either directly or through a pull-up resistor to V_{3P3D} supply. A simple connection diagram is shown in Figure 3.



a) $\overline{\text{RESET}}$ External Connection Example

b) Unused $\overline{\text{RESET}}$ Connection Example

Figure 3: $\overline{\text{RESET}}$ Pin Connections

1.3 Analog Front-End and Conversion

The Analog Front-End (AFE) of the 78M6610+PSU includes an input multiplexer, delta-sigma A/D converter, bias current references, voltage references, temperature sensor, and several voltage fault comparators.

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then processed through an FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to differential voltage input pins. The full-scale signal level that can be applied to the voltage input pins is V_{3P3A} ±250 mV. Considering a sinusoidal waveform, the maximum RMS voltage is:

$$\mathrm{VrmsMAX} = \frac{250mV}{\sqrt{2}} = 176.78\mathrm{mV}$$

Although the voltage input is differential, a common-mode voltage of less than ±25 mV is recommended in order to utilize the available dynamic range.

Temperature Inputs

ATEMP1 and ATEMP2 are single-ended inputs that allow temperature measurement through an external sensing element (NTC, RTD etc.). The temperature measurement is generally used to monitor heat-sink or exhaust air operating conditions. TEMP2 is only available with the 24-pin package option.

1.4 24-Bit Energy Measurement Processor (EMP)

The 78M6610+PSU integrates a dedicated 24-bit signal processor that performs all the digital signal processing necessary for energy measurement, alarm generation, calibration, compensation, etc. Refer to Section 2 for a description of functionality and operations.

1.5 Flash and RAM

The 78M6610+PSU includes 8KB of on-chip flash memory. The flash memory primarily contains program code, but also stores coefficients, calibration data, and configuration settings. The 78M6610+PSU includes 1.5KB of on-chip RAM which contains the values of input and output registers and is utilized by the FW for its operations.

1.6 Communication Peripherals

The 78M6610+PSU includes three communication interface options: UART, SPI, and I^2C.

Since the I/O pins are shared, only one mode is supported at a time. Two pins are sampled at power-on or reset to determine which interface will be active.

1.7 Multi-purpose Digital I/O Pins

The MP0 and MP1 input/output pins are not currently used. The pins have an internal pull-up and can be left floating.

1.8 Alarm Pins (ACFAULT, ACCRIT)

Alarm pins are available to signal an alarm condition has been reached. Table 1 shows the available alarm pins and the intended usage. The alarm thresholds and conditions are programmable through dedicated registers. The status of each individual alarm is accessible through a status register.

Table 1: Alarm Pins Functional Description

ACFAULT	Non critical warning updated once per accumulation interval.
ACCRIT	Critical condition detected; AC Dropout, or SAG (see Section 2.5).

The alarm pins are open drain and active low (0=alarm); these pin needs to be pulled-up and can be wired-or.

2 Functional Description and Operation

This section describes the 78M6610+PSU functionality. It includes measurements and relevant calculations, alarms, auxiliary functions such as calibrations, zero-crossing, relay control, etc.

A set of input (write), output (read) and read/write registers are provided to allow access to calculated data and alarms and to configure the device. The input (write) registers values can be saved into flash memory through a specific command. The values saved into flash memory will be loaded in these registers at reset or power-on as defaults.

2.1 Voltage and Current Inputs Conditioning

The sensor input voltages are digitized using a single integrated second-order delta-sigma A/D converter. The analog front-end includes a temperature sensor whose output is digitized and used for temperature (gain) compensation.

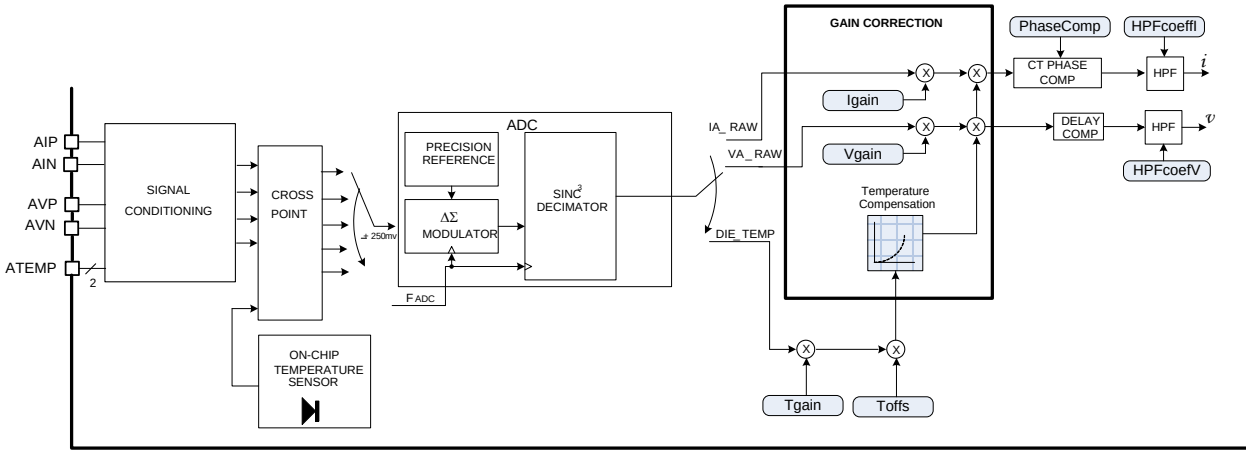


Figure 4: Analog Input Signal Conditioning

2.1.1 High Pass Filters (HPF) and Offset Correction

The high-pass filters (HPF) in Figure 4 and Figure 5 can remove any DC from the signal paths and consequently from power and RMS calculated values. The HPFs work by subtracting the value of the offset register (Voffs, Ioffs) from the corresponding voltage or current input. The offset registers can be set by the user, by an automatic calibration routine or adjusted dynamically by the FW.

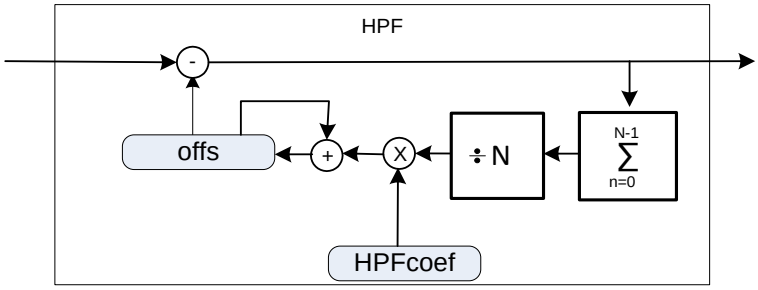


Figure 5: HPF

2.1.2 Phase Compensation

A phase compensation register is provided to compensate phase errors introduced by current transformers (CT) or external filters. The amount of phase shift is set by the PhaseComp register as a fractional number of ADC samples with a total range of +/- 4 ADC samples (roughly +/- 20 degrees for a 60Hz line frequency).

2.2 Current and Voltage RMS Calculations

The 78M6610+PSU provides true RMS measurements for both current and voltage inputs. The RMS is obtained by performing the square sum of the instantaneous samples of voltage and current over a time interval (commonly referred as accumulation time) and then performing a square root of the result after dividing by the number of samples in the time interval.

$$VRMS = \sqrt[2]{\frac{\sum_{n=0}^{N-1} Vn^2}{N}} \qquad IRMS = \sqrt[2]{\frac{\sum_{n=0}^{N-1} In^2}{N}}$$

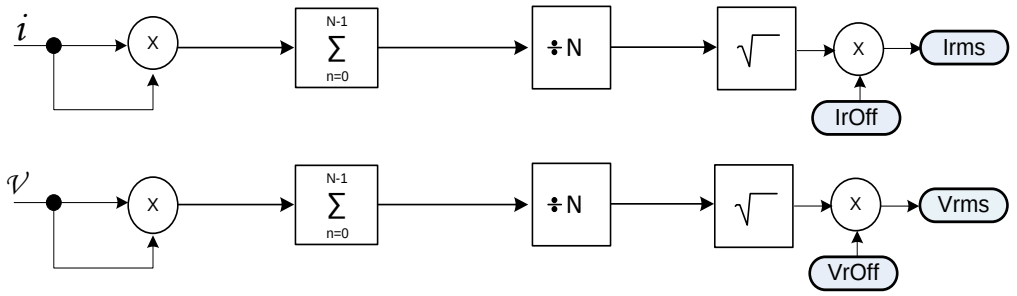


Figure 6: RMS Calculations

2.3 Power Calculations and Power Factor

The 78M6610+PSU computes the active, reactive, and apparent power. In addition, the 78M6610+PSU computes the fundamental power, determined only by the fundamental components of the voltage and current and the harmonic power, determined by the harmonic components of the voltage and current.

2.3.1 Active Power Calculation

Active power is calculated as the product of the voltage and current waveforms. The resulting waveform is the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. The instantaneous power is then averaged over N samples (accumulation time) for the computation of the active power available at register WATT.

$$WATT = \frac{\sum_{n=1}^{N-1} v_n \, i_n}{N}$$

2.3.2 Apparent Power

The apparent power (S) is the product of RMS voltage (V_{RMS}) and current (I_{RMS}). The apparent power results, also referred as Volt-Amps, are available at the register VA.

$$S = I_{RMS} * V_{RMS}$$

2.3.3 Power Factor

The power factor (PF) is calculated as active power (WATT) divided by the apparent power (S). The sign of the power factor is determined by the active power sign.

$$PF = \frac{\text{WATT}}{\text{S}}$$

2.3.4 Reactive Power

The reactive power is calculated as multiplication of instantaneous samples of current (i) and the instantaneous quadrature voltage (Vq). The quadrature voltage is obtained through a 90° phase shift (quadrature delay) of the voltage samples. The samples are then averaged over the accumulation time interval and updated in the VAR register.

$$Q = \sqrt{\sum_{n=0}^{N-1} i_n \times vq_n}$$

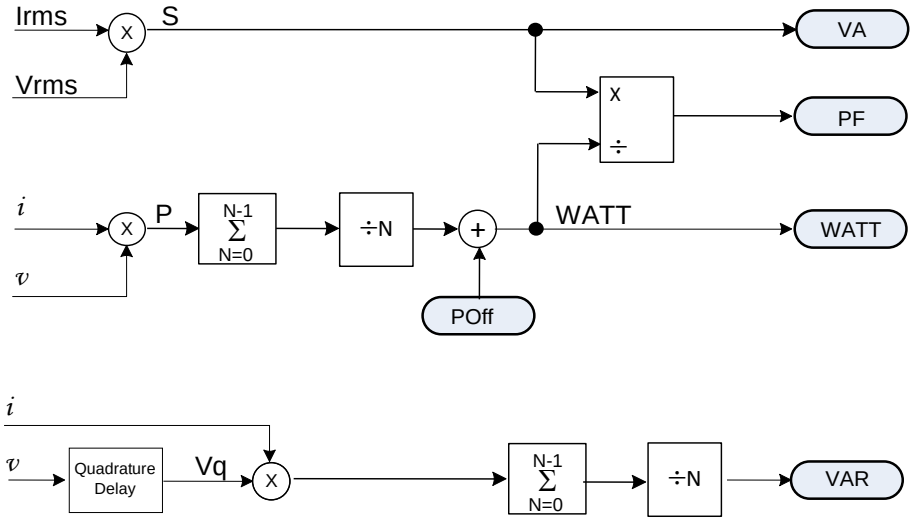


Figure 7: Power (Active, Reactive, and Apparent) and Power Factor Calculation

2.4 Fundamental and Harmonics Calculations

Fundamental and Harmonics

The 78M6610+PSU provides measurements on fundamental and total harmonic of voltage, current, and power (active, reactive, and apparent).

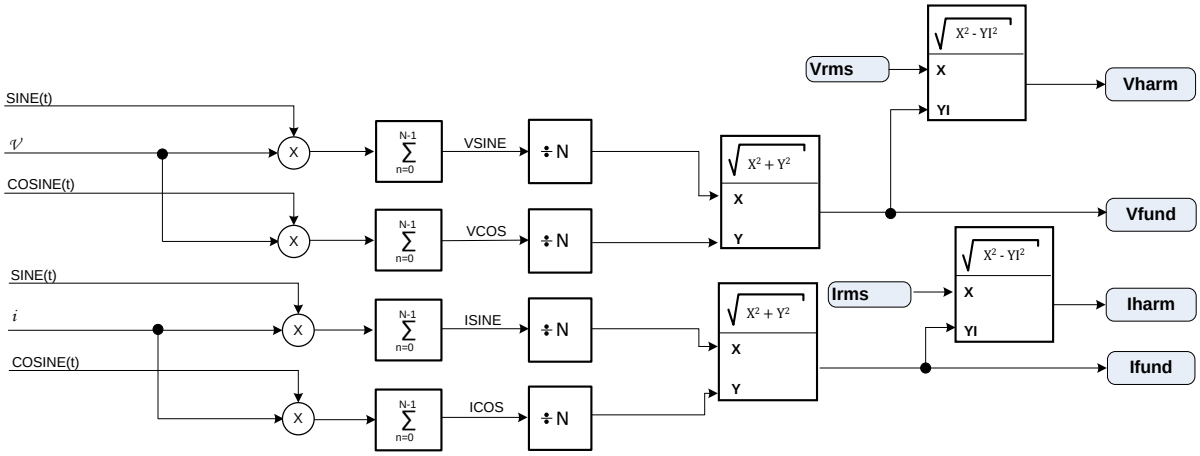


Figure 8: Voltage and Current Fundamental and Harmonic Calculations

Fundamental and Harmonic Selection

The 78M6610+PSU allows extraction and calculation of a single selected harmonic. By default, the fundamental (first harmonic) is selected for voltage, current, active, reactive real and apparent power calculations. The HARM register is used to select the single harmonic to extract.

By setting the value in the HARM register to a higher harmonic, the fundamental result registers will contain amplitudes of the selected harmonic. In this case the harmonic result register will contain the balance of the voltage, current, or power.

2.5 Accumulation Interval

The accumulation interval mode is configurable by the user through the Accum and AccumCyc registers and the status of the line lock bit.

The ACCUM register contains an unsigned integer values representing the accumulation interval (time) expressed in number of high-rate samples.

The accumulation interval can also be locked to the incoming line voltage cycles. The LINELOCK bit in the command register allows the accumulation interval to be determined by the ACCUM register or to be locked to the line cycle.

Once locked to the line cycle the accumulation interval will end after the first low-to-high zero crossing of the Reference AC Voltage (see Zero-Crossing Detection) input occurs once the Minimum Accumulation time has elapsed. The Actual Accumulation Interval will span an integer number of line cycles. When LINELOCK is not set, the Accumulation Interval will equal the value set by the ACCUM register.

The effective sample rate for each input of the 78M6610+PSU is 4KS/s. The DIVISOR register reports the actual number of samples within any given accumulation interval.

It is also possible to set the accumulation interval based on a number of AC Voltage line cycles. If the Line Lock (LL) Command register bit is set and AccumCyc register is non-zero then the device will calculate, on every frequency update, a new Accum value based upon the line frequency. The formula is as follows:

$$Accum = \frac{\text{SampleRate}}{\text{Line Frequency}} - 18$$

The computed Accum value locks the accumulation interval to the number of AC line voltage cycles, specified by the AccumCyc line cycles regardless of the system frequency.

2.6 Zero-Crossing Detection

The 78M6610+PSU includes a zero-crossing detection feature on both AC input channels. The zero-crossing detection allows measurements to be synchronized to the frequency of the incoming waveforms. The time delay of the zero-crossing output versus the effective zero crossing is approximately 500 µs.

2.7 Alarms

The 78M6610+PSU includes a set of user-configurable alarms. Most alarms have a corresponding register to store the threshold above which (in the case of “max” limits), or below which (in the case of “min” limits) an alarm condition is generated. Such a condition does not necessarily cause an alarm. The condition must exist for the duration of the associated hold-off time.

If the alarm condition exceeds the hold-off time, an alarm event is generated and reported in the corresponding bit of the alarm register. The corresponding event counter is also incremented.

The alarm bit will continue to be set as long as the alarm condition persists, even if the user clears it by accessing the AlarmReset register. However, event counters will only record one event until the next new assertion of the alarm.

The registers AlarmMask1 and AlarmMask2 allow the user to select which alarm will be used to drive the corresponding alarm pins (AlarmMask1 controls $\overline{\text{ACFAULT}}$ pin while AlarmMask2 controls $\overline{\text{ACCRIT}}$ pin). For example, to select OverCurrent and Vsurge to drive the $\overline{\text{ACFAULT}}$ pin, AlarmMask1 should be set to 0x000440.

The AlarmSet register allows forcing a particular alarm in the alarm register. This function is mainly intended for relay control and system test purposes.

The AlarmReset register allows clearing a particular alarm in the alarm register.

The AlarmSticky register allows the user to select which bits in the alarm register should remain set even after the alarm condition no longer exists. These bits will remain set until reset by the host/user. All other Alarms will be reset at the end of the accumulation interval unless the alarm condition remains.

Exceptions: Relay_On, Zero_Cross, and Data_Ready are not influenced by the value of the AlarmSticky register. By default, all the bits in the AlarmSticky register are set.

2.8 Voltage and Current Min/Max and Peak Tracking

2.8.1 Voltage and Current Min/Max Tracking

The 78M6610+PSU allows recording the lowest and highest voltage and current rms values. These values are stored in the registers Vhi, Vlo, Ihi, and Ilo. To reset these values it is necessary to write to these registers. For example, a value of 0x000000 should be written in the Vhi or Ihi register in order to reset them. Similarly, a value of 0x7FFFFF should be written to the Vlo and Ilo registers in order to reset them.

2.8.2 Voltage and Current Peak Tracking

The 78M6610+PSU allows recording the highest voltage and current measured during an accumulation interval. These values are updated at each accumulation interval and available on the output registers Vpeak and Ipeak, for voltage and current, respectively.

2.9 X+Y Capacitor Current and I/R Voltage Drop Compensation

The 78M6610+PSU location in the power supply AC input stage can be different from design to design. In order to achieve high accuracy, the components preceding the measurement point should be accounted for. For example, current flowing in filter capacitors or the voltage drop across PCB traces (I, Vdrop) should be considered in the measurement as shown in Figure 9.

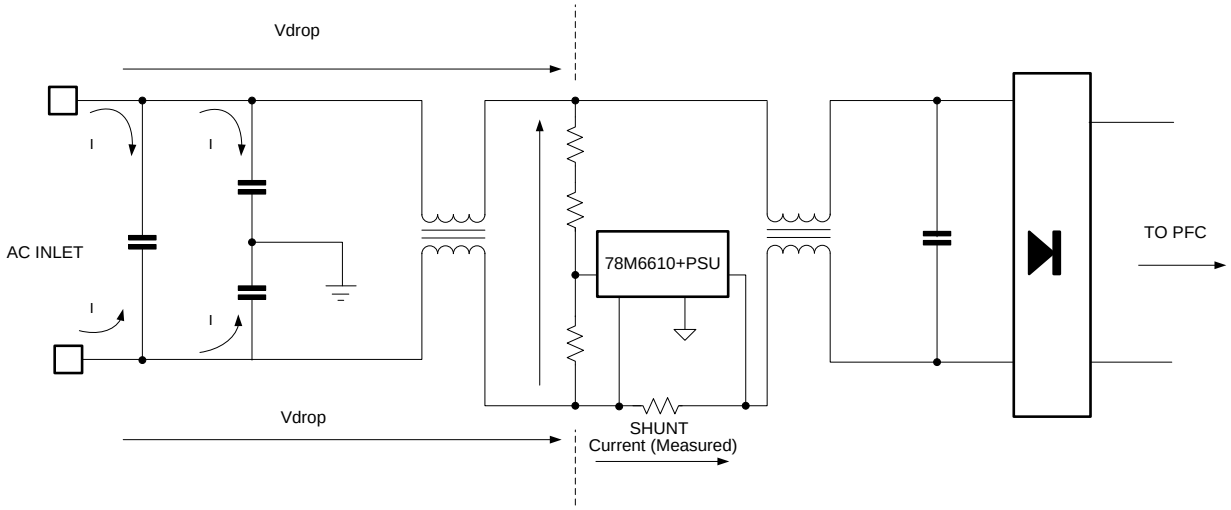


Figure 9: Typical Measurement Location in Power Supplies

2.9.1 X+Y Capacitor Compensation

The 78M6610+PSU, and therefore the measurement point, is usually located between the inlet and the diode bridge. This stage is where the EMI filters are usually located as shown in Figure 9.

In this case the current flowing through the filter (X+Y) capacitors preceding the measurement cannot be measured and is compensated for by the 78M6610+PSU. The current in flowing into these capacitors is at 90° phase respect to the voltage; therefore it has no effect on the power measurement. The effect is prominent in the current reading, in particular at light loads. Compensation is required in order to achieve higher accuracy.

A fixed coefficient value can be set for compensation, however due to the tolerance of the filter capacitors (in the +/-20% range) a calibration routine is included in the firmware. Calibration of the X+Y capacitor coefficient facilitates higher accuracy in the measurement of the current

2.9.2 I/R Voltage Drop Compensation

The PCB traces have a certain resistance that at high loads causes a voltage drop from the inlet to the measurement point. The voltage drop causes an error in the voltage and power measurements. The correction is proportional to the current measured. A coefficient proportional to the input stage resistance is available and tunable by the user. Usually this coefficient is set by the user for a specific hardware and does not require calibration.

2.10 External Temperature Monitor

The ATEMP1 and ATEMP2 inputs are dedicated to the acquisition of an external temperature. These inputs are single ended with a range of +/-250 mV referenced to the 3.3VDC supply (V_{3P3A}). The converted value is multiplied by a user programmable gain and the results are reported in the EXTEMP registers as a voltage drop from V_{3P3}.

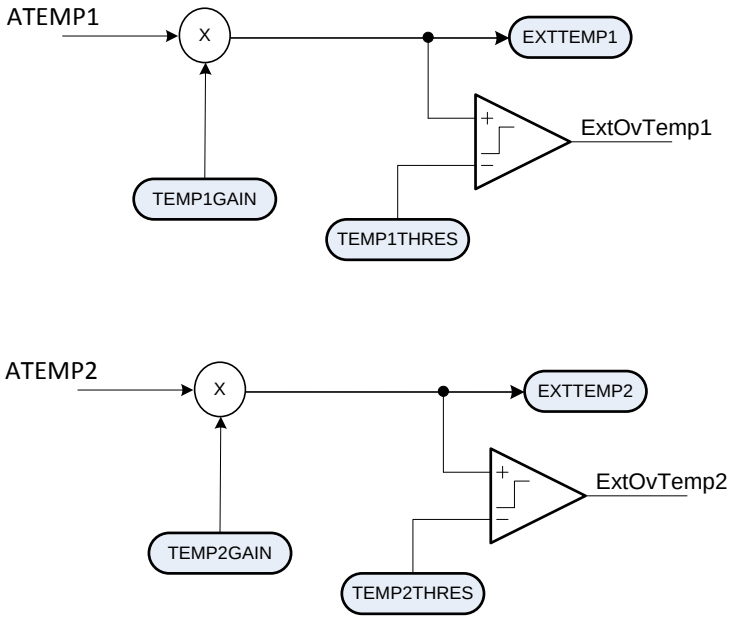


Figure 10: External Temperature Monitor

The output of the multiplier block is also compared with the value contained in a user-programmable register to generate a corresponding alarm once that limit value is exceeded.

2.11 Voltage Sag and Surge Detection

The 78M6610+PSU implements a voltage sag detection function, which can generate an alarm when the line voltage drops below a programmable threshold.

The firmware calculates on a sample-by-sample basis the trailing mean square of the input voltage:

$$V_{MS} = \frac{f_{line}}{2 \times f_{sample}} \times \sum_{n=-int(\frac{f_{sample}}{2 \times f_{line}})}^{0} {v_n}^2$$

At each sample interval the V_{MS} value is compared to a programmable threshold contained in the Vsag register. If V_{MS} falls below the threshold, the firmware sets the Vsag bit in the Alarms register. If Vsag is enabled in the AlarmMask2 register, the $\overline{\text{ACCRIT}}$ pin will also be asserted low. If the Vsag bit is set in the AlarmsSticky register, then Alarms.Vsag will remain set and $\overline{\text{ACCRIT}}$ will remain low until the Vsag alarm is cleared via the AlarmReset register or the 78M6610+PSU is reset. If AlarmsSticky.Vsag is cleared, then Alarms.Vsag will be cleared and $\overline{\text{ACCRIT}}$ set high as soon as the V_{MS} monitor is greater than the programmable threshold.

The sample count for sag detection is automatically adjusted by the firmware to maintain coverage over half of the AC cycle. Sag detection is disabled by default and can be enabled by writing a non-zero value to the VSAG register. If the VSAG register is set to 0, the sag feature is disabled.

The sag detection can be used to monitor or record the quality of the power line or utilize the sag alarm pin to notify external devices (for example a host microprocessor) of a pending power-down. The external device can then enter a power-down mode (for example saving data or recording the event) before a Power outage. Figure 11 shows a typical sag event.

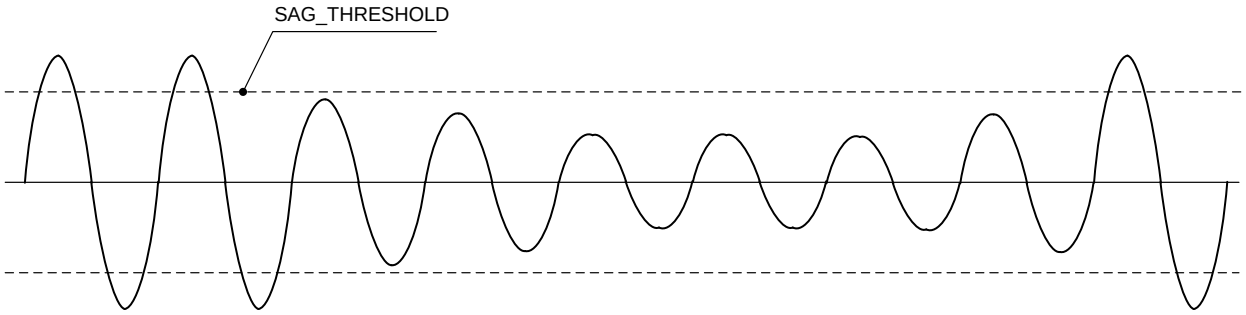


Figure 11: Typical Sag Event

2.12 Relay Control

The firmware includes relay control logic and provides a digital output RELAYCTRL for controlling a relay.

The relay control may operate in either an autonomous mode or in a slave mode. The operating mode is selected by the setting of the AUTORELAY bit in the COMMAND register. A bit in the ALARMS register reports the state of the RELAYCTRL output.

2.12.1 Autonomous Mode

When autonomous relay control mode is enabled, the 78M6610+PSU firmware controls the state of RELAYCTRL output, based upon the input line voltage.

At power on, RELAYCTRL output is inactive. When the RMS voltage is within specified upper and lower turn-on thresholds (RelayOnMin, RelayOnMax) for a specified time (RelayOnTime), RELAYCTRL output will be activated. Should the RMS voltage exceed the specified turn-off thresholds (RelayOffMin, RelayOffMax) for a specified time (RelayOffTime), RELAYCTRL output will be deactivated. The turn-on and turn-off thresholds are specified separately, as are delay times, to provide hysteresis to prevent unwanted switching of the relay due to short-term fluctuations in voltage.

The autonomous mode can be used to automatically control the in-rush current relay as shown in Figure 12.

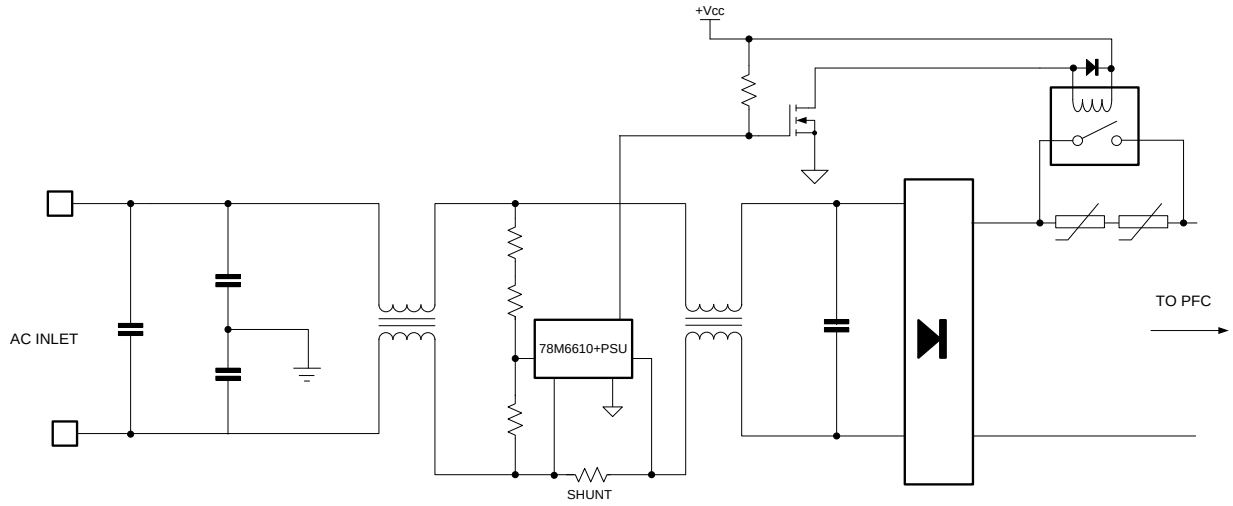


Figure 12: Relay Control for In-rush Current Limitation Circuitry

2.12.2 Slave Mode

When slave mode relay control is selected, the RELAYCTRL output is manually controlled by setting or clearing the RELAY_ON bit in the AlarmSet and AlarmReset registers.

2.12.3 Activation Delay

The relay control logic allows setting a delay time for energizing and de-energizing the relay. The delay time for energizing and de-energizing the relay is relative to the zero crossing of the Voltage as shown in Figure 13.

The time specified in the registers is expressed in the number of high-rate samples.

The default timings are:
Energized delay time (RelayOnDelay) = 0x000000 sample counts
De-Energized delay time (RelayOffDelay) = 0x000000 sample counts

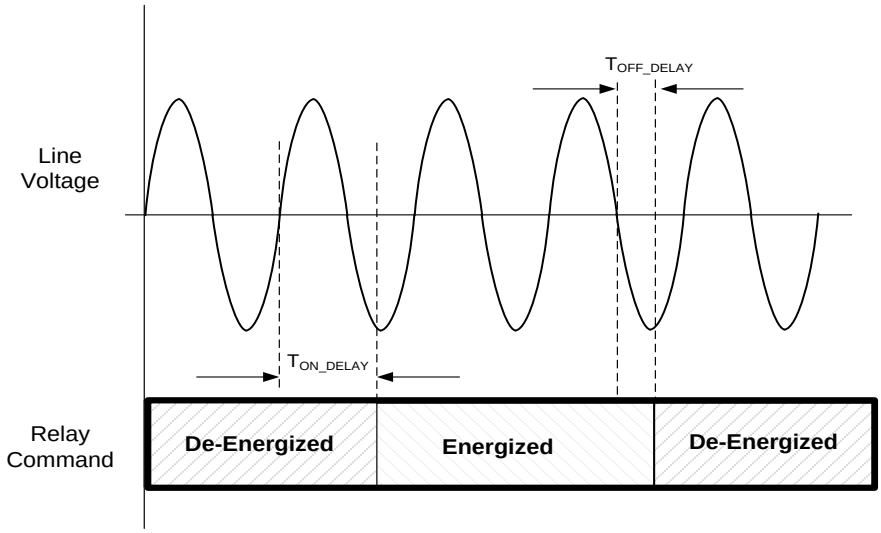


Figure 13: Relay Control

Table 2: Relay Configuration Register and Sequence Delay Register

Function	Register	Default Value	Comments
TON_Delay	RelayOnDelay 0x6b	0	Line Relay Activation Time Delay
TOFF_Delay	RelayOffDelay 0x6c	0	Line Relay De-Activation Time Delay

2.13 On-Chip Calibration Routines

The 78M6610+PSU includes current and voltage and temperature calibration routines. These routines modify gain and offset coefficients. The device also includes routines for the calibration of the X+Y capacitor and R resistance compensation coefficients.

The user can set and start a calibration routine through the Command register. When the calibration process completes, command register bits 23:16 (set to 0xCA to issue a calibration command) are cleared along with bits associated with channels that calibrated successfully. Any channels that failed will have their corresponding bit left set. After completion of the calibration, the new coefficients can be saved into flash memory as defaults by issuing the Access (ACC) Command.

2.13.1 Voltage and Current Gain Calibration

In order to calibrate the voltage and current channels, a stable AC supply must be applied to the channel to be calibrated. The value corresponding to the applied AC supply (usually measured using a power meter) must be entered in the relevant target register (VTarget, ITarget). Figure 15 shows a typical calibration setup.

To start the calibration, the calibration command must be written to the Command register.

Initially, the value of the gain is set to unity for the selected channels. RMS values are then calculated on all inputs and averaged over the number of measurement cycles set by the register CalCyc. The new gain is calculated by dividing the appropriate Target register value by the averaged measured value. The new gain is then written to the select Gain registers unless an error occurred.

On completion, the command bits are cleared in the Command register, leaving only the system setup bits. In case of a failed calibration, the corresponding bit in the command register is left set.
During calibration, the line-lock mode should be set. Once completed, the calibration routines will store the new gain coefficients in the relevant registers. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Access (ACC) Command.

2.13.2 Offset Calibration

The FW provide build in routines for calibration of the offset registers (Ioffs, Voffs).

To calibrate offset, all DC signals should be removed from all inputs although it is possible to do the calibration in the presence of AC signals. In the command, the user also specifies which channel(s) to calibrate. Target registers are not used for Offset calibration.

During the calibration process, each input is accumulated over the entire calibration interval as specified by the CalCycs register. The result is divided by the total number of samples and written to the appropriate offset register if selected in the calibration command. Using the Offset Calibration command will set the HPF coefficients (HPFcoefV, HPFcoefI) to zero thereby fixing the offset registers (Ioffs, Voffs) to their calibrated values. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Access (ACC) Command.

2.13.3 X+Y Capacitor and R Compensation Coefficient Calibration

Most applications use a line input filter to minimize the EM emissions as shown in Figure 15. The current in the filter capacitors (Icap) preceding the 78M6610+PSU cannot be measured. In order to obtain high accuracy of the current measurement it should be compounded in the total current (Irms) calculation.

Fixed compensation coefficient values can the used, knowing the filter capacitors value. However due to the tolerance of the filter capacitors (often ±20%), in order to obtain higher accuracy in the current measurement, it could required to utilize a specific coefficient for each system. The 78M6610+PSU provides a calibration routine for the X+Y capacitor compensation coefficient.

The routine X-Y compensation coefficient calibration, utilizes both measured voltage and frequency and the target current measured using an external power meter as in Figure 15.

To start the command, the user writes the calibration command, setting bits XYR and I, and other needed options such as line-lock. On completion, the XYcomp parameter will be written with an estimate for the bulk capacitance. Once completed, the calibration routines will store the new gain coefficients in the relevant registers. During the calibration process, each input is accumulated over the entire calibration interval as specified by the CalCycs register.

This routine is not recursive; the user may need to re-issue the calibration command until the current reading matches the target current.

After completion of the calibration, in order to save the new coefficients into flash memory as defaults, it is necessary to issue the Access (ACC) Command.

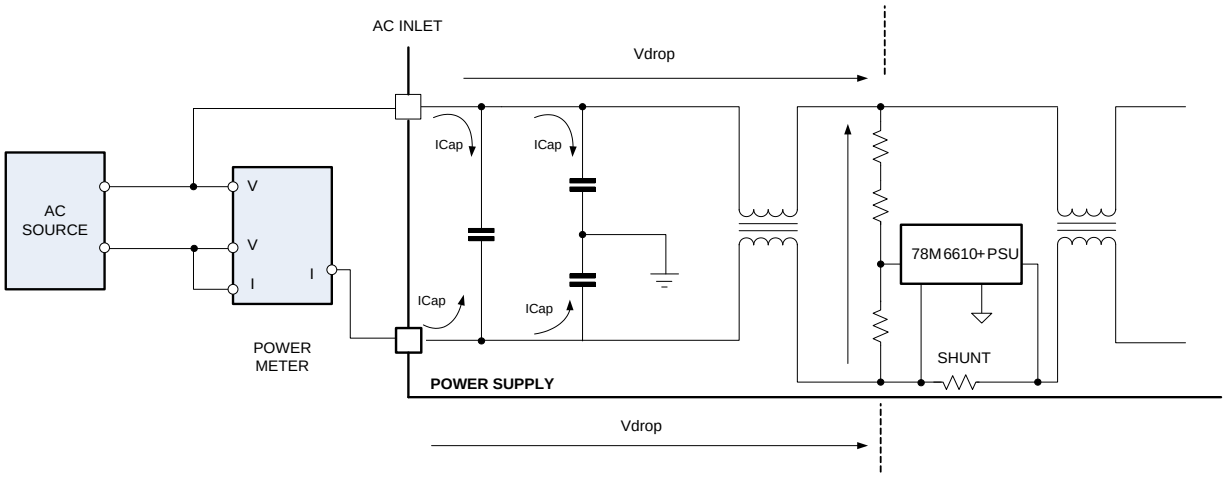


Figure 14: Typical Calibration Setup

2.13.4 On-Chip Temperature Calibration

To calibrate the on-chip temperature sensor, the user must first write only the “T” command bit to a “1” (all other bits 0). This command prevents the firmware from overwriting TempC register. Next the user must write the known chip temperature to TempC. Finally the user writes the Calibration Command to 0xCA0400 (Calibrate Temperature). This will cause the Toffs parameter to be updated with a new offset based on the known temperature supplied by the user. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Access (ACC) Command.

2.13.5 External Temperature Calibration

To calibrate External Temperature, the user must first write only the “X” command bit to a “1” (all other bits 0). This prevents the firmware from overwriting ExtTemp. Next the user must write the known external temperature reading to ExtTemp. Finally the user writes the Calibration Command to 0xCA0100 (Calibrate External Temperature). This will cause the Xgain parameter to be updated with a new gain based on the known external temperature value supplied by the user. In order to save the new coefficients into flash memory as defaults, it is necessary to issue the Access (ACC) Command.

3 Data Access and Configurability

The 78M6610+PSU has several user accessible registers that are used for configuring the device and to access results data. These registers are read (output), write (input), or read/write type, such as the Command register. These registers are accessible through the serial interfaces available on-chip (UART, SPI, and I^2C).

Warning

Writing to reserved registers or to unspecified memory locations could result in malfunctions or unexpected results.

Note

The documented address locations apply to the UART interface. For SPI or I^2C addressing, one must divide the address by 3.

3.1 Register Descriptions

Data Types

The input and output registers have different data types, depending on their assignment and functions. Table 3 shows the different data types.

The notation used indicates whether the number is signed, unsigned, or bit-mapped and the location of the binary point.

- U Indicates an unsigned value.
- S Indicates a signed value.
- . If present, indicates a fixed point number
- nn If to the right of the decimal, indicates the number of bits to the right of the binary point. If no decimal is present, indicates the total bits in the number.

Example: S.21

Bit Position											
23	22	21	.	20	19	18	17	…	2	1	0
$S(-2^2)$	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}	…	2^{-19}	2^{-20}	2^{-21}

Table 3: Data Type Description

Data Type	Description
UINT24	A 24-bit unsigned integer having a range of 0 to 16777215. Typically used for counters
INT24	A 24-bit signed integer with a range of -8388608 to +8388607.
USI24	A 24-bit unsigned scaled integer (scaled by the user).
SSI24	A 24-bit signed scaled integer (scaled by the user).
U.24	A 24-bit unsigned fixed-point value with the binary point to the left of bit 23 with a range of 0 to $1-2^{-24}$.
U.23	A 24-bit unsigned fixed-point number with the binary point to the left of bit 22 and with a range of 0 to $1-2^{-23}$.
U.22	A 24-bit unsigned fixed-point number with the binary point to the left of bit 21 and with a range of 0 to $2-2^{-22}$.
U.21	A 24-bit unsigned fixed point number with the binary point to the left of bit 20 and with a range of 0 to $4-2^{21}$.
S.23	A 24-bit signed fixed point number with the binary point to the left of bit 22 and with a range of -1.0 to $1-2^{-23}$.
S.21	A 24-bit signed fixed-point number with a binary point to the left of bit 20 and with a range of -4.0 to $4-2^{-21.}$
S.16	A 24-bit signed fixed-point number with a binary point to the left of bit 16 and with a range of -128 to +128
Boolean (B24)	A variable containing 24 independent single-bit values.

3.2 Scaling Registers (Iscale, Vscale, Pscale, Tscale, Fscale)

The scaling registers can be used to set the full-scale values and choosing the resolution of related parameters and results.

For voltage and current inputs, full scale is defined as +/-250 mV (DC or Peak). The voltage input is usually scaled down from the AC inlet using a sensing element: resistor divider, voltage transformer, etc.

The current input is connected to current sensing element, generally a low value resistive shunt or current transformer (CT).

The Iscale and Vscale parameters need to be set in order to match the full scale range of the current and voltage inputs with the full scale range of the sensor.

Examples

Voltage: A voltage divider produces an output of 250 mV (peak) with 230 V (peak) applied at its input. A resolution of 1 mV is needed. In this case, the value of VSCALE register should be:

VSCALE = 230 * 1000 = 230000

Current: A current shunt produces a voltage drop of 250 mV (peak) at 30 A (peak). A resolution of 1 mA is needed. In this case the value of ISCALE register should be:

ISCALE = 30 * 1000 = 30000

Power: To set the power scaling register PSCALE it is necessary to multiply the full-scale voltage by the full-scale current and by the desired resolution. For 1 mW resolution:

PSCALE: 230 volts x 30 amps x 1000 = 6900000 mw. The value of Pscale register should be set to 6900000.

The scaling registers for Line Frequency, Power Factor, and Temperature do not set full scale values. They only set resolution. For example, setting Tscale to 1000 the value of the temperature is represented in 1/1000 of Degree Celsius. For example, by setting the Tscale register to 1000, a temperature of 27°C is reported as 27000 in the Temperature register.

> **Note**
>
> **All 78M6610+PSU registers are 24 bits and most are signed. The largest signed integer is +/- 8388608. In case of larger numbers, a lower resolution must be chosen. For example, 10 mW versus 1 mW is case of PSCALE register.**

Table 4: Registers with Scalable Values

Scaling Register	Registers Affected by Scaling
Iscale	Irms Ifund Iharm Ihi Ilo Ipeak Imax Itarget
Vscale	Vrms Vfund Vharm Vhi Vlo Vpeak Vsurge Vsag Vdrop Vmin Vmax Vtarget RelayOnMin RelayOnMax RelayOffMin RelayOffMax
Pscale	Power VA VAR Paverage Pfund Pharm Qfund Qharm Pmax
PFscale	PF
Tscale	Temperature Tmin Tmax Xtemperature Xmin Xmax
Fscale	Frequency Fmin Fmax

3.3 Output Registers

The output registers provide access to the measurement results. Unless otherwise specified, these registers are read-only. Divide the address by 3 for I^2C or SPI access.

Table 5: Output Registers

Address (Hex)	Variable Name	Data Type	Description
0x00	Command	B24	Command Register (see Command Register Section)
0x03	FW version	UINT24	Firmware release date in hex format (0x00YMDD)
0x12	Temperature	S.16	Chip Temperature (-128°C to +128°C, binary point to left of bit 16)
0x15	VA	SSI24	Apparent Power (LSB weight determined by Pscale)
0x18	VAR	SSI24	Reactive Power (LSB weight determined by Pscale)
0x1B	Vrms	USI24	RMS Voltage (LSB weight determined by Vscale)
0x1E	Irms	USI24	RMS Current (LSB weight determined by Iscale)
0x21	Watt	SSI24	Active Power (LSB weight determined by Pscale)
0x24	PAverage	SSI24	Active Power Averaged over 30s Window (LSB determined by Pscale)
0x27	PF	SSI24	Power Factor (LSB weight determined by PFscale)
0x2A	Frequency	USI24	Line Frequency (LSB weight determined by Fscale)
0x30	Alarms	B24	Alarm Status Registers
0x33	Vfund	USI24	RMS Voltage (Fundamental) (LSB weight determined by Vscale)
0x36	Ifund	USI24	RMS Current (Fundamental) (LSB weight determined by Iscale)
0x39	Pfund	SSI24	Active Power (Fundamental) (LSB weight determined by Pscale)
0x3C	Qfund	SSI24	Reactive Power (Fundamental) (LSB weight determined by Pscale)
0x3F	VAfund	SSI24	Apparent Power (Fundamental) (LSB weight determined by Pscale)
0x42	Vharm	USI24	RMS Voltage (Harmonic) (LSB weight determined by Vscale)
0x45	Iharm	USI24	RMS Current (Harmonic) (LSB weight determined by Iscale)
0x48	Pharm	SSI24	Active Power (Harmonic) (LSB weight determined by Pscale)
0x4B	Qharm	SSI24	Reactive Power (Harmonic) (LSB weight determined by Pscale)
0x4E	VAharm	SSI24	Apparent Power (Harmonic) (LSB weight determined by Pscale)
0x57	ILow	USI24	Lowest RMS Current Recorded Since Reset (LSB determined by Iscale)
0x5A	IHigh	USI24	Highest RMS Current Recorded Since Reset (LSB determined by Iscale)
0x5D	Ipeak	USI24	Highest Current in last accumulation Interval (LSB determined by Iscale)
0x60	VLow	USI24	Lowest RMS Voltage Recorded Since Reset (LSB determined by Vscale)
0x63	VHigh	USI24	Highest RMS Voltage Recorded Since Reset (LSB weight determined by Vscale)
0x66	Vpeak	USI24	Highest Voltage in last accumulation Interval (LSB weight determined by Vscale)
0xA8:C9	–	UINT24	Event Counters for Alarms

Address (Hex)	Variable Name	Data Type	Description
0xD5	ExtTemp1	USI24	External temperature 1 (ATEMP1 input)
0xD8	ExtTemp2	USI24	External temperature 2 (ATEMP2 input)
0x10E	Divisor	UINT24	Actual Accumulation interval for low rate results
0x147	DIOState	B24	State of DIO Outputs
0x156	Irms1	UINT24	Unscaled RMS Current
0x159	Vrms1	UINT24	Unscaled RMS Voltage
0x15C	Power1	INT24	Unscaled Active Power
0x15F	Var1	INT24	Unscaled Reactive Power
0x162	VA1	INT24	Unscaled Apparent Power
0x165	PF1	INT24	Unscaled Power Factor
0x168	Freq1	UINT24	Unscaled Frequency

High-Rate Result (Output Registers)

These output registers contain the instantaneous values of voltage, current, power and quadrature power. The high-rate registers are updated at the ADC Sampling Frequency (4.0 kHz). These register, given the relatively high update rate, should be accessed with a high speed interface such as SPI.

Table 6: High-Rate Result Registers

Address (Hex)	Variable Name	Data Type	Description
0x16B	V (1)	INT24	High-Rate Voltage
0x16E	I (1)	INT24	High-Rate Current
0x171	Vq (1)	INT24	High-Rate Quadrature Voltage
0x174	P (1)	INT24	High-Rate Power
0x177	PQ (1)	INT24	High-Rate Quadrature Power
0x17A	Cycle (1)	UINT24	High-Rate samples
0x17D	Scycle (1)	UINT24	High-Rate Sag/Surge Cycles

Note:

1) The high rate registers are updated at the ADC converter sample rate. In order to access real time data it is preferable to utilize the SPI interface.

3.4 Input Registers (Setup and Calibration)

Input Registers are used to configure the device, issue commands etc. The input registers content can be saved to flash memory the values restored as defaults upon power-on or reset.

Table 7: Input Registers

Address (Hex)	Variable Name	Data Type	Flash Saved	Description	Default (Decimal)
0x00	Command	B24	Y	Command Register (see Command Register Section)	
0x06	PhaseComp	S.21	Y	Phase compensation (high-rate samples)	0
0x09	Alarm_Mask1	B24	Y	Alarm mask bits for $\overline{\text{ACFAULT}}$ pin	
0x0C	Alarm_Set	B24	Y	Sets corresponding alarm bits	
0x0F	Alarm_Reset	B24	Y	Clears corresponding alarm bits	
0x2D	DevAddr	UINT24	Y	UART (MultiPoint) and I^2C Address	0
0x51	Alarm_Mask2	B24	Y	Alarm mask bits for $\overline{\text{ACCRIT}}$ pin	
0x54	Sticky	B24	Y	Alarm bits to control auto-reset of alarm status	
0x69:8D	–	–	Y	Alarm Limit Registers (See Section 3.6)	
0x90:A2	–	–	Y	Alarm Holdoff Time Registers (See Section 3.6)	
0xA5	IrOff	U.23	Y	RMS Current Offset Adjust	
0xA8	VrOff	U.23	Y	RMS Voltage Offset Adjust	
0xAB	POff	U.23	Y	Power Offset Adjust	
0xCC:DC	RESERVED	N/A	N/A	Registers 0xCC through 0xDC are reserved.	N/A
0xDB	Temp1Gain	UINT24	Y	External Temperature Gain.	0
0xDE	Temp2Gain	UINT24	Y	External Temperature Gain.	0
0xE1	HPFCoeffI	U.23	Y	Current offset removal settling time	1
0xE4	HPFCoeffV	U.23	Y	Voltage offset removal settling time	1
0xE7	Itarget	UINT24	Y	Calibration current gain target.	168,000
0xEA	Vtarget	UINT24	Y	Calibration voltage gain target.	130,000
0xED	CalCyc	UINT24	Y	Number of Calibration cycles to average.	5
0xF0	Igain	U.21	Y	Current Gain setting (updated after calibration) range 0 to 4	1
0xF3	Vgain	U.21	Y	Voltage Gain Setting (updated after calibration).	1
0xF6	Ioff	S.23	Y	Current offset (updated after calibration).	N/A
0xF9	Voff	S.23	Y	Voltage offset (updated after calibration).	N/A
0xFC	Tgain	U.24	Y	Die temperature gain setting (updated after calibration).	701,233
0xFF	Toffs	U.24	Y	Die Temperature offset (updated after calibration).	287,831
0x102	SysGain	S.23	N	Temperature compensated system gain (updated after calibration).	N/A
0x105	Harm	UINT24	N	Harmonic selector.	1
0x108	Saccum	UINT24	N	Accumulation interval for Sag and Surge.	40
0x10B	Accum	UINT24	N	Accumulation Interval for calculation (RMS, etc.).	400
0x111	Frame	UINT48	N	Low rate frame number counter.	N/A

Address (Hex)	Variable Name	Data Type	Flash Saved	Description	Default (Decimal)
0x117	XYcomp	UINT24	Y	Line Filters Capacitive Compensation.	0
0x11A	Rcomp	UINT24	Y	Resistive I/R drop compensation.	0
0x11D	Iscale	UINT24	Y	Current scaling register.	30,000
0x120	Vscale	UINT24	Y	Voltage scaling register.	30,000
0x123	Pscale	UINT24	Y	Power scaling register.	6,900,000
0x126	PFscale	UINT24	Y	Power Factor scaling register.	1,000
0x129	Fscale	UINT24	Y	Frequency scaling register.	1,000
0x12C	Tscale	UINT24	Y	Temperature Scaling register.	1,000
0x12F:144	–	UINT24	Y	Relay Configuration Registers (See Section 3.5)	
0x14A	TC1	UINT24	Y	Temperature Compensation.	0
0x14D	TC2	UINT24	Y	Temperature Compensation.	0
0x147	RESERVED	B24	N	Read-Only Register	N/A

3.5 Relay Configuration

The registers in Table 8 are used to configure the relay operations.

Table 8: Relay Configuration Registers

Address	Register	Format	Flash Saved	Description	Default (Decimal)
0x12F	RelayOnMin	UINT24	Y	Minimum Voltage to keep Relay ON (LSB weight determined by Vscale)	85,000
0x132	RelayOnMax	UINT24	Y	Maximum Voltage to keep Relay ON (LSB weight determined by Vscale)	255,000
0x135	RelayOnTime	UINT24	Y	Hold ON Time (samples) if min/max not met	4
0x138	RelayOffMin	UINT24	Y	Minimum Voltage to keep Relay OFF (LSB weight determined by Vscale)	90,000
0x13B	RelayOffMax	UINT24	Y	Maximum Voltage to keep Relay OFF (LSB weight determined by Vscale)	250,000
0x13E	RelayOffTime	UINT24	Y	Hold OFF Time (samples) if min/max met	4
0x141	RelayOnDelay	UINT24	Y	Relay Closure Time (ms)	0
0x144	RelayOffDelay	UINT24	Y	Relay Opening Time (ms)	0

3.6 DIOState Register

The DIOState register reports the state of the digital input/output pins. Unconnected or floating pins are reported as set as one. Table 9 lists the bit assignments.

Table 9: DIOState Register

Bit	Pin Status	Function
23-11	N/A	N/A
10	MP1	Multi-Purpose Digital I/O
9	MP0	Multi-Purpose Digital I/O
8	IFCONFIG	UART/I^2C/SPI Selection
7	$\overline{\text{ACFAULT}}$	ACFAULT Alarm
6	ADDR1	I^2C/Multi-Point UART Address
5	SSB/DIR/SCL	Slave Select (SPI) / RS485 TX-RX / I^2C Serial Clock
4	$\overline{\text{ACCRIT}}$	AC Input Voltage Alarm (Critical)
3	SDO/TX/SDAi	SPI DATA OUT/ UART TX/I^2C Data In
2	SDI/RX/SDAo	SPI DATA IN / UART RX/I^2C Data Out
1	SPCK/ADDR0	SPI CLOCK IN / I^2C/Multi-Point UART Address
0	RELAYCTRL	Relay Control Output

3.7 Alarms and Alarms Configuration Registers

3.7.1 Alarms Status Register (address 0x30)

The Alarms Status register is an output register (read-only) that contains the status of the alarms and other conditions. Table 10 reports the Alarms register bit assignment and the corresponding limit registers (thresholds) and Hold-Off time registers.

Table 10: Alarms Register and Corresponding Configuration Registers

Bit	Alarms Register (Bit)	Limit Register (1)	Hold-Off Register (1)	Function
23	DataReady	–	–	Low-Rate results have been updated.
22	OverTemp	Tmax	TminHold	Die Temperature is Over Limit.
21	UnderTemp	Tmin	TminHold	Die Temperature is Under Limit.
19	ExtOvTemp1	XMax1	–	External Temperature 1 is Over Limit.
18	ExtOvTemp2	XMax2	–	External Temperature 2 is Over Limit.
17-12	Not Used	N/A	N/A	Not Used.
11	Vsag	Vsag	VsagHold	Voltage Sagged below limit.
10	Vsurge	Vsurge	VsagHold	Voltage Surged above limit.
9	VdropOut	Vdrop	–	Voltage Dropped below limit.
8	OverVolt	Vmax	VminHold	RMS Voltage went above upper limit.
7	UnderVolt	Vmin	VminHold	RMS Voltage fell below lower limit.
6	OverCurrent	Imax	ImaxHold	RMS Current went above limit.
5	OverPower	Pmax	PmaxHold	Power went above limit.
4	OverFreq	Fmax	Fminhold	Line Frequency went above upper limit.
3	UnderFreq	Fmin	Fminhold	Line Frequency fell below lower limit.
2	Relay_On	–	–	Relay is ON.
1	Zero_Cross	–	–	Voltage low-to-high Zero Crossing Detected (auto-clears).
0	Not Used	–	–	Not Used.

Note:

1) These are input registers and their value can be saved in flash memory as defaults through the ACC Command.

3.7.2 AlarmSticky Register (address 0x54)

The AlarmSticky register is an input register that allows configuring individual bits into the Alarms register to hold the alarm status (“sticky”) until an AlarmReset command is issued. Each alarm can otherwise be set to auto-reset at the completion of each accumulation interval.

The AlarmSticky register can be saved into flash memory.

Table 11: AlarmSticky Register Bits Assignment

Bit	Alarm	Function
23	N/A	N/A
22	OverTemp	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
21	UnderTemp	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
19	ExtOvTemp1	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
18	ExtOvTemp2	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
17-12	Not Used	Not Used.
11	Vsag	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
10	Vsurge	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
9	VdropOut	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
8	OverVolt	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
7	UnderVolt	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
6	OverCurrent	1 = Alarm bit is set until AlarmReset command is issued. 0 = Alarm bit is cleared at every accumulation Interval.
5	OverPower	1 = Alarm bit is set until AlarmReset command. 0 = Alarm cleared at every accumulation Interval.
4	OverFreq	1 = Alarm bit is set until AlarmReset command. 0 = Alarm cleared at every accumulation Interval.
3	UnderFreq	1 = Alarm bit is set until AlarmReset command. 0 = Alarm cleared at every accumulation Interval.
2	N/A	N/A
1	N/A	N/A
0	Not Used	Not Used.

3.7.3 AlarmMask1 (address 0x09) and AlarmMask2 (address 0x51)

The registers AlarmMask1 and AlarmMask2 allow the user to select which alarm will be used to drive the corresponding alarm pins: AlarmMask1 controls $\overline{\text{ACFAULT}}$ pin while AlarmMask2 controls $\overline{\text{ACCRIT}}$ pin. For example, to select OverCurrent and Vsurge to drive the $\overline{\text{ACFAULT}}$ pin, AlarmMask1 should be set to 0x000440. The AlarmMask1 and AlarmMask2 registers can be saved into flash memory.

Table 12: AlarmMask1 and AlarmMask2 Registers Bits Assignment

Bit	Alarm/ Status	Default	Function
23	DataReady	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
22	OverTemp	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
21	UnderTemp	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
19	ExtOvTemp1	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
18	ExtOvTemp2	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
17-12	Not Used		Not Used
11	Vsag	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
10	Vsurge	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
9	VdropOut	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
8	OverVolt	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
7	UnderVolt	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
6	OverCurrent	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
5	OverPower	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
4	OverFreq	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
3	UnderFreq	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
2	Relay_On	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
1	Zero_Cross	0	1 = Alarm drives alarm output pin; 0 = Alarm has no effect on alarm output pin.
0	Not Used		Not Used.

3.7.4 AlarmSet Register (address 0x0C)

The AlarmSet register is used to force an alarm by setting the corresponding bit. This register is mainly used for relay control and system test purposes.

Table 13: AlarmSet Register Bit Assignments

Bit	Alarm/ Status	Default	Function
23	DataReady	0	1 = Force Alarm; 0 = No Operation
22	OverTemp	0	1 = Force Alarm; 0 = No Operation
21	UnderTemp	0	1 = Force Alarm; 0 = No Operation
19	ExtOvTemp1	0	1 = Force Alarm; 0 = No Operation
18	ExtOvTemp2	0	1 = Force Alarm; 0 = No Operation
17-12	Not Used	–	Not Used
11	Vsag	0	1 = Force Alarm; 0 = No Operation
10	Vsurge	0	1 = Force Alarm; 0 = No Operation
9	VdropOut	0	1 = Force Alarm; 0 = No Operation
8	OverVolt	0	1 = Force Alarm; 0 = No Operation
7	UnderVolt	0	1 = Force Alarm; 0 = No Operation
6	OverCurrent	0	1 = Force Alarm; 0 = No Operation
5	OverPower	0	1 = Force Alarm; 0 = No Operation
4	OverFreq	0	1 = Force Alarm; 0 = No Operation
3	UnderFreq	0	1 = Force Alarm; 0 = No Operation
2	Relay_On	0	1 = Force Alarm; 0 = No Operation
1	Zero_Cross	0	1 = Force Alarm; 0 = No Operation
0	Not Used	–	Not Used

3.7.5 AlarmReset Register (address 0x0F)

The AlarmReset register is used to clear an alarm by setting the corresponding bit.

Table 14: AlarmReset Registers Bit Assignments

Bit	Alarm/ Status	Default	Function
23	DataReady	0	1 = Clear Alarm ; 0 = No Operation
22	OverTemp	0	1 = Clear Alarm ; 0 = No Operation
21	UnderTemp	0	1 = Clear Alarm ; 0 = No Operation
19	ExtOvTemp1	0	1 = Clear Alarm ; 0 = No Operation
18	ExtOvTemp2	0	1 = Clear Alarm ; 0 = No Operation
17-12	Not Used	–	Not Used
11	Vsag	0	1 = Clear Alarm ; 0 = No Operation
10	Vsurge	0	1 = Clear Alarm ; 0 = No Operation
9	VdropOut	0	1 = Clear Alarm ; 0 = No Operation
8	OverVolt	0	1 = Clear Alarm ; 0 = No Operation
7	UnderVolt	0	1 = Clear Alarm ; 0 = No Operation
6	OverCurrent	0	1 = Clear Alarm ; 0 = No Operation
5	OverPower	0	1 = Clear Alarm ; 0 = No Operation
4	OverFreq	0	1 = Clear Alarm ; 0 = No Operation
3	UnderFreq	0	1 = Clear Alarm ; 0 = No Operation
2	Relay_On	0	1 = Clear Alarm ; 0 = No Operation
1	Zero_Cross	0	1 = Clear Alarm ; 0 = No Operation
0	Not Used	–	Not Used

3.7.6 Alarms Configuration Registers (Thresholds and Hold-Off Time)

Table 15: Alarms Threshold Registers

Address	Register	Format	Flash Saved	Default	Description
0x69	VsurgeTh	UINT24	Y	225,000	Voltage threshold above which VSURGE alarm is activated.
0x6C	VsagTh	UINT24	Y	95,000	Voltage threshold below which VSAG alarm will be activated.
0x6F	VminTh	UINT24	Y	95,000	Voltage threshold below which UNDERVOLT alarm will be activated.
0x72	VmaxTh	UINT24	Y	245,000	Voltage threshold above which OVERVOLT alarm will be activated.
0x75	VdropTh	UINT24	Y	95,000	Voltage threshold below which VDROP alarm will be activated.
0x78	ImaxTh	UINT24	Y	30,000	Current High Alarm Limit.
0x7B	PmaxTh	UINT24	Y	7,350,000	Power High Alarm Limit.
0x7E	TminTh	INT24	Y	-40,000	Die temperature threshold below which the UNDERTEMP alarm will be activated.
0x81	TmaxTh	INT24	Y	125,000	Die temperature threshold above which the OVERTEMP alarm will be activated.
0x84	Temp1Thres	UINT24	Y	0	External temperature (thermistor) threshold below which the ExtOvTemp1alarm will be activated.
0x87	Temp2Thres	UINT24	Y	0	External temperature (thermistor) threshold below which the ExtOvTemp2 alarm will be activated.
0x8A	FminTh	UINT24	Y	40,000	Line Frequency threshold below which the UNDERFREQ alarm will be activated.
0x8D	FmaxTh	UINT24	Y	70,000	Line frequency threshold above which the OVERFREQ alarm will be activated.

Table 16: Alarms Hold-Off Timers Registers

Address	Register	Format	Flash Saved	Default	Description
0x90	VSagHo VSurgeHo	UINT24	Y	4	Holdoff Time (in High-rate sample) for Voltage Sag and Surge Alarm (shared)
0x93	Not Used	–	–	–	
0x96	VminHo VmaxHo	UINT24	Y	4	Number of consecutive accumulation intervals in which the RMS voltage must exceed the specified limit before the UNDERVOLT or OVERVOLT alarms will be activated.
0x99	ImaxHo	UINT24	Y	4	Number of consecutive accumulation intervals in which the RMS current must exceed the IMAX threshold before the OVERCURRENT alarm will be activated.
0x9C	PmaxHo	INT24	Y	4	Number of consecutive accumulation intervals in which power must exceed the PMAX threshold before the OVERWATT alarm will be activated.
0x9F	TminHo TmaxHo	INT24	Y	4	Number of consecutive accumulation intervals in which the die temperature must exceed either TMIN or TMAX before the OVERTEMP or UNDERTEMP alarm will be activated.
0xA2	FminHo FmaxHo	UINT24	Y	4	Number of consecutive accumulation intervals in which the line frequency must exceed either FMIN or FMAX before the UNDERFREQ or OVERFREQ alarm will be activated.

3.7.7 Alarm Counter Registers

Counter registers increment at each alarm occurrence and can be cleared by the user by writing a zero value.

Table 17: Alarms Counter Registers

Address	Register	Format	Description
0xAE	TminCnt	UINT24	The number of times an UNDERTEMP event has been detected.
0xB1	TmaxCnt	UINT24	The number of times an OVERTEMP event has been detected.
0xB4	VminCnt	UINT24	The number of times an UNDERVOLT event has been detected.
0xB7	VmaxCnt	UINT24	The number of times an OVERVOLT event has been detected.
0xBA	ImaxCnt	UINT24	The number of times an OVERCURRENT event has been detected.
0xBD	PmaxCnt	UINT24	The number of times an OVERWATT event has been detected.
0xC0	FminCnt	UINT24	The number of times an UNDERFREQ event has been detected.
0xC3	FmaxCnt	UINT24	The number of times an OVERFREQ event has been detected.
0xC6	VsagCnt	UINT24	The number of times a VSAG event has been detected.
0xC9	Vsurgecnt	UINT24	The number of times a VSURGE event has been detected.

3.8 Command Register

The Command Register is located at address 0x00. Use this register to perform specific tasks such as saving coefficients and some input registers into flash memory. It also allows issuing calibration commands.

Save to Flash Command

Use the ACC command to save to flash the calibration coefficients and system defaults contained in the some of the input registers. Upon reset or power-on, the values stored in flash will become new system defaults.

The following table describes the ACC command bits:

Bit(s)	Value	Description
23:12	0xACC	"Access" Command.
11:8	0x2	2: Save Calibration to flash.
7:6	0x0	Not used.
5	1	Line Lock Bit.
4:0	0x0	Not used.

General Settings (Command 000)

The general settings command allows the user to enable functions such as UART auto reporting, relay operations, and Line Lock mode etc.

Bit(s)	Value	Description
23:12	0x00	"General settings" command.
11	0	Not Used
10	T	Stop temperature update: 1=stop; 0=update. This bit prevents the firmware from overwriting the TempC (temperature result) register. This is necessary when supplying a known temperature for calibration.
6	FREQ	Stop Frequency update 1=stop; 0=update. This bit stops the update of Freq used by the sine/cosine generator for fundamental and harmonic measurements. It is the unscaled value of Frequency with 8 integer and 16 fraction bits. The user can set the fundamental frequency when FREQ is set.
5	LL	Line Lock 1= lock to line cycle; 0= independent. This bit selects the accumulation interval (computation cycle) mode. If not locked the computation is executed over a fixed number of samples (high rate) contained in the Accum register. If locked, the computation is executed over a number of samples accumulation interval.
4	TC	Enable Gain/Temperature compensation 1=enable; 0=disable. This bit allows the firmware to modify the system gain based on measured temperature.
3	AR	Enable Auto Reporting 1=enable; 0=disable. This bit enables auto reporting mode on UART. The user or host can also set or clear this command bit, enabling or disabling auto reporting.
2	AY	Enable Autonomous Relay operation 1=enable; 0=disable/normal mode. This bit enables autonomous relay operation. The user or host can also set or clear this command bit, enabling or disabling autonomous operation.
1:0	–	Not used

CA (Calibration) Command

The Calibration Command starts the calibration process for the selected inputs. It is assumed that appropriate input signals are applied before starting calibration. When the calibration process completes, bits 23:16 are cleared along with bits associated with channels that calibrated successfully. Any channels that failed will have their corresponding bit left set.

Bit(s)	Value	Description
23:16	0xCA	“Calibrate” Command.
15:14	0	Not Used (set to 0)
13	XYR	Calibrate X+Y or R Compensation Coefficient
12	V	Calibrate Voltage.
11	I	Calibrate Current.
10	T	Calibrate Temperature.
9	O	Calibrate Offset versus Gain.
8:7	0	Note Used (set to 0)
6	FREQ	Stop Freq Update.
5	LL	Lock Sample Period to Line Cycle.
4:0	0	Not Used (set to 0)

NOTE:

During calibration, the “line-lock” bit should be set.

4 Serial Interfaces

All user registers are contained in a 256 word (24-bits each) area of the on-chip RAM and can be accessed through the UART, SPI, or I^2C interfaces. For word-addressable SPI and I^2C interfaces, one must divide the documented register address by 3. While access to a single byte is possible with some interfaces, it is highly recommended that the user access words (or multiple words) of data with each transaction.

Serial Interface Selection

The 78M6610+PSU provides UART, I^2C, and SPI interface options, but only one interface can be active at a time. The user activates the interface through the configuration of pins IFCONFIG and SSB/DIR/SCL according to the following table.

Selected Interface	SSB/DIR/SCL	IFCONFIG
SPI	X (don't care)	0
UART	0	1
I^2C	1	1

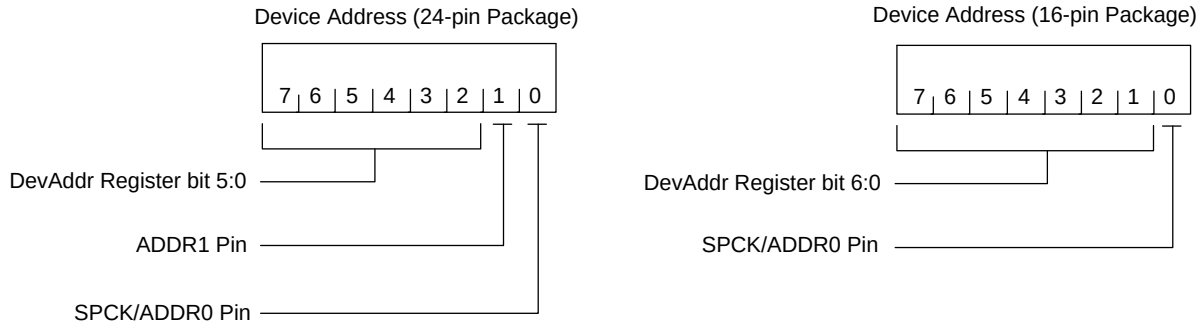
The interface selection pins are sampled following power-on and reset. The user should allow at least 10 ms from a power-on or reset event for them to be latched and the serial interface selected. During this time the status of these pins must not change.

Warning

Where applicable, pins should be configured via pull-up and pull-down resistors as these pins could become outputs after initialization. Therefore, direct connection to GNDD/GNDA or V_{3P3D}/V_{3P3A} supplies must be avoided.

Device Address (UART)

The UART interface supports a multi-point communications protocol. Each device is identified by a specific address that is configured through the DevAddr register and pins Addr0 and Addr1 according to the following figure. DevAddr Register Bits 23 through 7 are not used and should be set to 0. Their status has no effect on the device address.



A change of the address is always effective after a power-on or reset. During the initialization following a power-on or reset, the DevAddr register value is restored with the value contained in Flash memory and the address pin status is acquired.

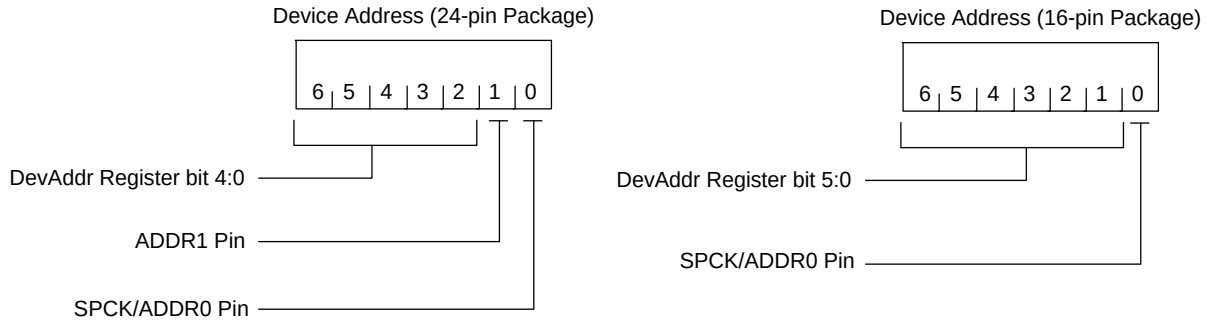
It is possible to modify the device address by setting the DevAddr register (through any of the interfaces) as well as the address pins status. If DevAddr register is modified, it is necessary to save its content into Flash through the ACC command. Following a reset or power-on the device will resume operation with the new address.

Note

In UART operation, the implemented protocol does not directly use the device address. An SSI ID equal to the device address+1 is used. For example, the theoretical device address range of 0 to 127 corresponds to an SSI ID range of 1 to 128.

Device Address (I^2C)

The I^2C interface address can be set through device pins and the DevAddr register.
The upper 5 bits (on 24-pin device) or 6 bits (on 16-pin device) are set through the DevAddr register.
While the lower 2-bits (24-pin device) or 1-bit (16-pin device) are set through the Addr0 and ADDR1 pins, according to the following figure.



The DevAddr register bits 23 through 6 are not used and their status has no effect on the device address configuration.

A change of the address is always effective after a power-on or reset. During the initialization following a power-on or reset, the DevAddr register value is restored with the value contained in Flash memory and the address pin status is acquired.

It is possible to modify the device address by setting the DevAddr register (through any of the interfaces) as well as the address pins status. If DevAddr register is modified, it is necessary to save its content into Flash through the ACC command. Following a reset or power-on the device will resume operation with the new address.

4.1 UART Interface

The byte-addressable UART interface on the 78M6610+PSU features a binary communication protocol called SSI with two modes:

- A Command Response mode supporting single and multi-point communications, including direction control for an RS-485 transceiver. This mode supports a 4-wire RS-485 bus.
- An Auto Report mode that transmits data automatically at the completion of an accumulation interval without host intervention.

The supported configuration is 38400 baud, 8-bit, no-parity, 1 stop-bit, no flow control. The SSB/DIR/SCL pin is used to drive an RS-485 transceiver output enable or direction pin.

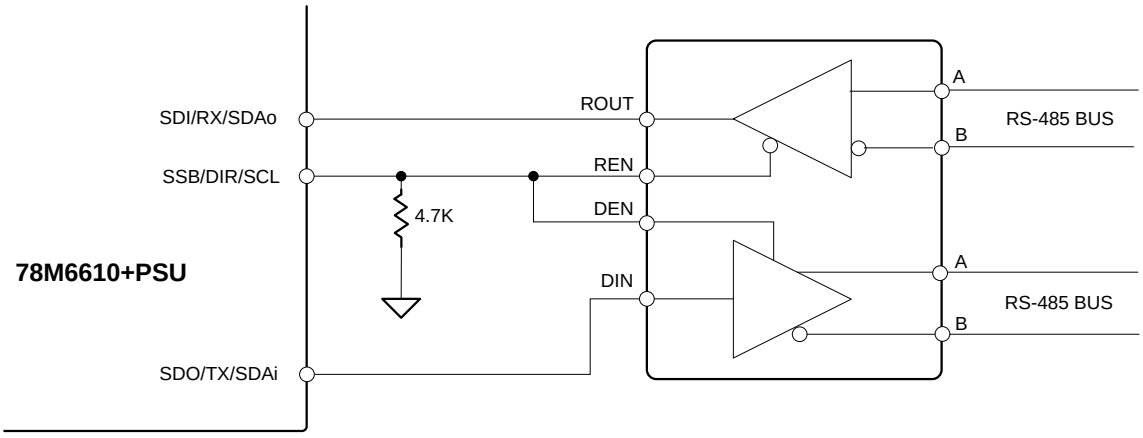


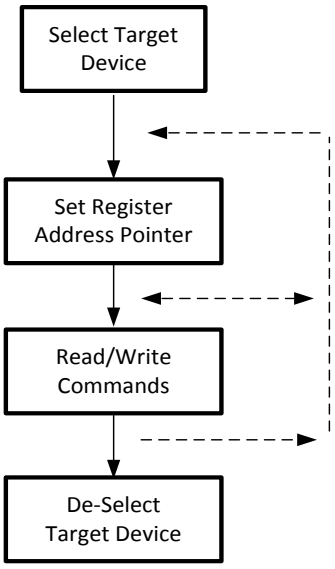
Figure 15: UART Connections on a RS-485 Bus

The implemented SSI protocol uses binary packets, which contain synchronization, addressing, payload, and data integrity check. The responses also contain acknowledge/error indicators.

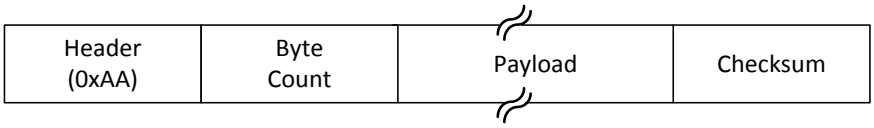
The SSI ID for each 78M6610+PSU is defined by a device address that is configured through the register DevAddr, which provides address bits 7 through 2 of the device address. While address bits 0 and 1 are configured through pins ADDR1 and SPCK/ADDR0 (24-pin package). In 16-pin package devices, the DevAddr register provides address bits 7 though 1, while bit 0 is configured through the pin SPCK/ADDR0.

4.1.1 Command-Response Protocol Description

In this protocol, the host is the master and must initiate communications. The master should first select the device that needs to communicate with, then set the device's register address pointer and finally performing the read or write operations. The sequence of operation is shown in the following diagram.



After sending the synchronization header code (0xAA), the master sends (in the following order) the byte counts (bytes in payload), the payload and then the checksum that provides data integrity check. The following figure shows a generic command packet generated from the master:



The payload contains commands, device address, registers address, data etc. The payload can contain either a single command or multiple commands. The protocol allows for reading or writing one up to 252 bytes in a single operation. Following is the data access method for both read and write. Only the payload is shown.

Device Selection

The device needs to be selected first using the following command:

PAYLOAD	
0xCF Command	SSI ID

The 78M6610+PSU replies with an acknowledge message.

Once the device is selected, the SSB/DIR/SCL pin will be asserted (logic high), enabling the RS-485 bus driver. The SSB/DIR/SCL pin will be asserted until the device is de-selected.

Register Address Pointer Selection

The following message sets the address pointer to the register (or set of registers) to read or write:

PAYLOAD	
0xA3 Command	Register Address (2 Bytes)

The 78M6610+PSU replies with an acknowledge message.

Read Command

It is possible to read data from the 78M6610+PSU using the 0xE command. To read 0 to 15 bytes, the command byte is completed with the number of bytes to read. For example, to read 3 bytes:

PAYLOAD
0xE3 Command

In order to read a larger number of bytes (up to 255), the command 0xE0 must be used. In this case, the command 0xE0 must be followed by a byte containing the number of bytes to be read. For example to read 31 bytes:

PAYLOAD	
0xE0 Command	0x1F (Number of Bytes to Read)

Write Command

It is possible to write data to the 78M6610+PSU using the 0xD command. To write 1 to 15 bytes, the command byte must be completed with the number of bytes of data to write. For example to write 3 bytes:

PAYLOAD	
0xD3 Command	Data (Number of Bytes = 3)

In order to write a larger number of bytes (up to 255), the command 0xD0 must be used. In this case, the number of data bytes to follow is determined by the Byte Count. For example to write 31 bytes:

PAYLOAD	
0xD0 Command	Data (Number of Bytes = Byte Count – 4)

After each read or write operation, the internal address pointer is incremented to point to the address that followed the target of the previous read or write operation.

Table 18 lists the commands that are supported by the 78M6610+PSU.

Table 18: Host Commands

Command	Parameters	Description
0 - 7F		(invalid)
80 - 9F		(not used)
A0		Clear address
A1	[byte-L]	Set Read/Write address bits [7:0]
A2	[byte-H]	Set Read/Write address bits [15:8]
A3	[byte-L][byte-H]	Set Read/Write address bits [15:0]
A4 - AF		(reserved for larger address targets)
B0 - BF		(not used)
C0		De-select Target (target will Acknowledge)
C1 - CE		Select target 1 to 14
CF	[byte]	Select target 0 to 255
D0	[data...]	Write bytes set by remainder of Byte Count
D1 - DF	[data...]	Write 1 to 15 bytes
E0	[byte]	Read 0 to 255 bytes
E1 – EF		Read 1 to 15 bytes
F0 - FF		(not used)

Slave Packets

The 78M6610+PSU replies to the host processor either with an acknowledge (either ACK or NACK) or with data. The format of slave packets depends upon the type of response to the master device.

Table 19 lists the reply codes and their meanings.

Table 19: Slave Reply Codes

Code	Definition
0xAA	Acknowledge with data.
0xAE	Auto Reporting Header (with data).
0xAD	Acknowledge without data.
0xB0	Negative Acknowledge (NACK).
0xBC	Command not implemented.
0xBD	Checksum failed.
0xBF	Buffer overflow (or packet too long).
- timeout -	Any condition too difficult to handle with a reply.

4.1.2 Auto-Reported Data

By default, the 78M6610+PSU automatically reports a set of data at the completion of each accumulation interval. This mode is used in systems where the host will not have to poll the 78M6610+PSU for data but it receives automatically data updated at the accumulation interval rate. Table 20 shows the default auto-reported data format.

Table 20: Default Measurements

Parameter/Register	Number of Bytes	Description
Packet Header	1	Start of Data Packet
Packet Length	1	Number of Bytes in the Packet
Vrms	3	RMS Voltage (address 0x1B)
Irms	3	RMS Current (address 0x1E)
Watt	3	Active Power (address 0x21)
PAverage	3	Active Power (30s average) (address 0x24)
PF	3	Power Factor (address 0x27)
Frequency	3	Line Frequency (address 0x2A)
ExtTemp	3	External Temperature (Temp Input) (address 0x2D)
Alarms	3	Alarms and Status (address 0x30)

The content of the auto-reported data packet is configurable by the user. Refer to the relevant application note describing the auto-report packet configuration procedure.

4.2 SPI Interface

The 78M6610+PSU can be configured as SPI slave. Once the SPI interface is activated, it utilizes the following pins:

SSB: Slave select (SS) is an input and active low signal.
SCK: Serial Data Clock (SCK) input.
SDO: Master Input/Slave Output (MISO), serial data output.
SDI: Master Output/Slave Input (MOSI), serial data input.

Clock Polarity and Phase

Figure 16 shows a single-byte transaction on the SPI bus. The data is shifted on the falling edge of the serial data clock and latched on the rising edge.

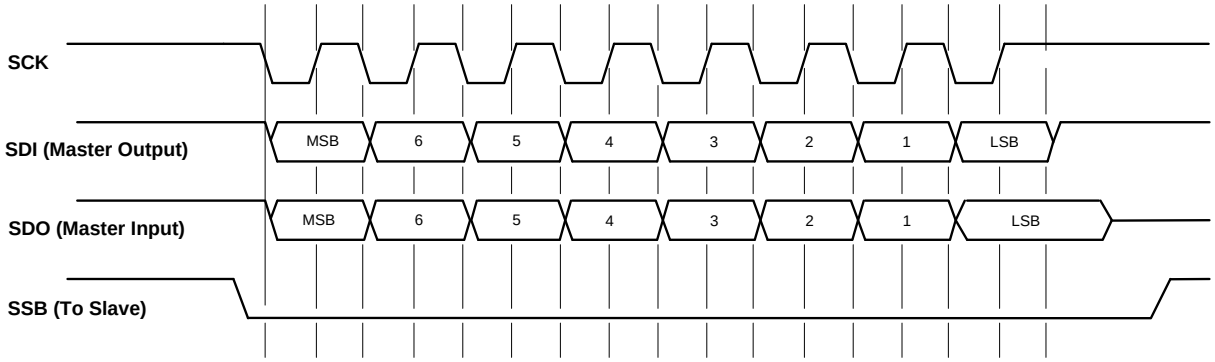


Figure 16: Single-Byte Transaction on the SPI Bus

SPI Protocol

The SPI allows access to read and write registers contained in a 256 word (24-bit) area of the on-chip RAM. The address of each register specified in Section 3 must be divided by 3 for SPI access. The first byte that the master needs to transmit to the 78M6610+PSU (slave) is the control byte. The control byte allows setting the number of words to be transferred and the most significant bits of the register address:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NBRACC[3:0]				ADDR7	ADDR6	0	1

ADDR7 and ADDR6 bits select bit 7 and 6 of the 8-bit register address to be accessed by the following data transactions.

NBRACC[3:0] represents the number of words (3-bytes) accesses to be performed by subsequent read/write transactions. The actual number of data addresses accessed per data transaction is NBRACC + 1. For single address access, the field is set at 0. NBRACC is reset to 0 when the operation (multiple reads or writes) is completed. NBRACC must be set to a non-zero value prior to each multiple word transaction.

The second type of transaction is dedicated to transporting data between the host and the device and is structured as follows:

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	ADDR[5:0]						R/W	0
2	DATA[23:16] @ Addr							
3	DATA[15:8] @ Addr							
4	DATA[7:0] @ Addr							
5	DATA[23:16] @ Addr + 1							
6	DATA[15:8] @ Addr +1							
7	DATA[7:0] @ Addr +1							
…	…							
(NbrAcc *3)	DATA[7:0] @ Addr + NbrAcc							
(NbrAcc*3)+1	DATA[23:16] @ Addr + NbrAcc							
(NbrAcc*3)+2	DATA[15:8] + NbrAcc							
(NbrAcc*3)+3	DATA[7:0] + NbrAcc							

R/W: Defines the directionality of the transaction (Read = 0; Write = 1);
ADDR[5:0]: Indicates the remainder of the address to access.

The following are some transaction examples.

Example 1: Write access of address 0x14.

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NbrAcc[3:0] = 0x00				Addr7=0	Addr6=0	0	1
2	Addr[5:0] = 0x14						WR=1	0
3	Data[23:16] @ 0x14							
4	Data[15:8] @ 0x14							
5	Data[7:0] @ 0x14							

Example 2: Read access of address 0x17 and 0x18.

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NbrAcc[3:0] = 0x01				Addr7=0	Addr6=0	0	1
2	Addr[5:0] = 0x17						RD=0	0
3	Data[23:16] @ 0x17							
4	Data[15:8] @ 0x17							
5	Data[7:0] @ 0x17							
6	Data[23:16] @ 0x18							
7	Data[15:8] @ 0x18							
8	Data[7:0] @ 0x18							

Example 3: Non-Contiguous Read accesses of address 0x17 and 0x0A.

Byte#	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	NbrAcc[3:0] = 0x00				Addr7=0	Addr6=0	0	1
2	Addr[5:0] = 0x17						RD=0	0
3	Data[23:16] @ 0x17							
4	Data[15:8] @ 0x17							
5	Data[7:0] @ 0x17							
6	NbrAcc[3:0] = 0x00				Addr7=0	Addr6=0	0	1
7	Addr[5:0] = 0x0A						W=1	0
8	Data[23:16] @ 0x0A							
9	Data[15:8] @ 0x0A							
10	Data[7:0] @ 0x0A							

The timing of the transaction can be organized in different ways depending on the host capabilities. The above transaction can be a succession of bytes as shown in **Figure 17**. Those bytes are carried by a continuously active SCK, with eight clock periods per byte.

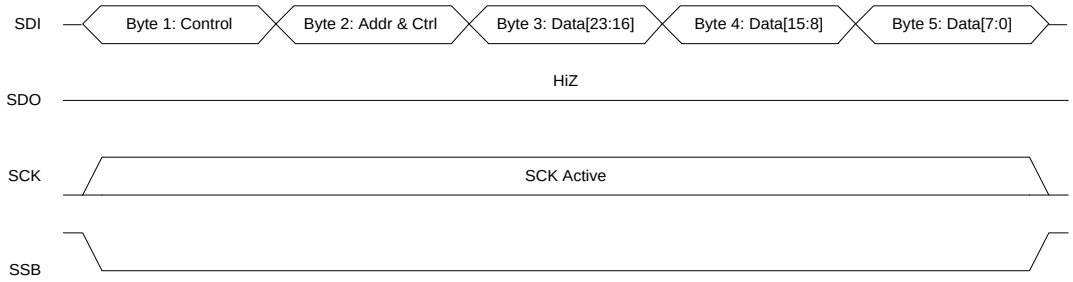


Figure 17: Write Access Example

The host also has the possibility to space out the bytes transmitted. In such a case, SCK is inactive during the “in-between-bytes” gap, as illustrated by **Figure 18**. Note that the figure shows two gaps, one between the configuration and the data transactions and another between bytes within the data transaction. The placement of those gaps is strictly for the purpose of illustrating the concept.

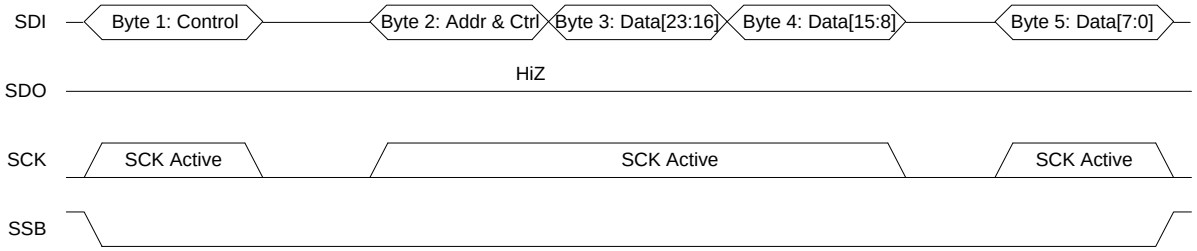


Figure 18: Write Access with Interrupted SCK

4.3 I²C Interface

The 78M6610+PSU has an I²C interface available at the SDAI, SDAO, and SCL pins. The interface supports I²C slave mode with a 7-bit address and operates at a data rate up to 400 kHz. Figure 19 shows two possible configurations. Configuration A is the standard configuration. The double pin for SDA allows the isolated configuration B.

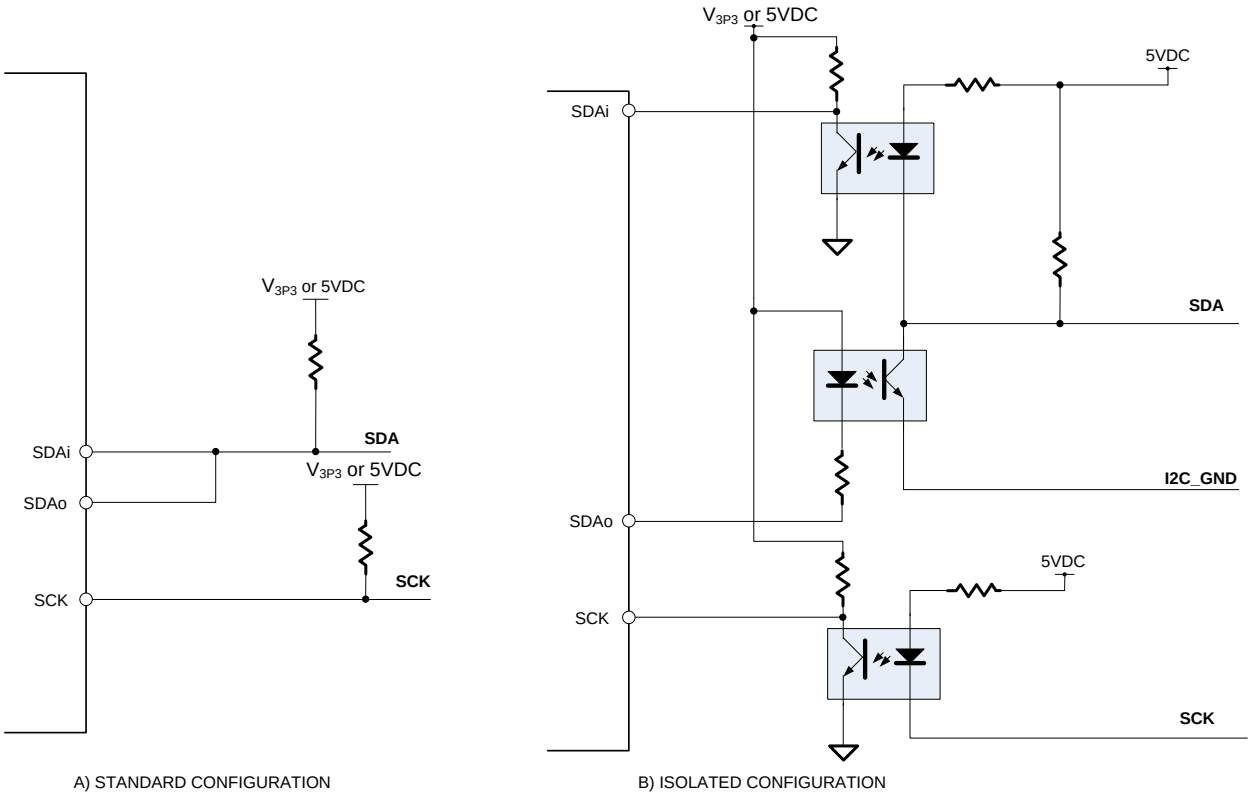


Figure 19: I²C Bus Connection in Standard (A) and Isolated (B) Configuration

The I²C interface allows access to read and write registers contained in a 256 word (24-bit) area of the on-chip RAM. The address of each register specified in Section 3 must be divided by 3 to obtain the relevant address for the I²C access. While access to a single byte is possible, it is highly recommended that the user access words (or multiple words) of data with each transaction.

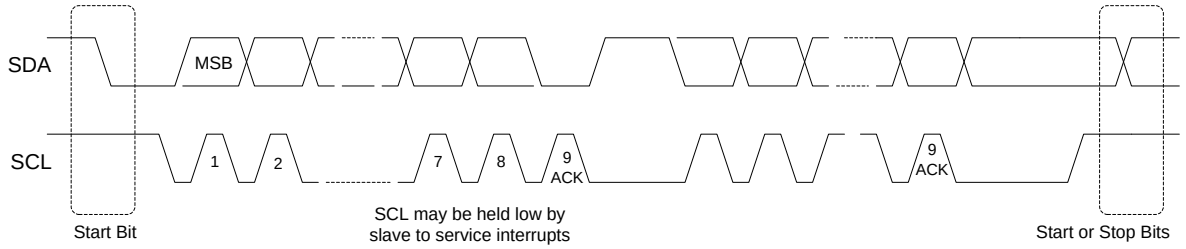
The device address of each 78M6610+PSU is configured through the register DevAddr, which defines address bits 6 through 2 of the device address. Address bits 0 and 1 are configured through pins ADDR1 and SPCK/ADDR0 (24-pin package). With the 16-pin package option, the DevAddr register defines address bits 6 though 1, while bit 0 is configured through the pin SPCK/ADDR0.

Bus Characteristics

- A data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

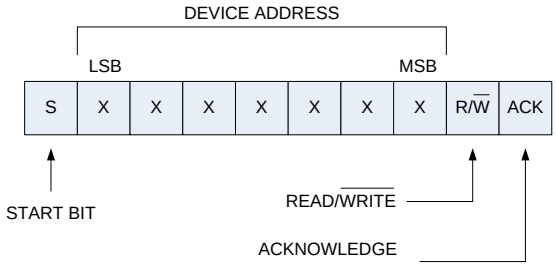
Bus Conditions:

- Bus not Busy (I): Both data and clock lines are HIGH indicating an Idle Condition.
- Start Data Transfer (S): a HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.
- Stop Data Transfer (P): a LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.
- Data Valid: The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.
- Acknowledge (A): Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (78M6610+PSU) will leave the data line HIGH to enable the master to generate the STOP condition.



Device Addressing

A control byte is the first byte received following the START condition from the master device.
The control byte consists of a seven bit address and a bit (LSB) indicating the type of access (0=write; 1=read).



Write Operations

Following the START (S) condition from the master, the device address (7-bits) and the R/W bit (logic low for write) are clocked onto the bus by the master. This indicates to the addressed slave receiver that the register address will follow after it has generated an acknowledge bit (A) during the ninth clock cycle. Therefore, the next byte transmitted by the master is the register address and will be written into the address pointer of the 78M6610+PSU. After receiving another acknowledge (A) signal from the 78M6610+PSU the master device will transmit the data byte(s) to be written into the addressed memory location. The data transfer ends when the master generates a stop (P) condition. This initiates the internal write cycle. The example in Figure 20 shows a 3-byte data write (24-bit register write).

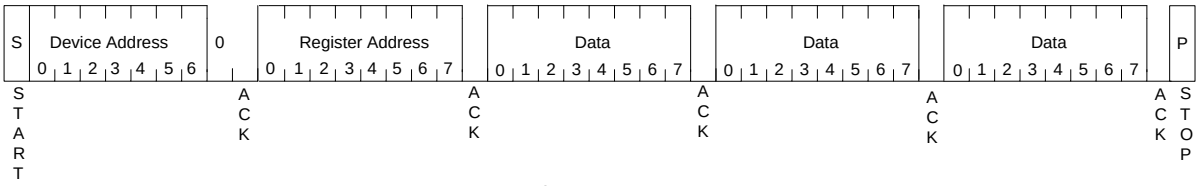


Figure 20: I²C Bus 3-byte Data Write

Upon receiving a STOP (P) condition, the internal register address pointer will be incremented.

The write access can be extended to multiple sequential registers. Figure 21 shows a transaction where multiple register are written sequentially.

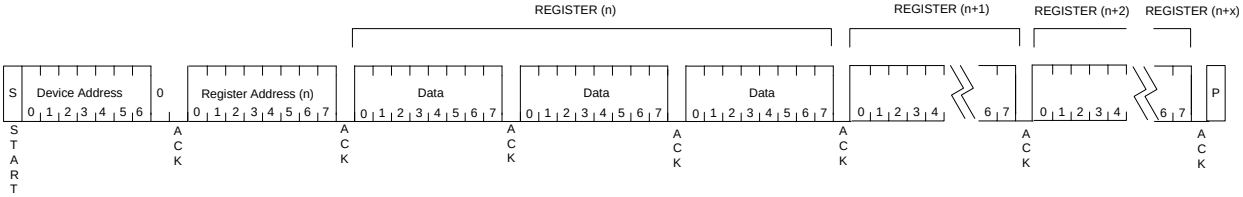


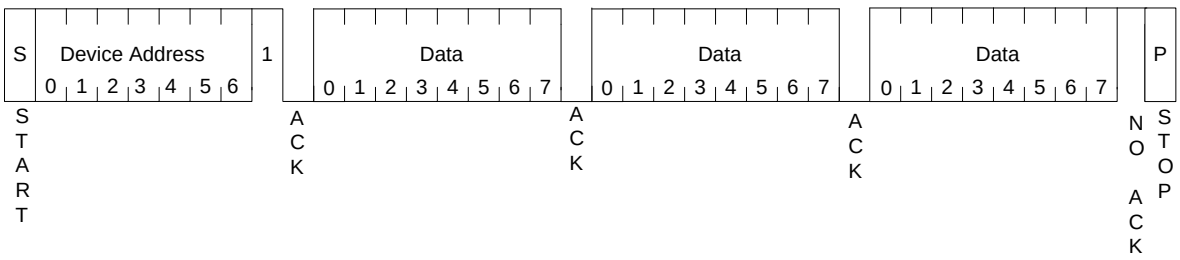
Figure 21: I²C Bus Multiple Sequential Register Write

Read Operations

Read operations are initiated in the same way as write operations with the exception that the R/W bit of the control byte is set to one. There are two basic types of read operations: current address read and random read.

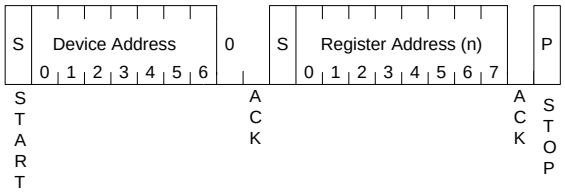
Current Address Read: the 78M6610+PSU contains an address counter that maintains the address of the last register accessed, internally incremented by one when the stop bit is received. Therefore, if the previous read access was to register address n, the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/W bit set to one, the 78M6610+PSU issues an acknowledge (A) and transmits the eight bit data byte. The master will not acknowledge the transfer, but generates a STOP condition to end the transfer and the 78M6610+PSU will discontinue the transmission.

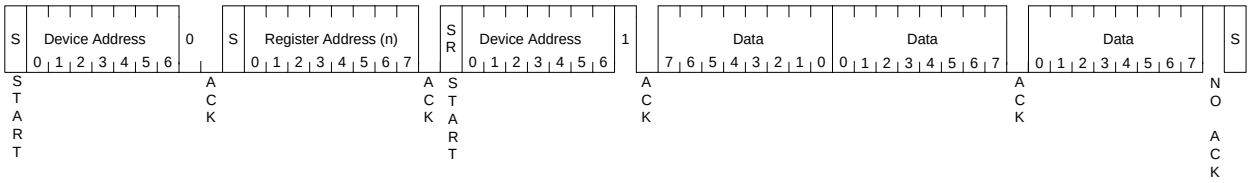


This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

If the register address pointer has not been set by previous operations, it is necessary to set it issuing a command as follows:



Random Read: random read operations allow the master to access any register in a random manner. To perform this operation, the register address must be set as part of the write operation. After the address is sent, the master generates a start condition following the acknowledge response. This sequence completes the write operation. The master should issue the control byte again this time, with the R/W bit set to 1 to indicate a read operation. The 78M6610+PSU will issue the acknowledge response, and transmit the data.
At the end of the transaction the master will not acknowledge the transfer and generate a STOP condition.



This read operation is not limited to 3 bytes but can be extended until the register address pointer reaches its maximum value.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5 V to 4.6 V
GNDD, GNDA	-0.5 V to +0.5 V
Analog Input Pins:	
AVN, AVP, AIN, AIP, ATEMP1, ATEMP2	-10 mA to +10 mA -0.5 V to V_{3P3}+0.5 V
Oscillator Pins:	
XIN, XOUT	-10 mA to +10 mA -0.5 V to 3.0 V
Digital Pins:	
IFCONFIG, $\overline{\text{ACFAULT}}$, ADDR1, SSB/DRI/SCL, $\overline{\text{ACCRIT}}$; SDO/TX/SDAi, SDI/RX/SDAo, ADDR0, RELAYCTRL, MP0, MP1, $\overline{\text{RESET}}$	-30 mA to +30 mA, -0.5 to V_{3P3D}+0.5
Temperatures:	
Operating junction temperature (peak, 100 ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	-45 °C to +165 °C
Solder temperature – 10 second duration	250 °C
ESD stress on all pins	4 kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-Maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

5.2 Recommended External Components

Name	From	To	Function	Value	Unit
XTAL	XIN	XOUT	20.000MHz	20.000	MHz
CXS	XIN	GND	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board).	18±10%	pF
CXL	XOUT	GND		18±10%	pF

5.3 Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V_{3P3})	Normal Operation	3.0	3.3	3.6	V
Operating Temperature		-40	–	+85	ºC

5.4 Performance Specifications

Note that production tests are performed at room temperature.

5.4.1 Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2	–	–	V
Digital low-level input voltage, V_{IL}		–	–	0.8	V

5.4.2 Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V_{3P3} –0.4	–	–	V
	I_{LOAD} = 10 mA	V_{3P3}- 0.6	–	–	V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0	–	0.4	V
	I_{LOAD} = 10 mA	–	–	0.5	V

5.4.3 Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V_{3P3D} and V_{3P3A} current (compounded)	Normal Operation, $\mathbf{V_{3P}}$=3.3V.	–	8.1	10.3	mA

5.4.4 Crystal Oscillator

Parameter	Condition	Min	Typ	Max	Unit
XIN to XOUT Capacitance		–	3[1]	–	pF
Capacitance to GND XIN XOUT		–	 5[1] 5[1]	–	 pF pF

[1] Guaranteed by design, not subject to test.

5.4.5 Internal RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Nominal Frequency		–	20.000	–	MHz
Accuracy		–	±1.5	–	%

5.4.6 ADC Converter, V_{3P3} Referenced

LSB values do not include the 9-bit left shift at EMP input.

Parameter	Condition	Min	Typ	Max	Unit
Usable Input Range (Vin-V_{3P3})		-250	–	250	mV peak
THD (First 10 harmonics)	Vin=65 Hz, 64 kpts FFT, Blackman-Harris window	–	-85	–	dB
Input Impedance	Vin=65 Hz	30	–	90	kΩ
Temperature coefficient of Input Impedance	Vin=65 Hz	–	1.7[1]	–	Ω/°C
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\ 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	Vin=200 mV pk, 65 Hz V_{3P3}=3.0V, 3.6V	–	–	**50**	ppm/%
Input Offset (Vin-V_{3P3})		-10		10	mV

[1] Guaranteed by design, not subject to test.

5.5 Timing Specifications

5.5.1 RESET

Parameter	Condition	Min	Typ	Max	Unit
Reset pulse fall time		–	1[1]	–	µs
Reset pulse width		–	5[1]	–	µs

[1] Guaranteed by design, not subject to test.

5.5.2 SPI Slave Port

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	SPCK cycle time		1	–	–	µs
$t_{SPILead}$	Enable lead time		15	–	–	ns
t_{SPILag}	Enable lag time		0	–	–	ns
t_{SPIW}	SPCK pulse width: High Low		 250 250	–	–	 ns ns
t_{SPISCK}	SSB to first SPCK fall	Ignore if SPCK is low when SSB falls.	–	2[1]	–	ns
t_{SPIDIS}	Disable time		–	0[1]	–	ns
t_{SPIEV}	SPCK to Data Out (SDO)			–	25	ns
t_{SPISU}	Data input setup time (SDI)		10	–	–	ns
t_{SPIH}	Data input hold time (SDI)		5	–	–	ns

[1] Guaranteed by design, not subject to test.

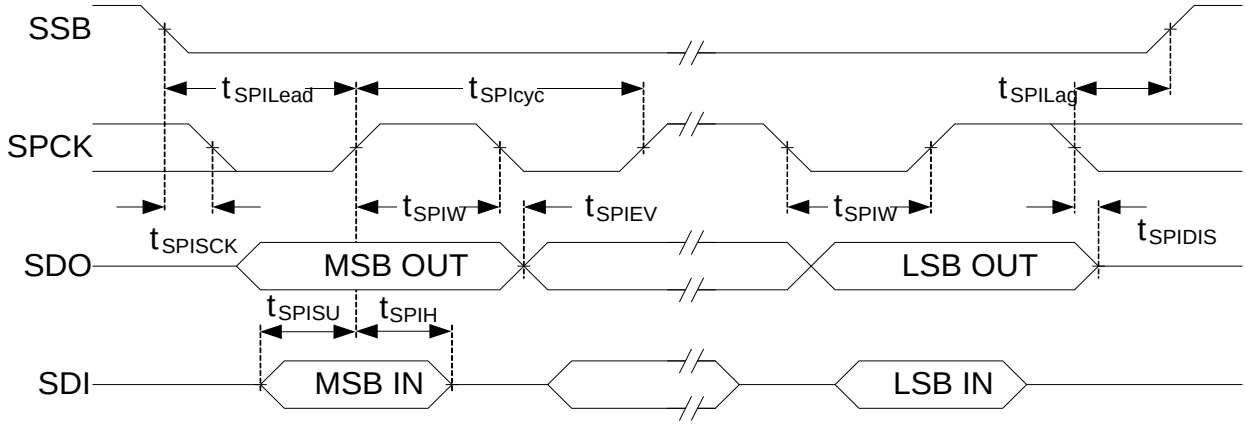


Figure 22: SPI Slave Port Timing

5.5.3 I²C Slave Port

Table 21: I²C Slave Port Timing[2]

Parameter	Condition	Min	Typ	Max	Unit
t_{BUF} Bus Idle (Free) time between transmissions (Stop/Start)		1500	-	–	ns
t_{ICF} I²C input Fall Time		20[1]	–	300	ns
t_{ICR} I²C input Rise Time		20[1]	–	300	ns
t_{STH} I²C Start or repeater Start condition hold time		500	–	–	ns
t_{STS} I²C Start or repeater Start condition setup time		600	–	–	ns
t_{SCH} I²C clock high time		600	–	–	ns
t_{SCL} I²C clock low time		1300	–	–	ns
t_{SDS} I²C serial data setup time		100	–	–	ns
t_{SDH} I²C serial data hold time		10	–	–	ns
t_{VDA} I²C Valid data time: - SCL low to SDA output valid - ACK signal from SCL low to SDA (out) low		–	–	900	ns

Notes:

[1] Dependent on bus capacitance.

[2] Guaranteed by design, not subject to test.

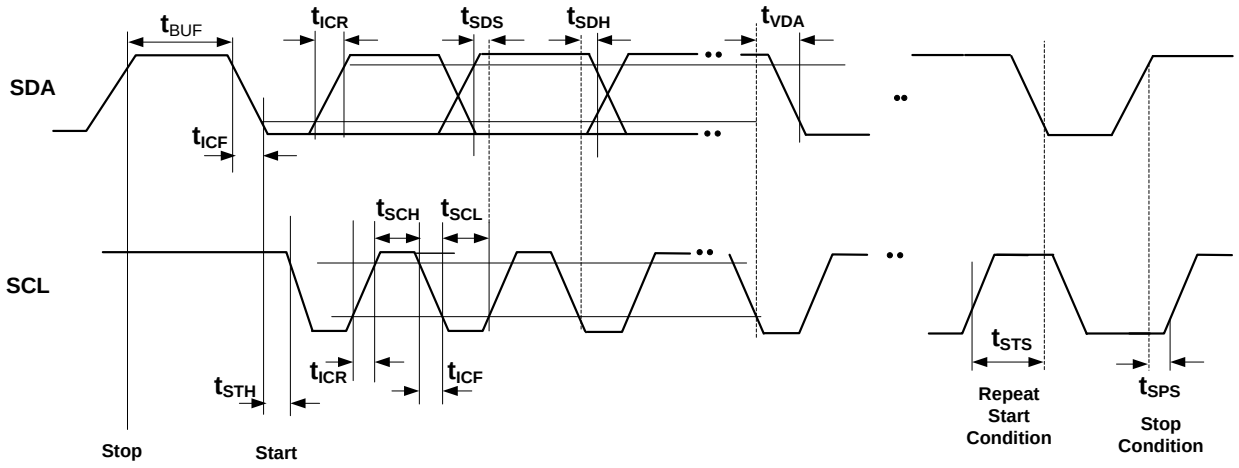
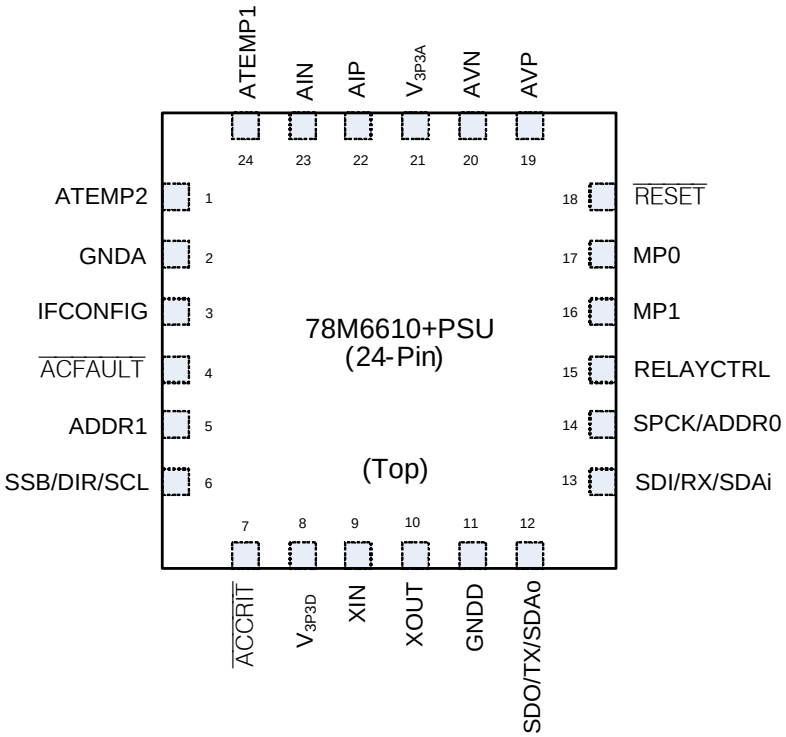


Figure 23: I²C (Slave) Port Timing

6 Packaging

6.1 24-pin QFN Pinout

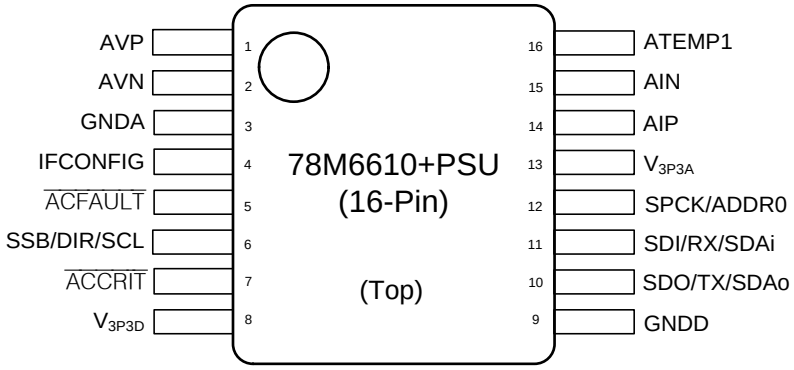


Pin	Signal	Function	Pin	Signal	Function
1	ATEMP2	Thermistor 2 input	13	SDI/RX/SDAi	SPI DATA IN / UART RX/ I^2C Data In
2	GNDA	GROUND (Analog)	14	SPCK/ADDR0	SPI CLOCK IN / I^2C/Multi-Point UART Address (1)
3	IFCONFIG	UART/SPI (1=UART; 0=SPI) (1)	15	RELAYCTRL	Relay Control Output
4	$\overline{\text{ACFAULT}}$	ACFAULT Alarm	16	MP0	Multi-Purpose Digital I/O
5	ADDR1	I^2C/Multi-Point UART Address (1)	17	MP1	Multi-Purpose Digital I/O
6	SSB/DIR/SCL	Slave Select (SPI) / RS485 TX-RX / I^2C Serial Clock (1)	18	$\overline{\text{RESET}}$	Reset Input
7	$\overline{\text{ACCRIT}}$	AC Voltage Alarm (Critical)	19	AVP	Voltage Input (positive)
8	V_{3P3D}	3.3VDC Supply (Digital)	20	AVN	Voltage Input (negative)
9	XIN	Crystal Oscillator Driver Input	21	V_{3P3A}	3.3VDC Supply (Analog)
10	XOUT	Crystal Oscillator Driver Output	22	AIP	Current Input (positive)
11	GNDD	GROUND (Digital)	23	AIN	Current Input (negative)
12	SDO/TX/SDAo	SPI DATA OUT/ UART TX/ I^2C Data Out	24	ATEMP1	Thermistor 1 input

Notes:

1) Pin is sampled after power-on or reset to select/configure the communication peripheral

6.2 16-Pin TSSOP Pinout



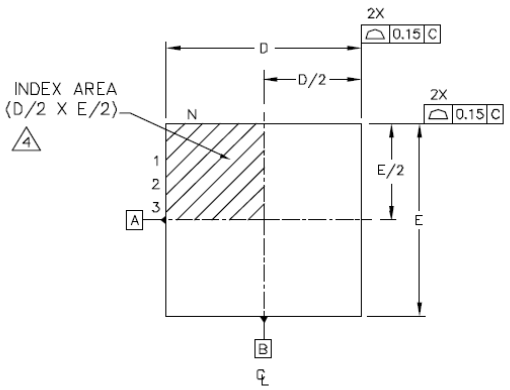
Pin	Signal	Function	Pin	Signal	Function
1	AVP	Voltage Input (positive)	9	GNDD	GROUND (Digital)
2	AVN	Voltage Input (negative)	10	SDO/TX/SDAo	SPI DATA OUT/ UART TX/ I^2C Data Out
3	GNDA	GROUND (Analog)	11	SDI/RX/SDAi	SPI DATA IN / UART RX/ I^2C Data In
4	IFCONFIG	UART/SPI (1=UART/I^2C; 0=SPI) (1)	12	SPCK/ADDR0	SPI CLOCK IN / I^2C/Multi-Point UART Address (1)
5	$\overline{\text{ACFAULT}}$	ACFAULT Alarm	13	V_{3P3A}	3.3VDC Supply (Analog)
6	SSB/DIR/SCL	Slave Select (SPI) / RS485 TX-RX / I^2C Serial Clock (1)	14	AIP	Current Input (positive)
7	$\overline{\text{ACCRIT}}$	AC Voltage Alarm (Critical)	15	AIN	Current Input (negative)
8	V_{3P3D}	3.3VDC Supply (Digital)	16	ATEMP1	Thermistor 1 input

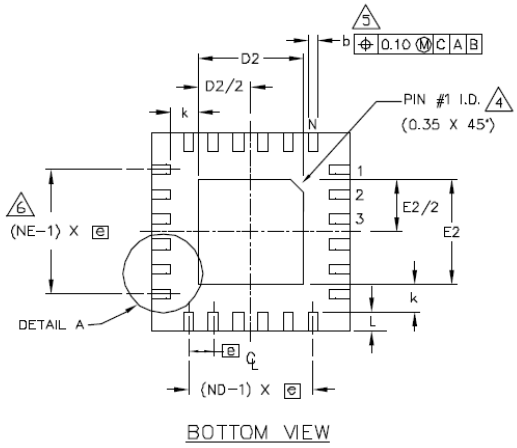
Notes:

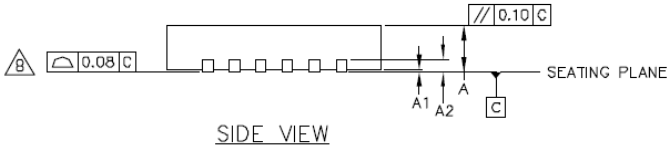
1) Pin is sampled after power-on or reset to select/configure the communication peripheral

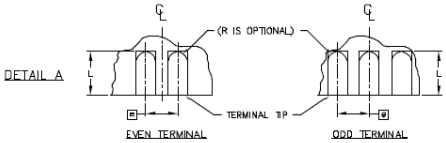
6.3 Package Outline

QFN-24 Package



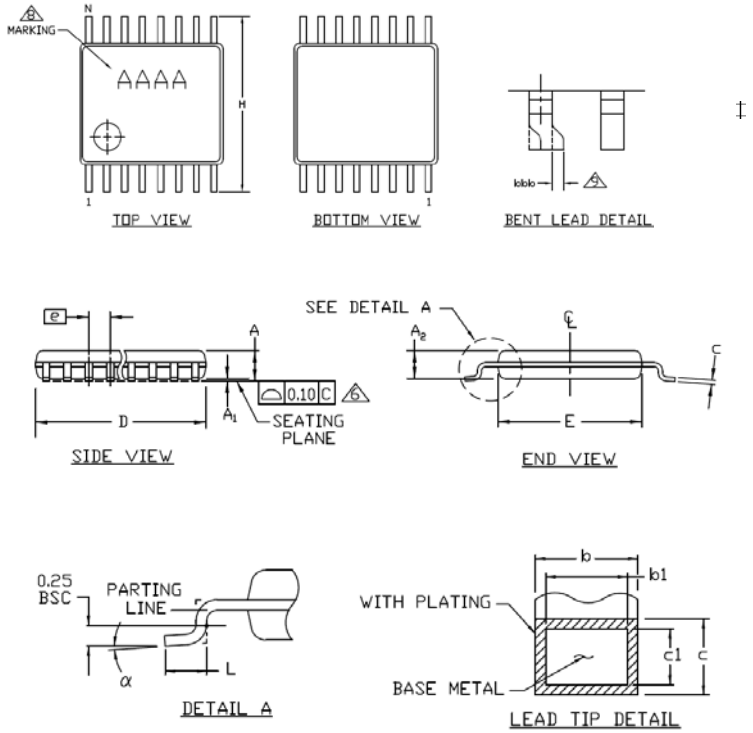






PKG	24L 4x4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2	0.20 REF		
b	0.18	0.23	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.50 BSC.		
k	0.25	–	–
L	0.30	0.40	0.50
N	24		
ND	6		
NE	6		
Jedec Var.	WGGD-2		

TSSOP-16 Package



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	4.90	5.10	.193	.201
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
bbb	0.10 MAX			

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.
10. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PBFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

7 Ordering Information

Part	Package	Option	Ordering Number	IC Marking
78M6610+PSU	QFN-24	Bulk	78M6610+PSU/B00	EMP
		Tape & Reel	78M6610+PSU/B00T	
	TSSOP-16	Bulk	78M6610+PSU/C00	
		Tape & Reel	78M6610+PSU/C00T	

8 Contact Information

For more information about the 78M6610+PSU or other Maxim Integrated products, contact technical support at **www.maximintegrated.com/support**.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	2/13	Revised pin description, RC Oscillator Specification, X+Y capacitor calibration, and accumulation interval description	7, 12, 13, 19, 20, 40, 45, 54, 55, 58, 59

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