BUILT ON Power

QorIQ Multicore Processor Development

QorIQ P5040 Development System

Overview

The P5040DS-PA is a flexible development system based on the dual-core 32/64-bit moded P5040 device. The board, with its 2.2 GHz P5040 and rich I/O mix, is intended for evaluation of the QorIQ P5040/P5021processor in networking, telecom and industrial applications, where its high-performance, high-efficiency core and integration make it very well suited as a control plane processor.

The P5040 development system, which exercises most capabilities of the P5040 processor, can serve as a reference for the customer's own hardware development, as a debug tool to check behaviors on the board compared to behaviors seen on customer boards or be used for software development and performance evaluation prior to completion of the customer's own board.

The P5040/P5021 processor is based upon the e5500mc core, built on Power Architecture®, offering speeds of 1.8 to 2.4 GHz. It has a three-level cache hierarchy with 32 KB of instruction and data cache per core, 512 KB of unified backside L2 cache per core, and 2 MB of shared frontside CoreNet platform cache fronting the dual memory controllers. The processor's I/O includes 20 SerDes lanes running at up to 5 GHz, multiplexed across three PCI Express® gen. 2.0 controllers, two 10 GE XAUI interfaces, four 1 GbE SGMII interfaces, four 2.5 Gb/s SGMII interfaces, two SATA 2.0 interfaces and the high-speed Aurora debug interface. It has a 64-bit DDR3 and DDR3L (low power) DRAM interface with 8-bit ECC support running at up to 1600 MHz data rate. It includes two USB 2.0 interfaces (including PHY), two DUARTs, an SD/MMC interface, a 32-bit local bus, four I^2C and SPI. It also includes the accelerator blocks collectively known as the data path acceleration architecture (DPAA) that offload various tasks from the core, including routine packet handling and security algorithm calculation as well as support for RAID 5/6 hardware assist.

The P5040DS has significant flexibility in allocation of its 20 SerDes lanes to various functions. Its base configuration supports two RGMII ports, two PCI Express x2 slots (two lanes to each slot), 4 x 4 slots for the optional Freescale SGMII-PEX-RISER, a 2 x 4 slot for the optional Freescale XAUI-RISER, the Aurora high-speed debug port and two SATA ports. It can also be configured to support one PCI Express slot of widths up to x8.

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The dual memory controllers of the P5040DS support 4 GB of DDR3 at 1600 MHz. It has 128 MB of NOR flash, 1 GB NAND flash, a 256 KB IC EEPROM and two SPI memories: 16 MB flash and 128 KB EEPROM. It also has two USB 2.0 receptacles and an SD card slot.

The P5040DS is pre-loaded with a software development kit with support for DPAA, including SMP Linux® kernel, Hugetlbfs for applications with a large memory footprint, user space DPAA for high-performance packet handling, u-boot and a GCC toolchain.

P5040DS Board Features

Processor

- P5040, 2.2 GHz core with 1600 MHz DDR3 data rate
- Multiple SysClk inputs for generating various device frequencies

Memory

- Dual unbuffered DDR3 240-pin uDIMM modules with ECC (72-bit bus), 4 GB memory, 1600 MHz data rate
- 128 MB NOR flash
- 1 GB NAND flash
- SPI-based 128 MB flash
- SPI-based 128 KB EEPROM
- SD connector to interface with an SD memory card

PCI Express

- Two x2 PCI Express slots
- Can support the Freescale XAUI-RISER and SGMII-PEX-RISER option cards

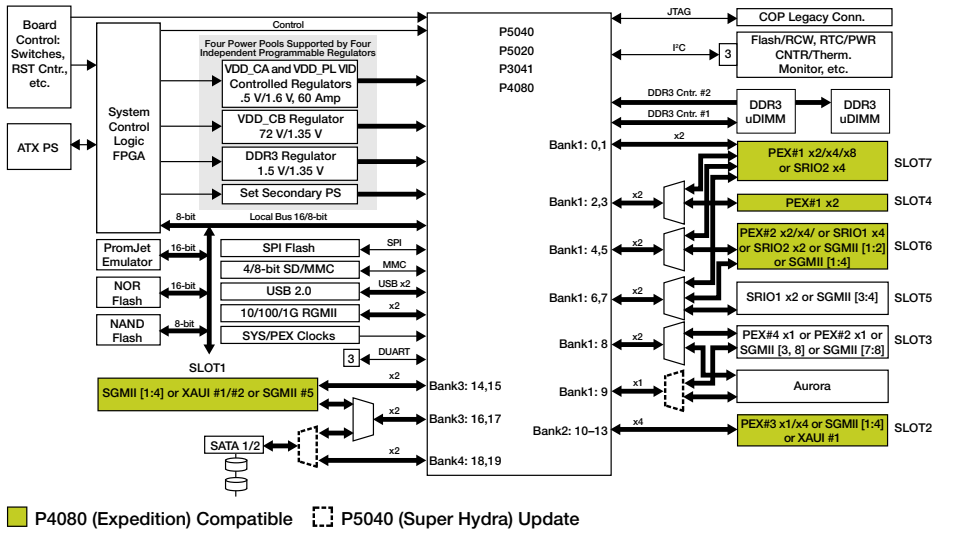
SATA

- Two vertical SATA connectors

USB 2.0

- Two High-Speed USB controllers
- One Type A and one MicroAB receptacle

P5040DS-PA Block Diagram



Ethernet

- Support two 10/100/1000 ports with no add-in cards
- dTSEC4 and dTSEC5 as RGMII to Vitesse VSC8244 PHY
- Optional SGMII-PEX-RISER expands 10/100/1000 port count to five
- 10 GE supported with optional XAUI-RISER card

DUART

- Two DUARTs

Debug

- JTAG/COP
- Aurora high-speed connector

Other

- IEEE® 1588 connector for Symmetricom option card
- Temperature sensor
- Eight general-purpose I/Os

For more information, visit freescale.com/QorIQ

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