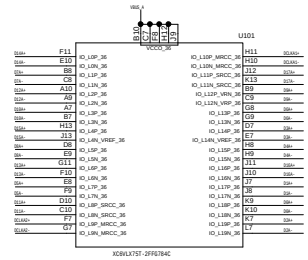
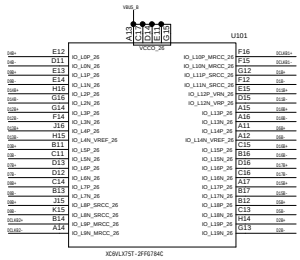
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1		APR-2011	

PARALLEL DATA BUS A AND B



DATA DIFF PAIRS CAN BE MOVED TO HELP ROUTING
DO NOT MOVE CLOCK DIFF PAIRS

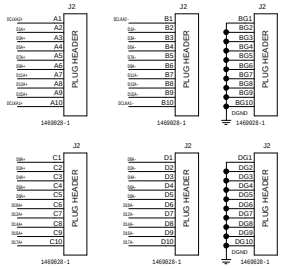


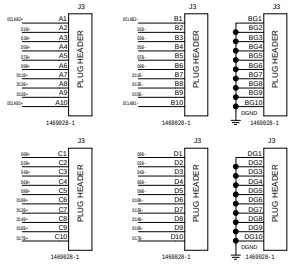
DATA DIFF PAIRS CAN BE MOVED TO HELP ROUTING
DO NOT MOVE CLOCK DIFF PAIRS

DIFF PAIR ROUTING LENGTHS MUST BE MATCHED TO WITHIN 50 MILS

BUS ROUTING LENGTHS MUST BE MATCHED TO WITHIN 250 MILS

NOTE: J1 IS ON SHEET 10



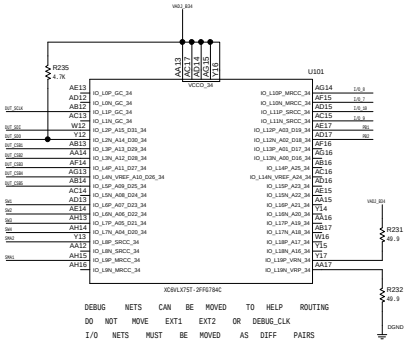


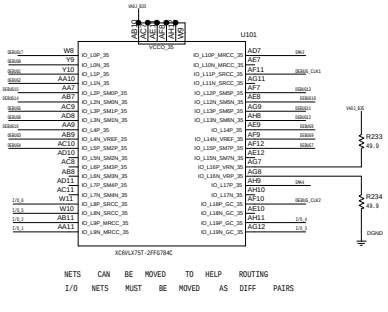
HADV6-REVD

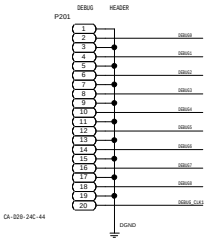
ANALOG DEVICES	SCHEMATIC	
	HADV6 <PRODUCT_1>	
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. - REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 1 OF 17

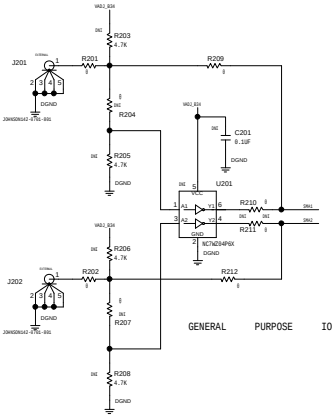
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

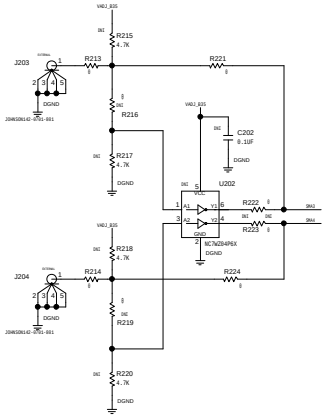
MISC. BANKS 34 AND 35

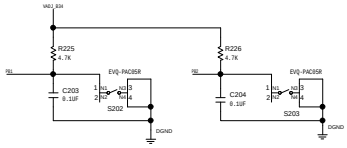


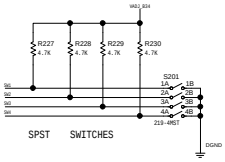


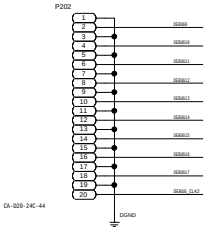








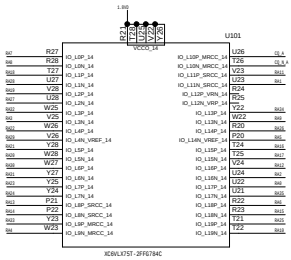


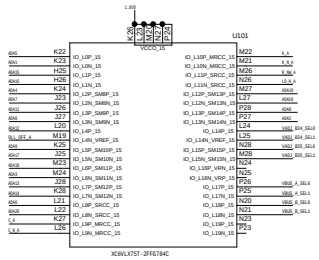


ANALOG DEVICES	SCHEMATIC		
	HADVE <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE> SHEET 2 OF 17

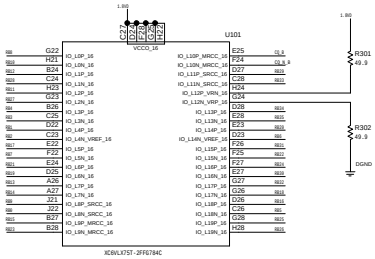
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

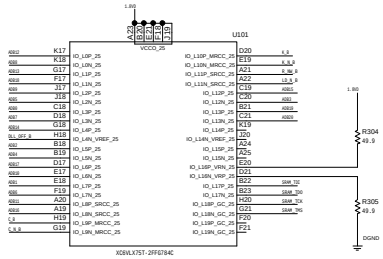
FPGA - SRAM INTERFACE AND BANK CONTROLS





RA, RB AND AD LINES CAN BE MOVED WITHIN BANKS TO HELP ROUTING
ASK ENGINEER BEFORE MOVING ANY OTHER LINES





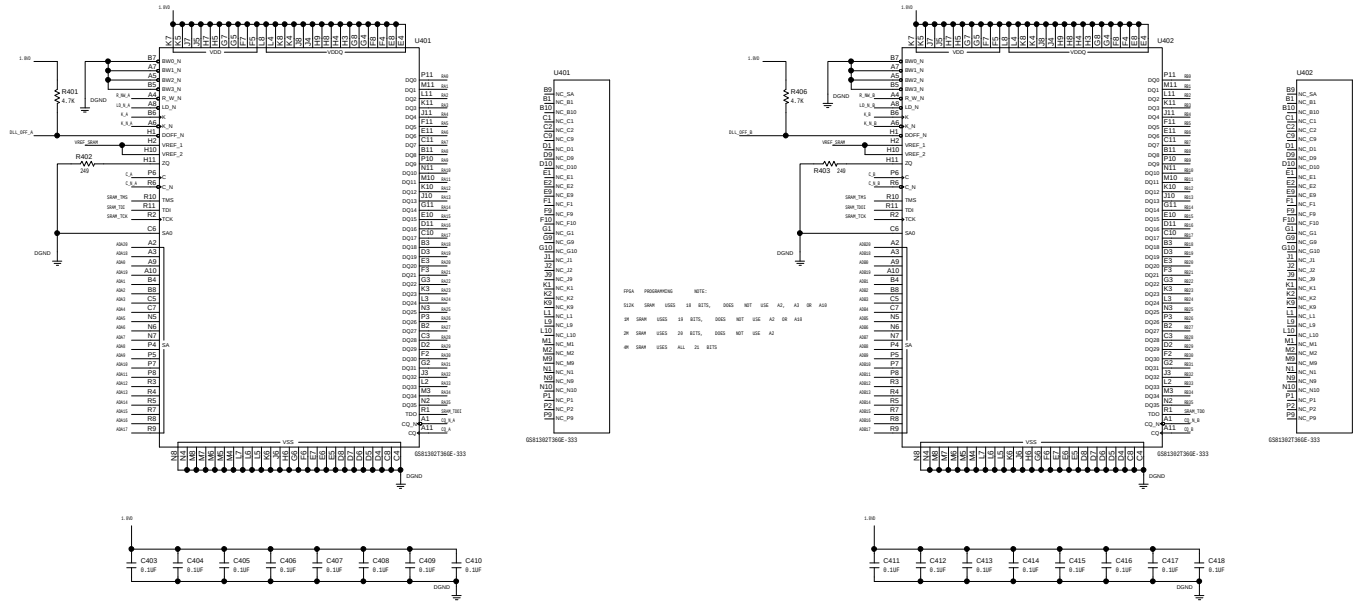
ANALOG DEVICES

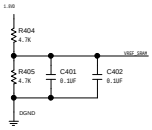
SCHEMATIC

MADVB <PRODUCT_1>			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -		REV D
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 3 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SRAM A AND B





PLACE ONE SRAM CHIP ON TOP SIDE

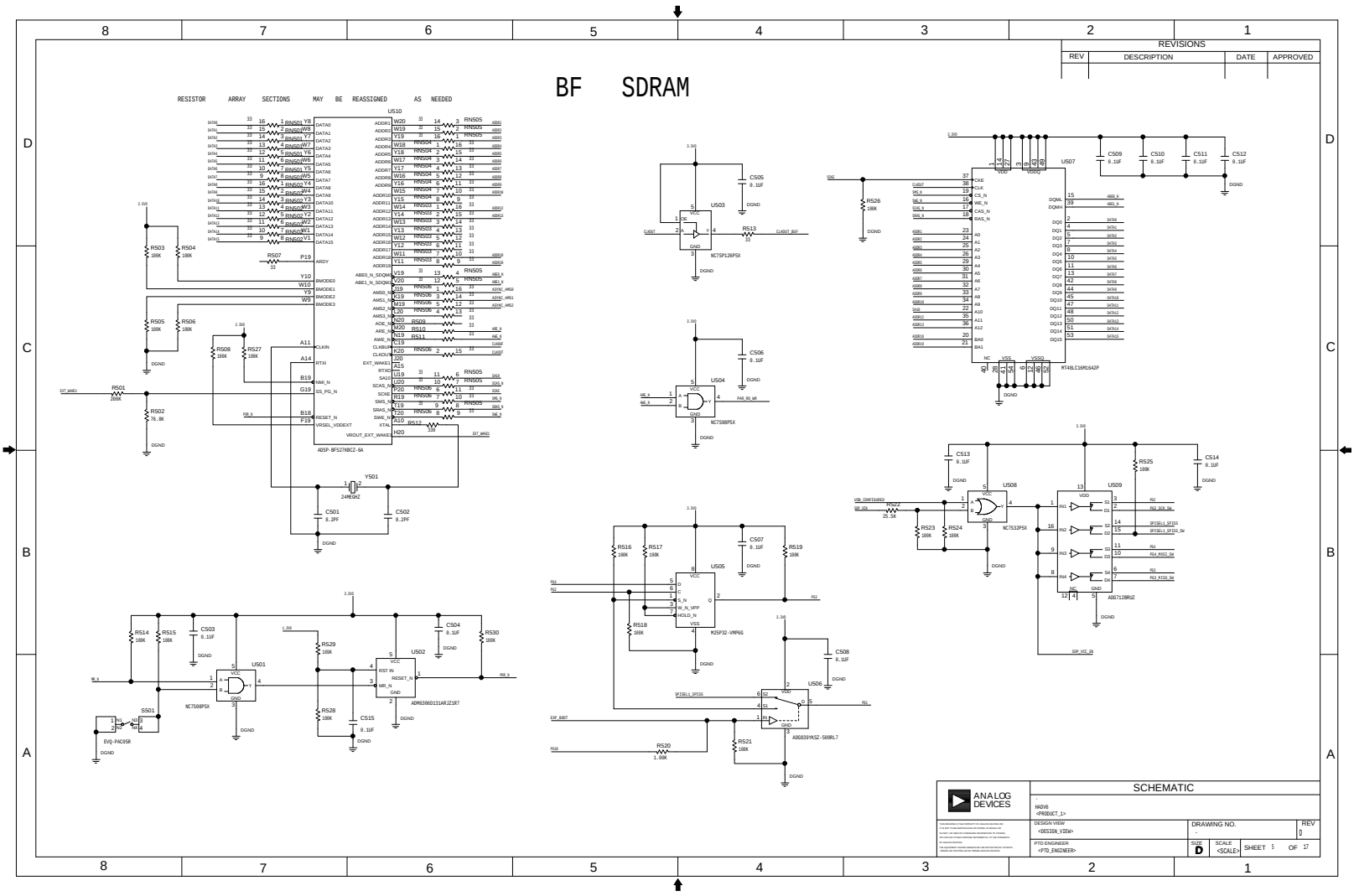
PLACE THE OTHER SRAM CHIP ON BOTTOM SIDE

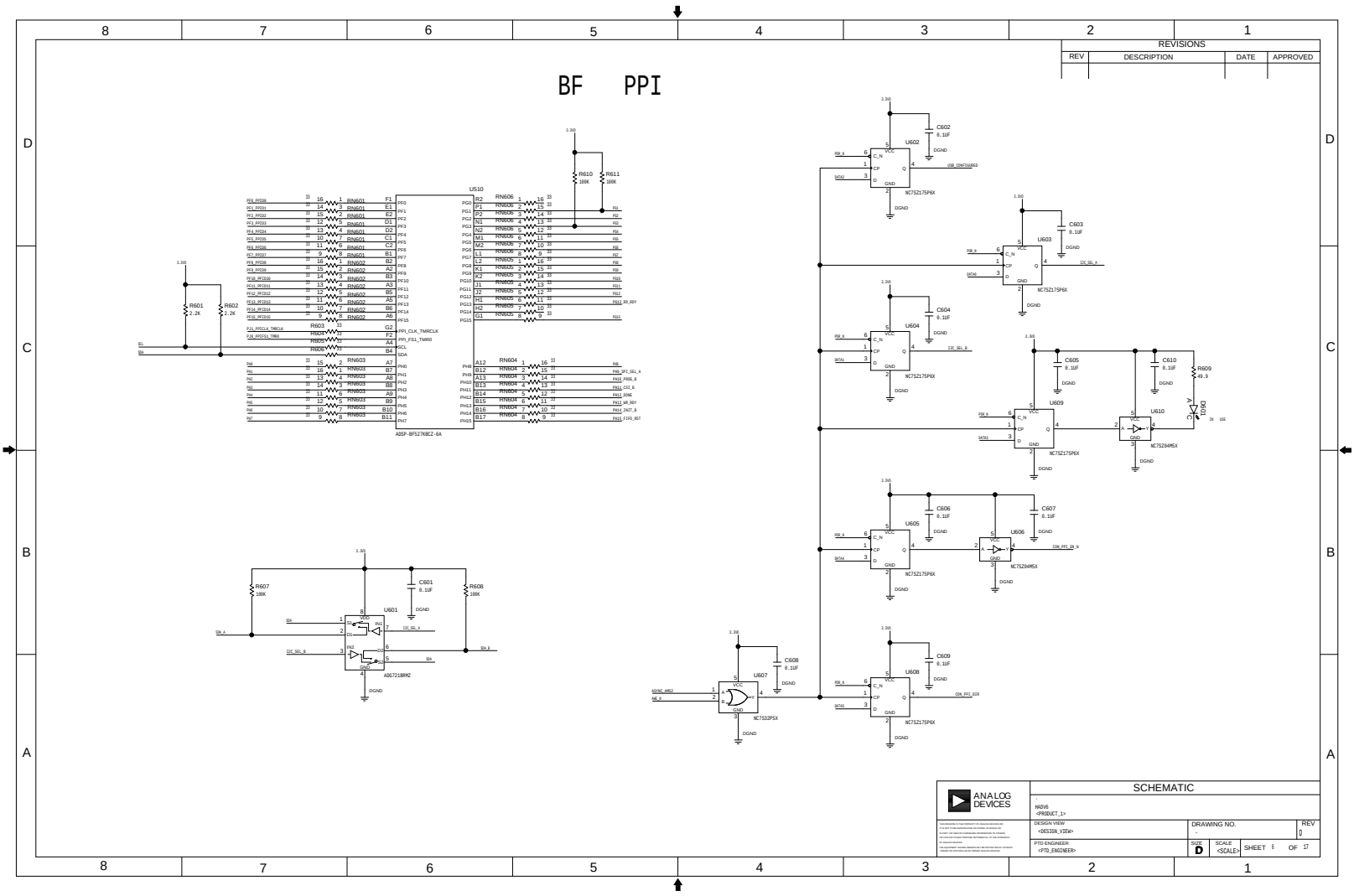
ADDRESS LINES ARE SHARED

K AND K_N LINES ARE SHARED

C AND C_N LINES ARE SHARED

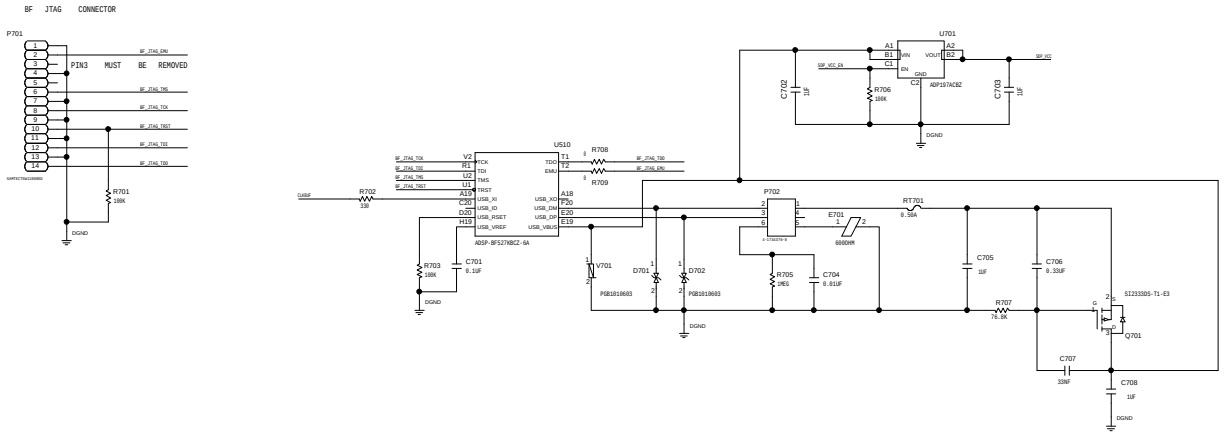
ANALOG DEVICES	SCHEMATIC		
	HADVS <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE> SHEET 4 OF 17

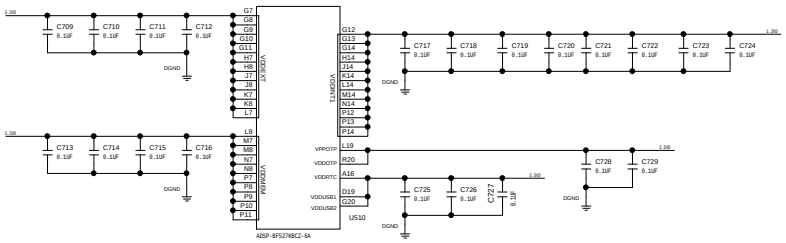


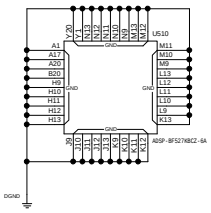


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

BF POWER,USB AND JTAG



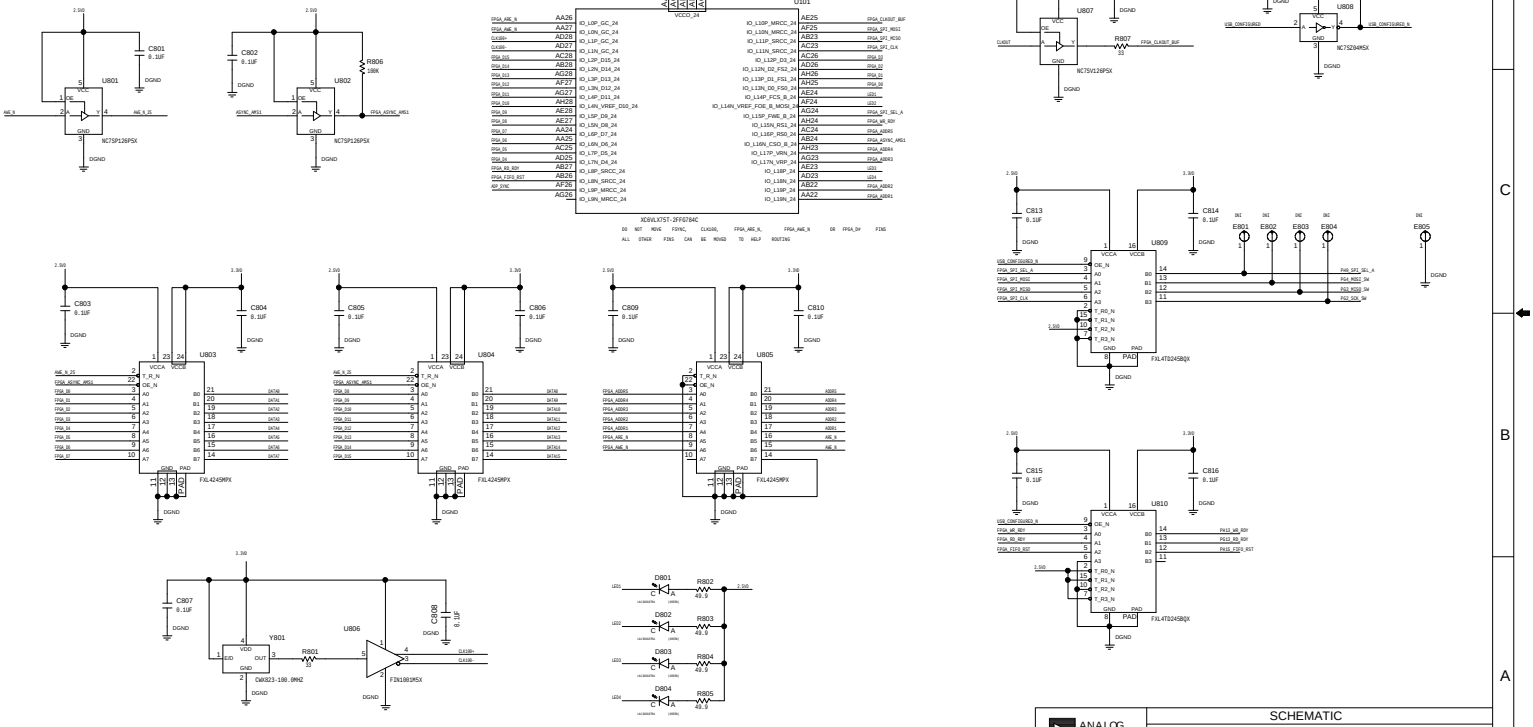




ANALOG DEVICES	SCHEMATIC
	HADVE <PRODUCT_1>
	DESIGN VIEW <DESIGN_VIEW>
	DRAWING NO. -
	REV D
	PTD ENGINEER <PTD_ENGINEER>
	SIZE D
	SCALE <SCALE>
	SHEET 7 OF 17

FPGA - BF INTERFACE, MISC

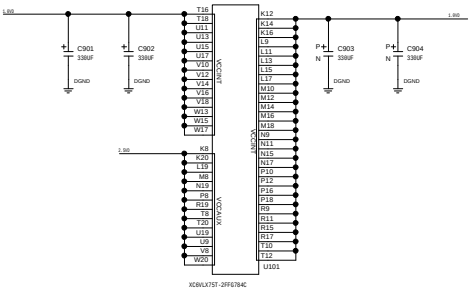
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

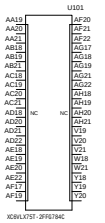


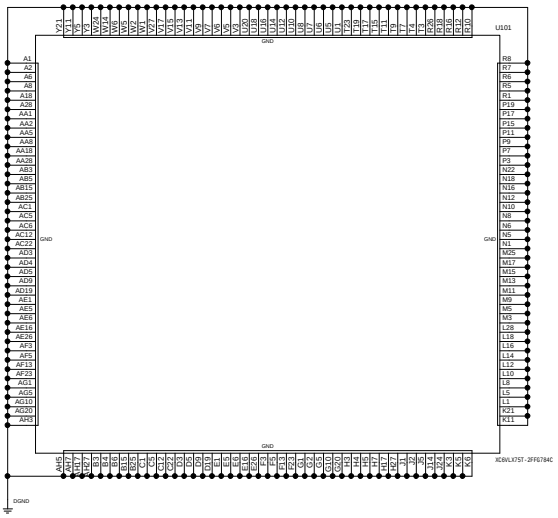
ANALOG DEVICES	SCHEMATIC
	HADVE
	<PRODUCT_1>
DESIGN VIEW	<DESIGN_VIEW>
PTD ENGINEER	<PTD_ENGINEER>
DRAWING NO.	-
REV	D
SIZE	D
SCALE	<SCALE>
SHEET	8 OF 17

FPGA POWER AND DECOUPLING

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



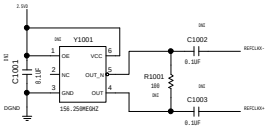


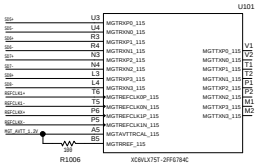


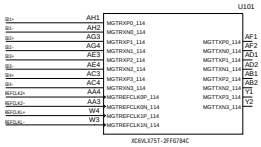
ANALOG DEVICES	SCHEMATIC	
	MADVE <PRODUCT_1>	
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. - REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 9 OF 17

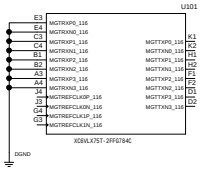
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

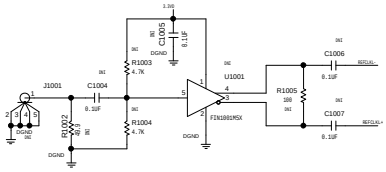
GTX CONNECTIONS











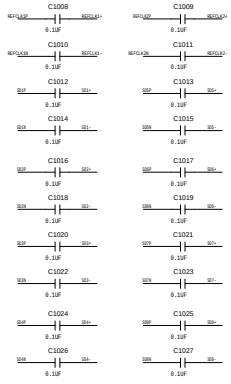
SD DIFF PAIRS MAY BE MOVED TO HELP ROUTING

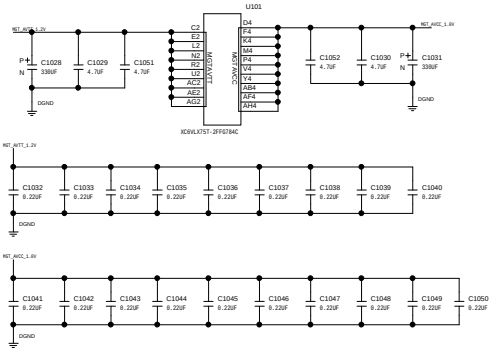
DO NOT CROSS BANKS

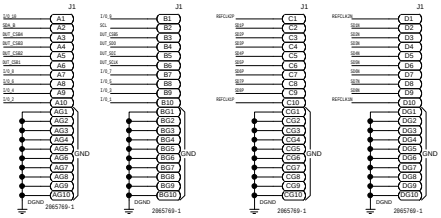
DIFF PAIR TRACE LENGTHS MUST BE MATCHED TO WITHIN 10 MILS

DIFF PAIR LANE LENGTHS MUST BE MATCHED TO WITHIN 100 MILS

TRACE LENGTHS BETWEEN R1006 AND FPGA MUST BE EQUAL IN LENGTH AND GEOMETRY



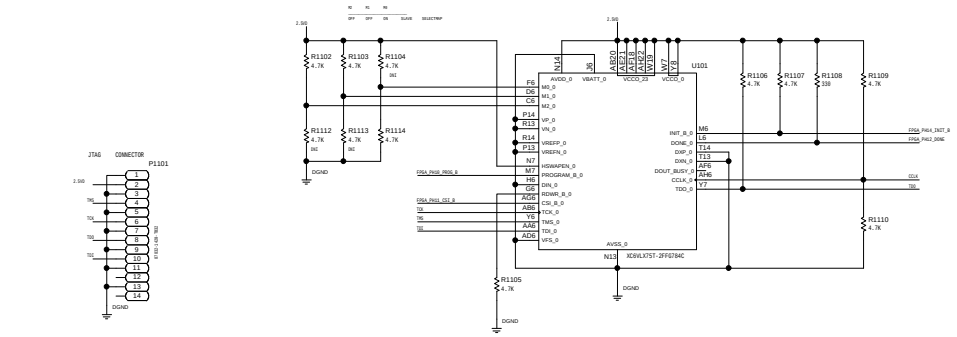




ANALOG DEVICES	SCHEMATIC		
	HADVB <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE> SHEET 10 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

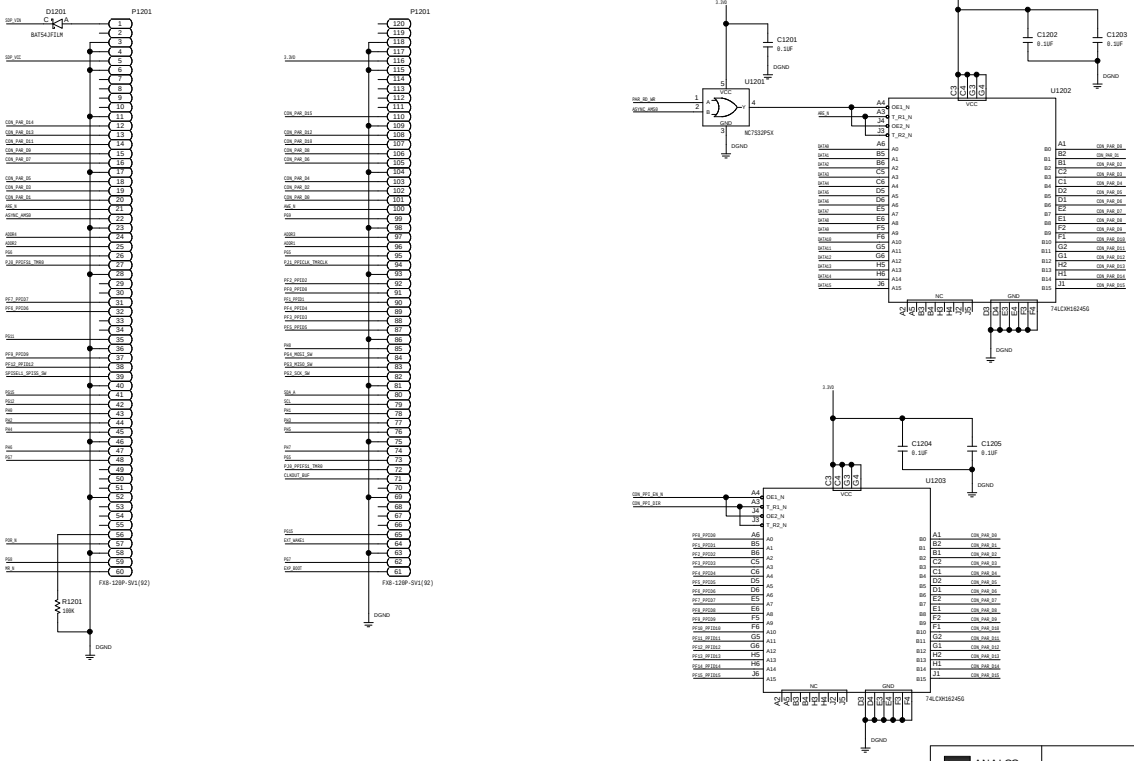
FPGA CONFIGURATION



ANALOG DEVICES	SCHEMATIC		
	MADVE <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV 0
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 11 OF 17	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

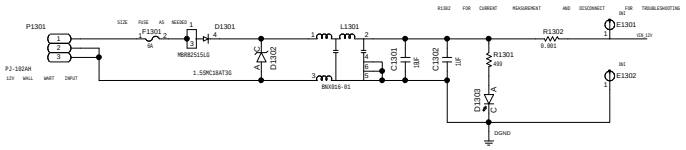
SDP CONNECTOR

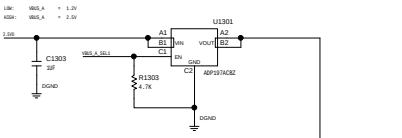


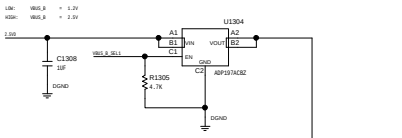
ANALOG DEVICES	SCHEMATIC		
	MADVS <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV 0
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 12 OF 17	

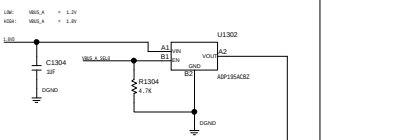
POWER SUPPLY INPUT AND CONTROLS

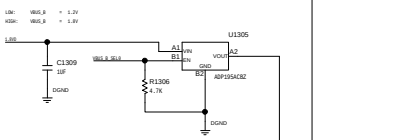
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

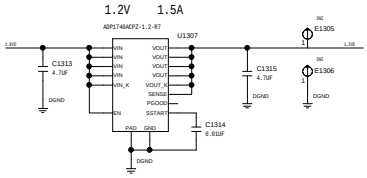


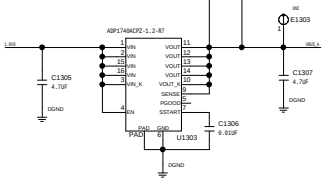


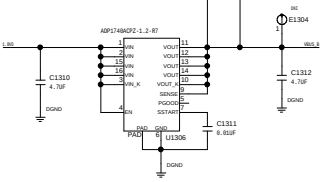












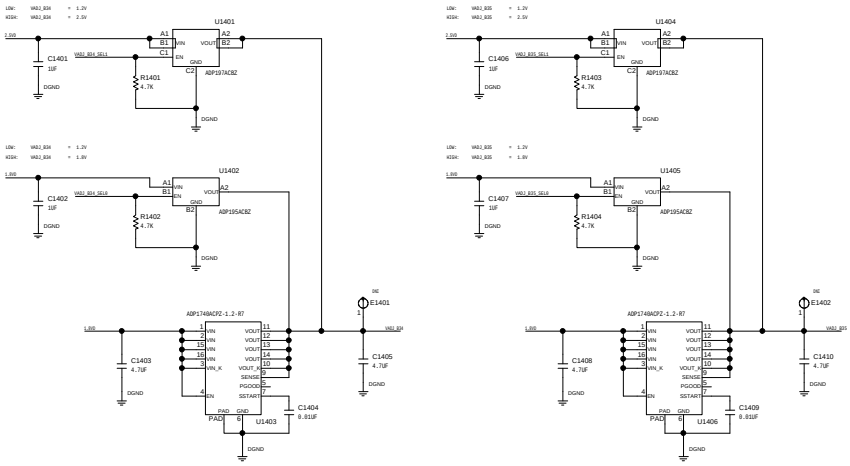
ANALOG DEVICES

SCHEMATIC

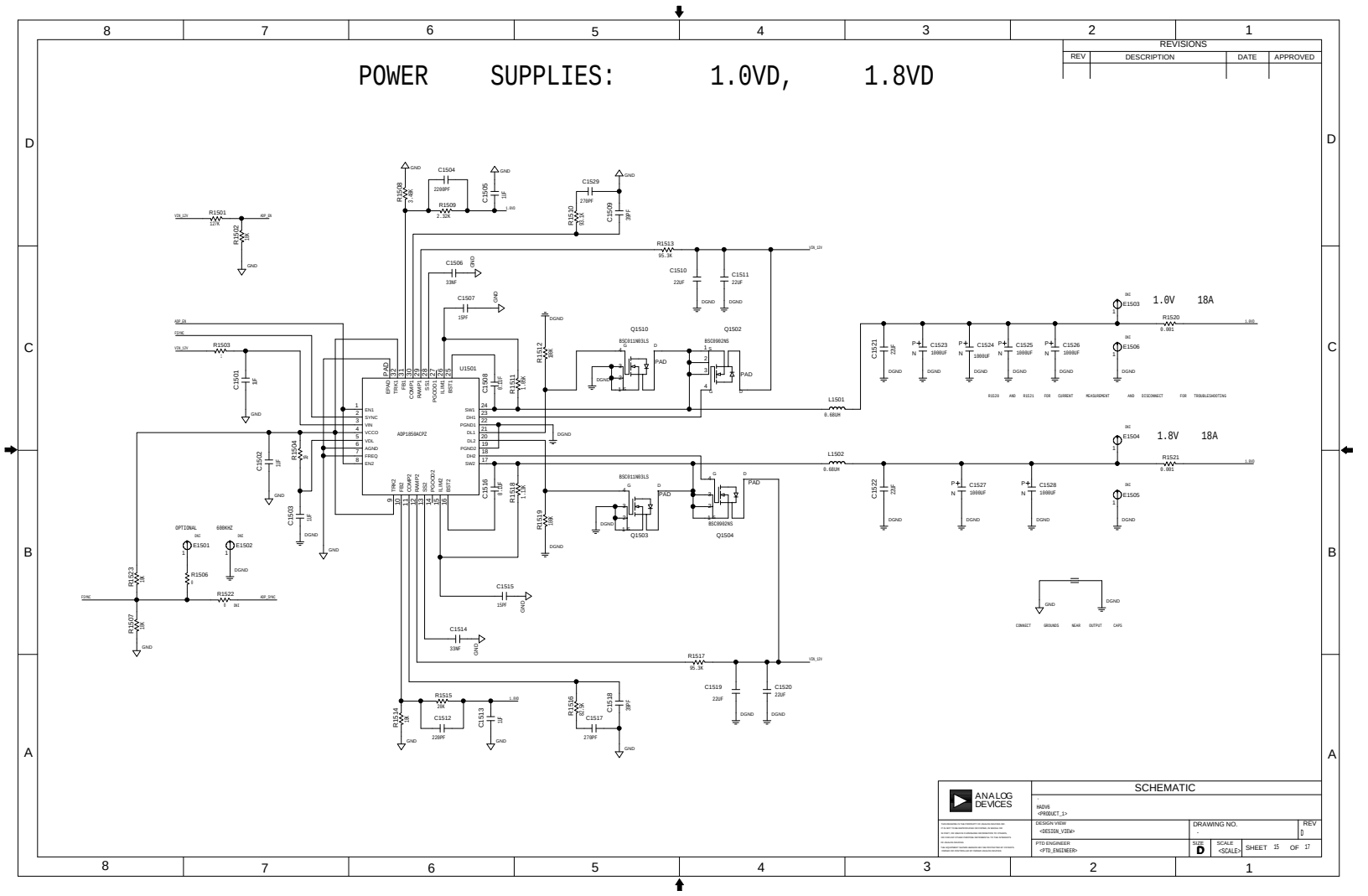
MADVB <PRODUCT_1>			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -		REV 0
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>	SHEET 13 OF 17

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

POWER SUPPLY CONTROLS

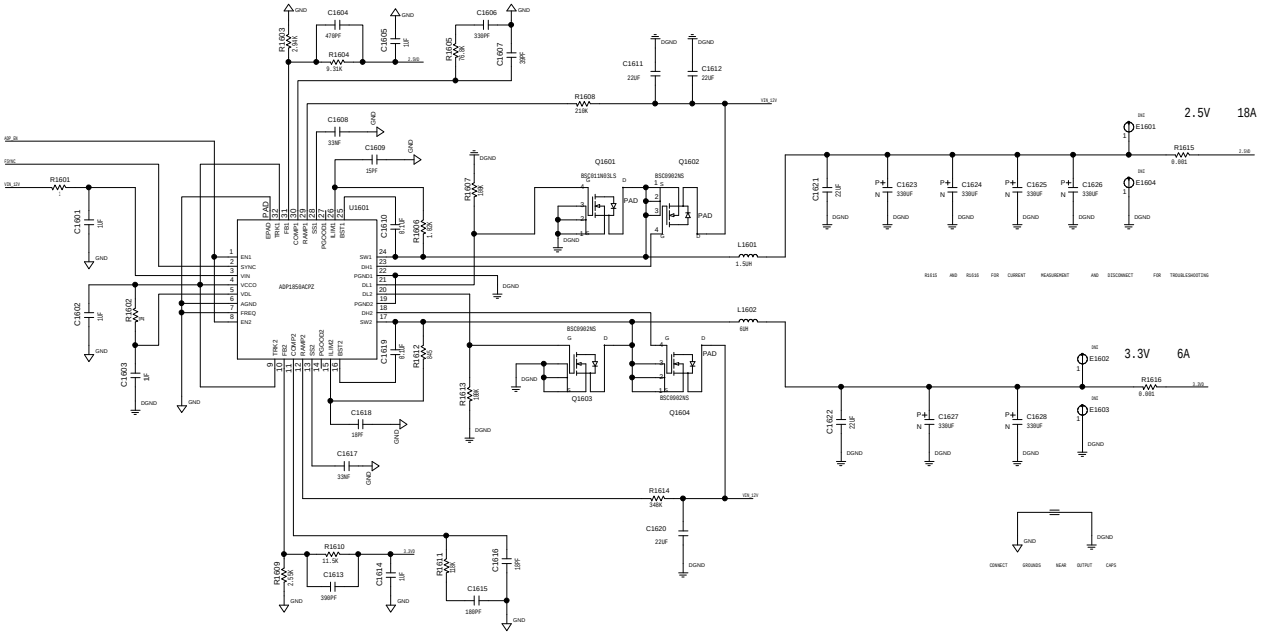


ANALOG DEVICES	SCHEMATIC	
	HADVS <PRODUCT_1>	
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. - REV 0
	PTD ENGINEER <PTD_ENGINEER>	SIZE D SCALE <SCALE> SHEET 14 OF 17



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

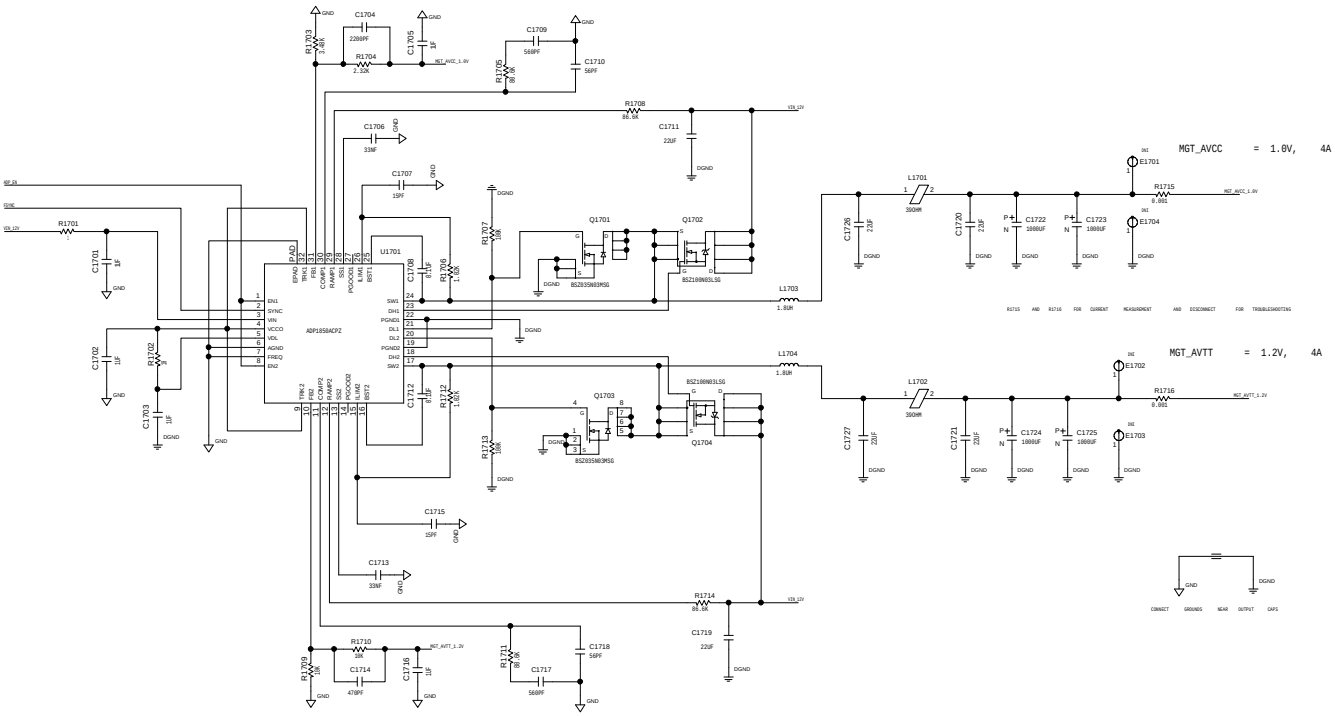
POWER SUPPLIES: 2.5VD, 3.3VD



ANALOG DEVICES	SCHEMATIC		
	HADVE <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV D
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE> SHEET 16 OF 17

GTX POWER SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



ANALOG DEVICES	SCHEMATIC		
	HADVS <PRODUCT_1>		
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. -	REV 0
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE <SCALE>
		SHEET 17 OF 17	