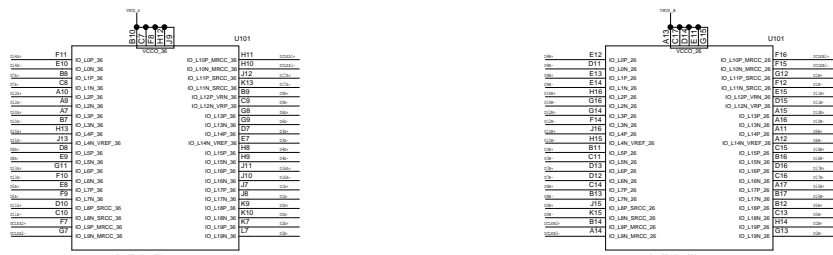


# PARALLEL DATA BUS A AND B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
1		09-2011	



DATA DIFF PAIRS CAN BE MOVED TO HELP ROUTING  
DO NOT MOVE CLOCK DIFF PAIRS

DIFF PAIR ROUTING LENGTHS MUST BE MATCHED TO WITHIN 50 MILS  
BUS ROUTING LENGTHS MUST BE MATCHED TO WITHIN 250 MILS

NOTE: J1 IS ON SHEET 10

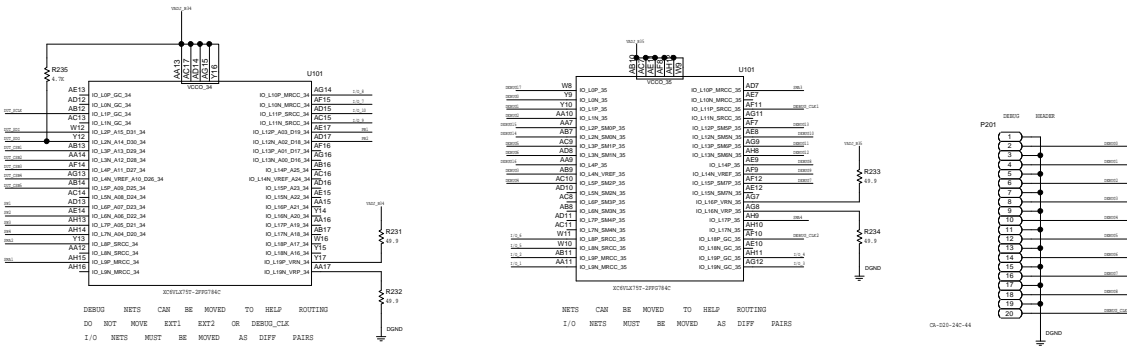


## HADV6-REVD

ANALOG DEVICES		SCHEMATIC	
REV	DESCRIPTION	DRAWING NO.	REV
1	HADV6-REVD	1000000000	D
PTD ENGINEER		SIZE	SCALE
+PTD_0000000000		D	SCALE
		SHEET	OF
		1	11

# MISC. BANKS 34 AND 35

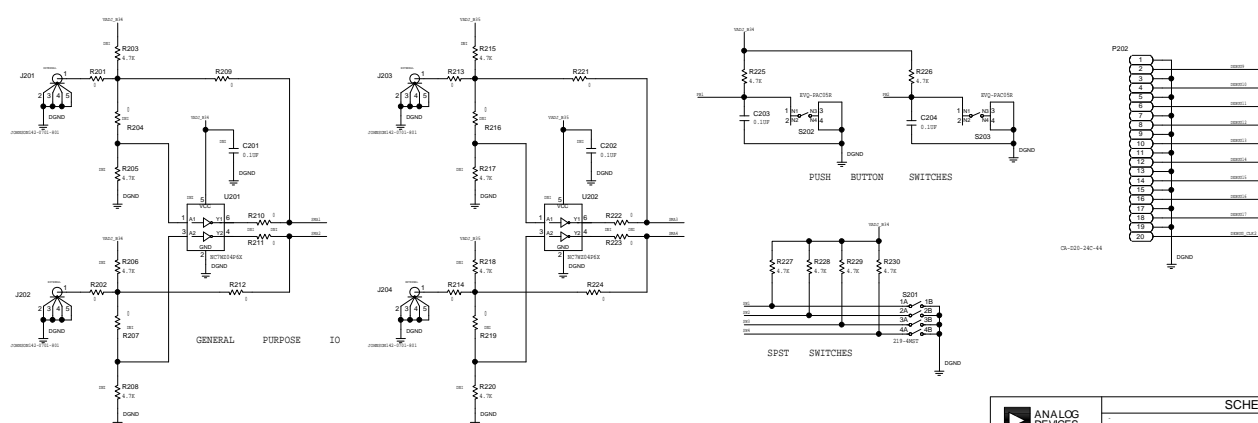
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



DEBUG NETS CAN BE MOVED TO HELP ROUTING  
DO NOT MOVE EXT1, EXT2 OR DEBUG\_CLK  
I/O NETS MUST BE MOVED AS DIFF PAIRS

NETS CAN BE MOVED TO HELP ROUTING  
I/O NETS MUST BE MOVED AS DIFF PAIRS

DS-020-240-44



GENERAL PURPOSE IO

PUSH BUTTON SWITCHES

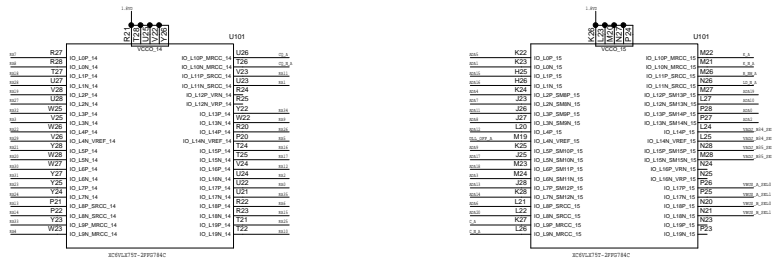
SPST SWITCHES

DS-020-240-44

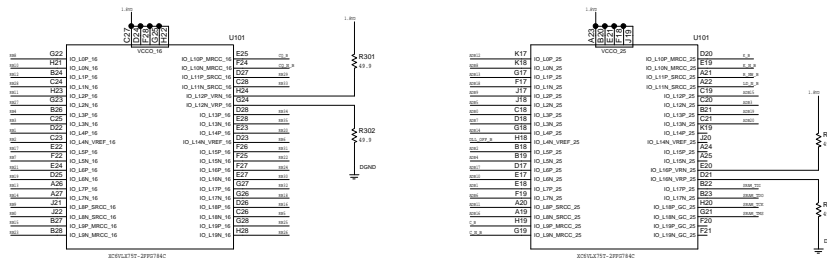
	SCHEMATIC		
	DS020 @PROJECT_1_3	DRAWING NO.	REV
	DESIGNER: <DESIGN_V123> PTD ENGINEER: <PTD_00000000>	SCALE (SCALE)	SHEET : OF 11

# FPGA - SRAM INTERFACE AND BANK CONTROLS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

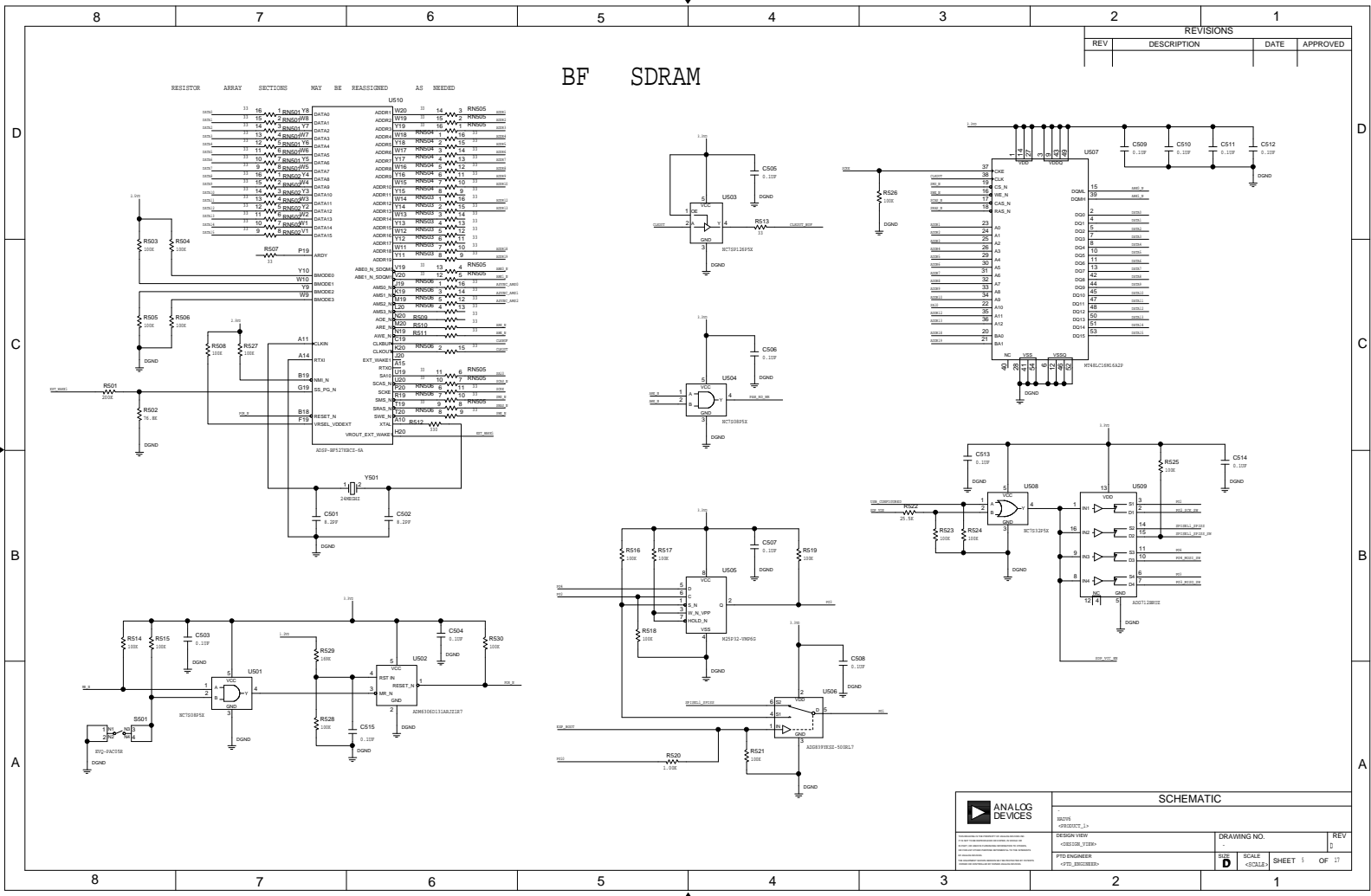


RA, RB AND AD LINES CAN BE MOVED WITHIN BANKS TO HELP ROUTING  
 ASK ENGINEER BEFORE MOVING ANY OTHER LINES



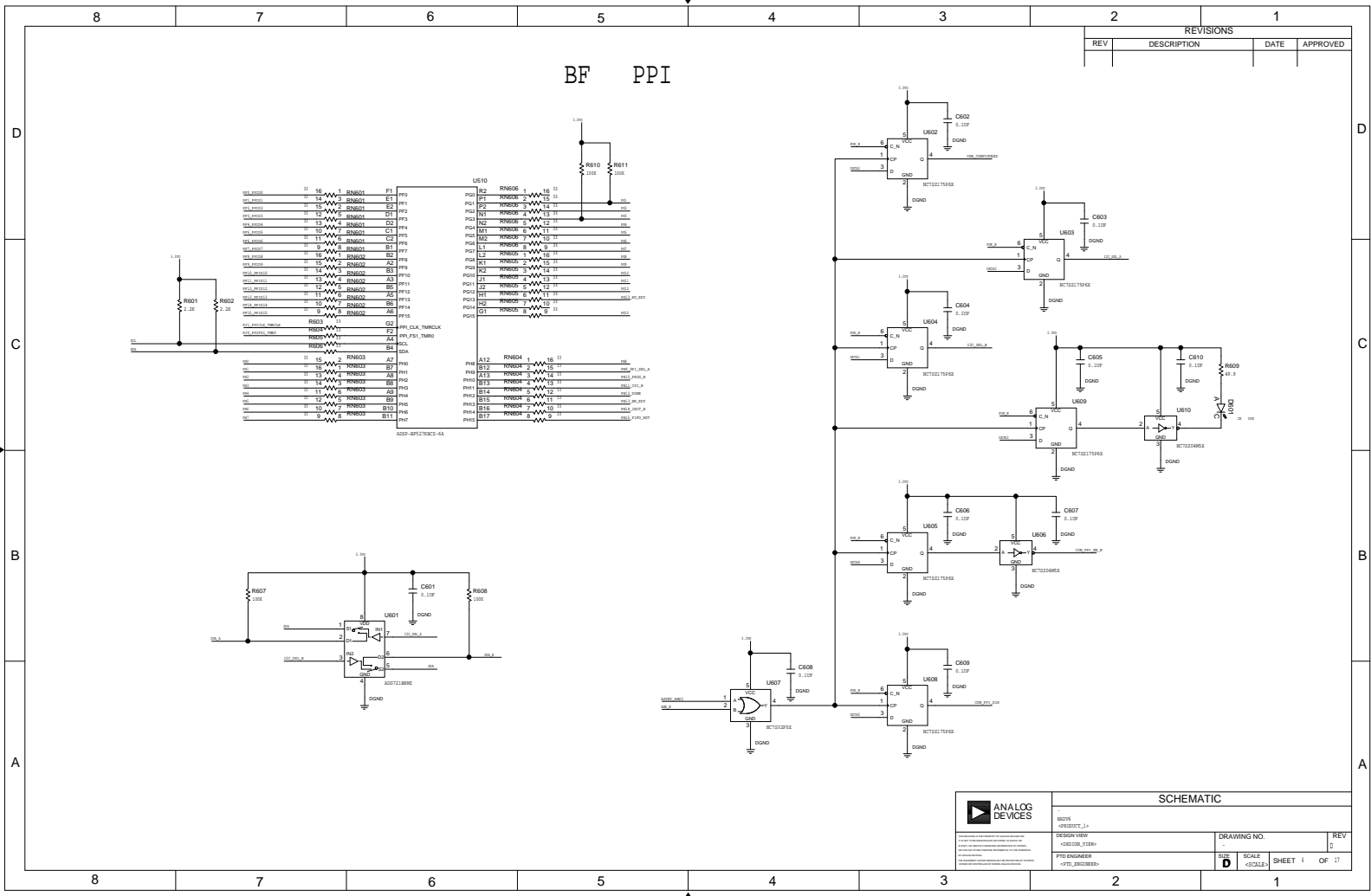
	SCHEMATIC		
	0205 #PRODUCT_11 DESIGN VIEW <08108_V100> PTD ENGINEER #PTD_08020800	DRAWING NO.	REV D
SIZE <b>D</b>	SCALE (SCALE)	SHEET 1	OF 11





REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	SCHEMATIC		
	82015 49830072_1 DESIGNER: <C50138_V129> PTD ENGINEER <PTD_49830072>	DRAWING NO. <C50138_V129>	REV D
SIZE D	SCALE <SCALE>	SHEET 1	OF 11



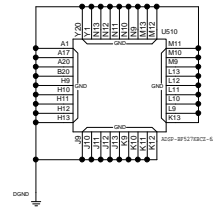
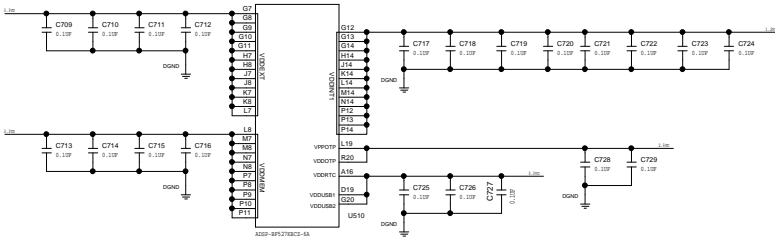
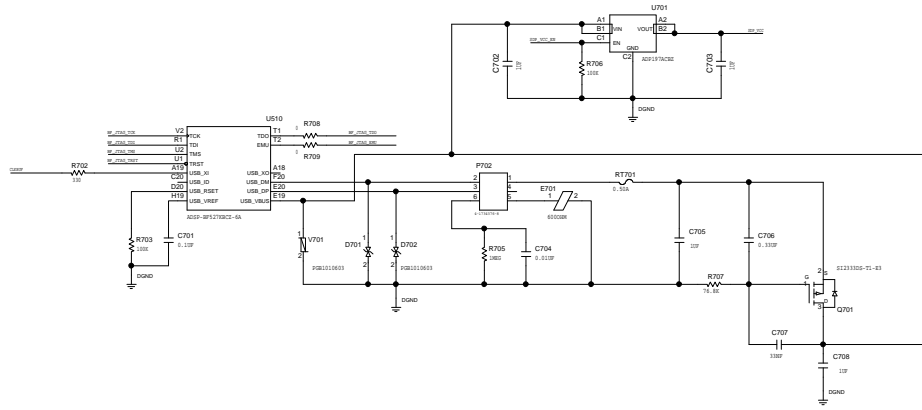
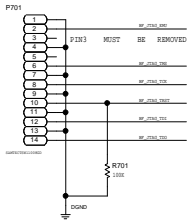
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

	SCHEMATIC		
	DESIGNER            PTD ENGINEER   	DRAWING NO.   	REV   
SIZE   	SCALE   	SHEET 1 OF 11	

# BF POWER, USB AND JTAG

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

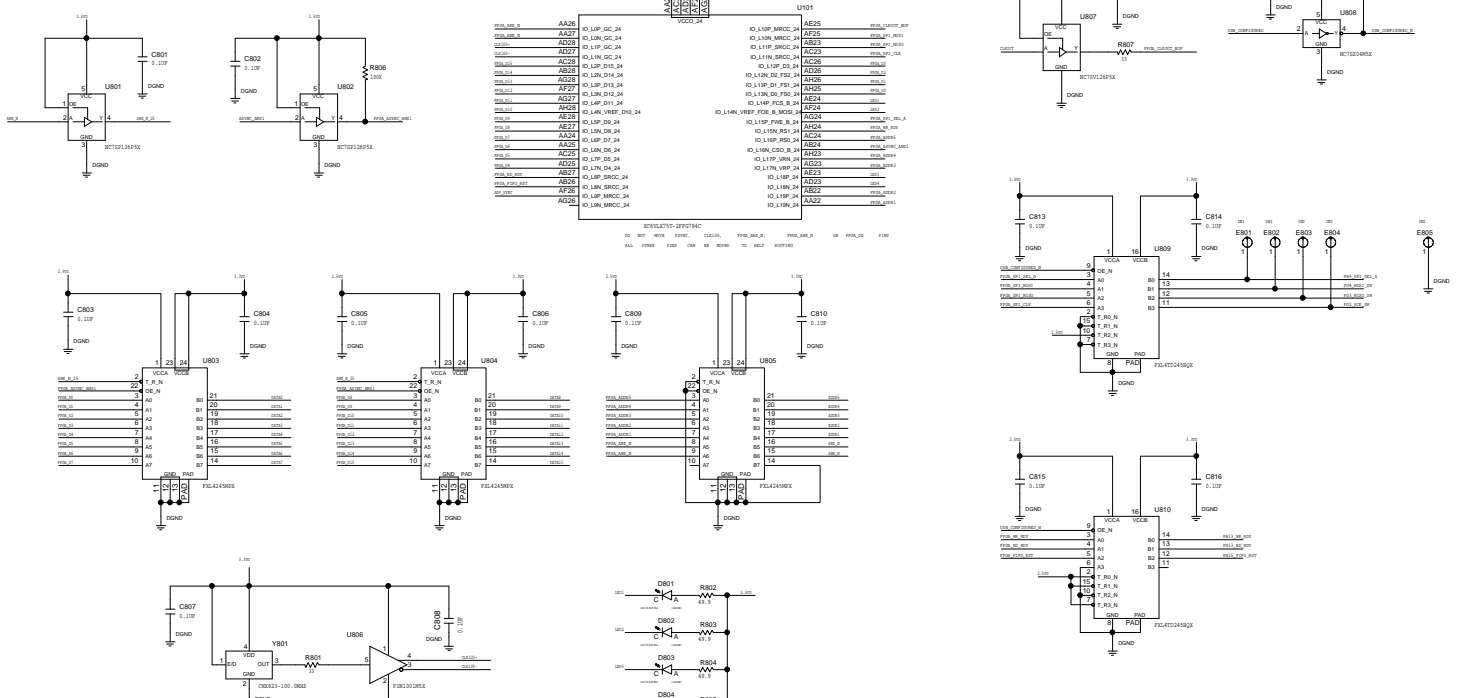
BF JTAG CONNECTOR



SCHEMATIC			
	82015 #REV0002_1.1 DESIGNER: V <C861038_V128> PTD ENGINEER #PTD_#00128000	DRAWING NO.	REV D
SIZE: <b>D</b>		SCALE: 1:1	SHEET 1 OF 11

# FPGA - BF INTERFACE, MISC

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



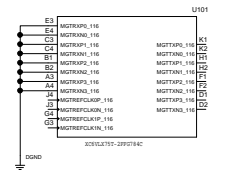
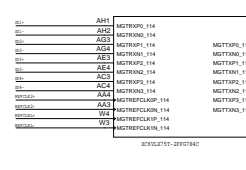
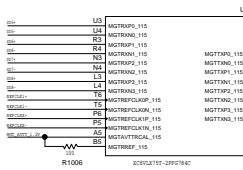
ANALOG DEVICES		SCHEMATIC	
REV	DESCRIPTION	DRAWING NO.	REV
001	09050071_1	080108_V100	D
DESIGNER	PTD	SCALE	SHEET 1 OF 11
PTD ENGINEER	PTD_08010800	(SCALE)	



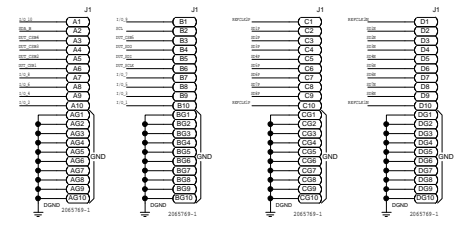
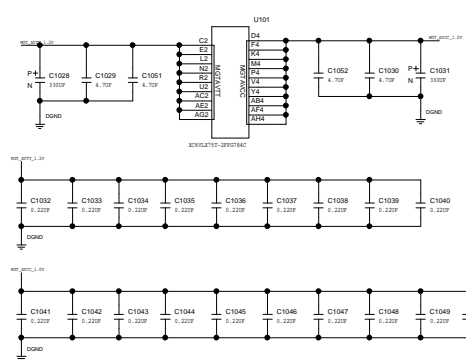
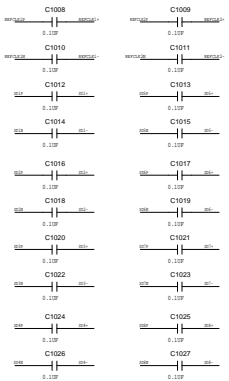
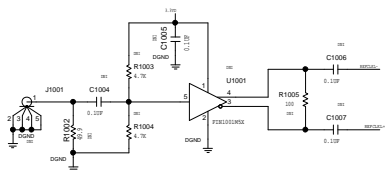
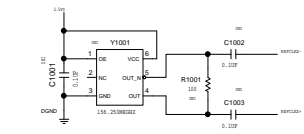


# GTX CONNECTIONS

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



SD DIFF PAIRS MAY BE MOVED TO HELP ROUTING  
 DO NOT CROSS BANKS  
 DIFF PAIR TRACE LENGTHS MUST BE MATCHED TO WITHIN 10 MILS  
 DIFF PAIR LANE LENGTHS MUST BE MATCHED TO WITHIN 100 MILS  
 TRACE LENGTHS BETWEEN R1006 AND FPGA MUST BE EQUAL IN LENGTH AND GEOMETRY

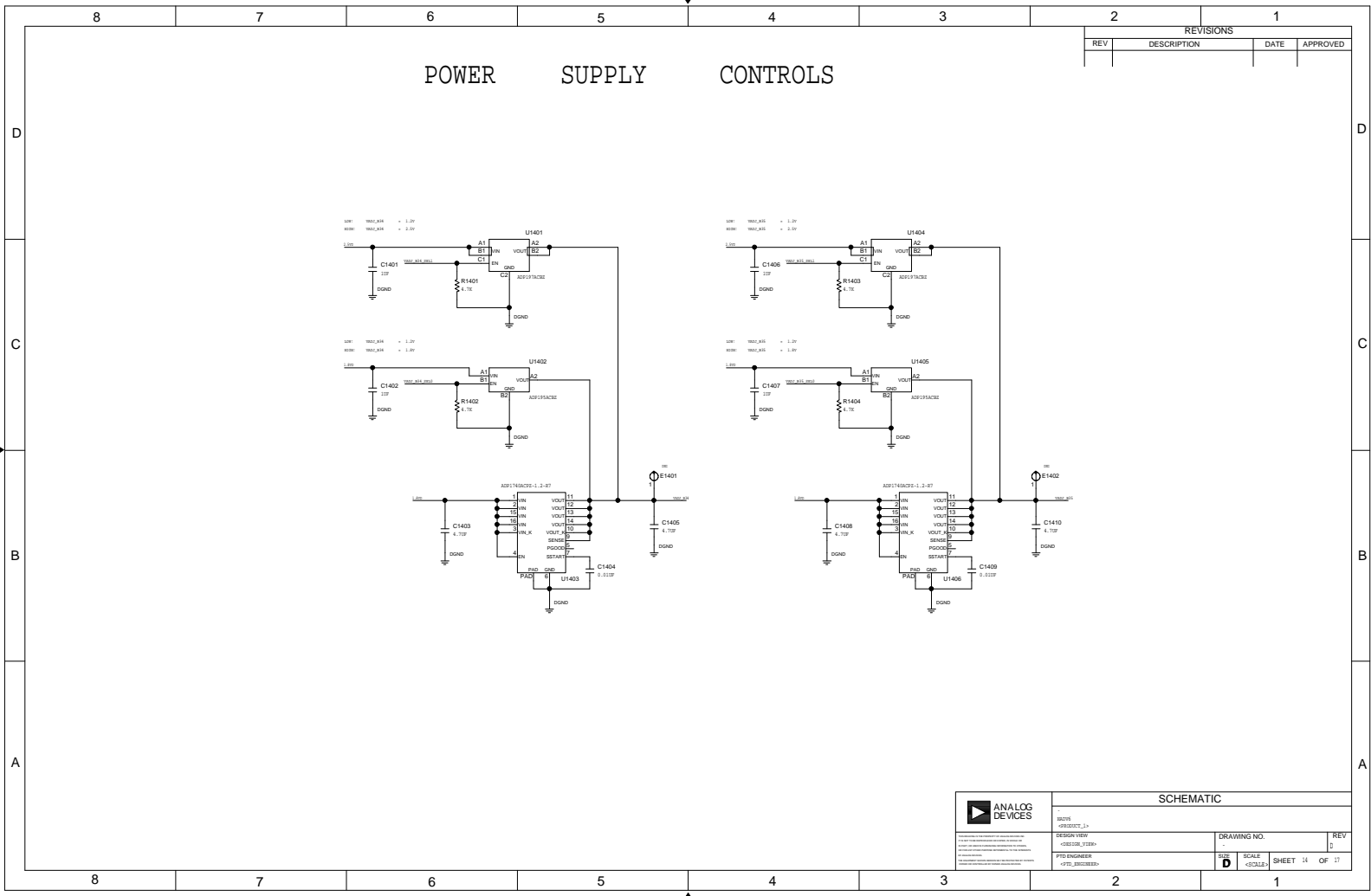


	SCHEMATIC		
	DESIGNER	DRAWING NO.	REV
	PTD ENGINEER	SCALE	SHEET







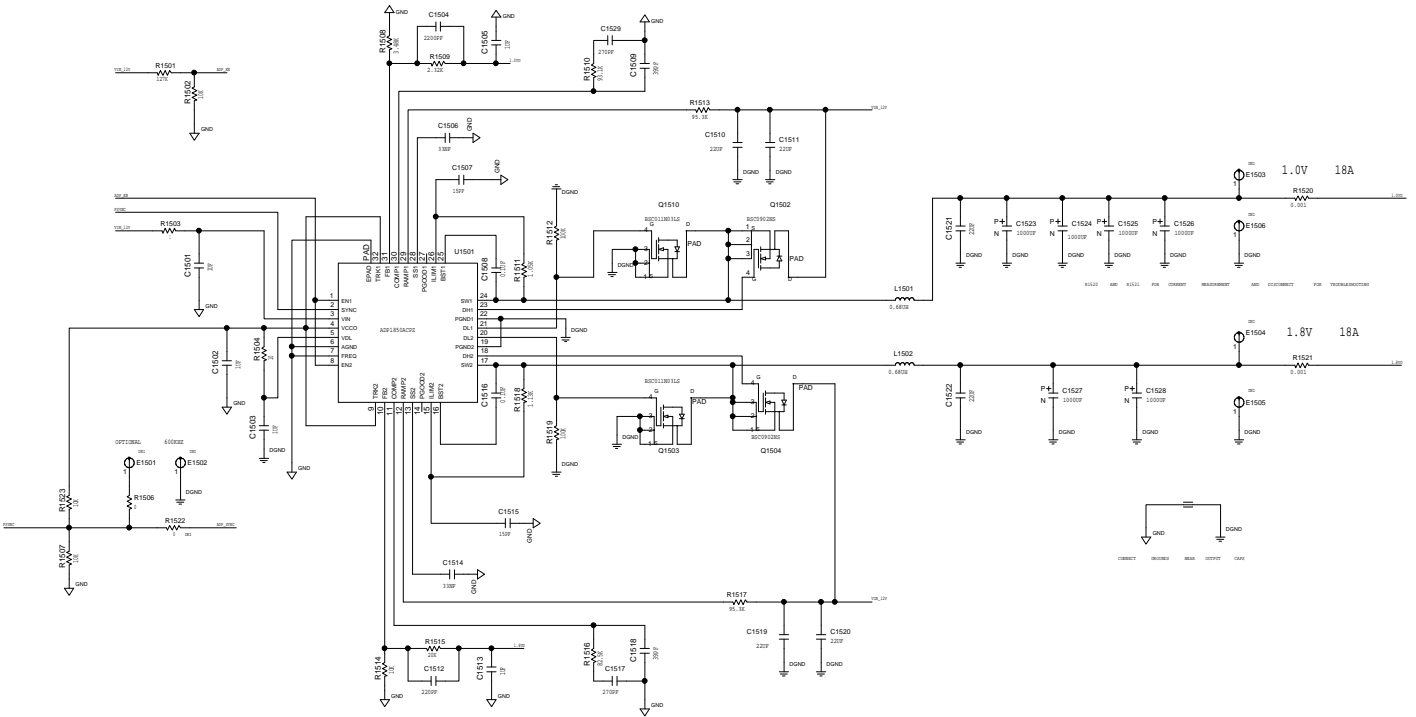


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SCHEMATIC			
		02015 0903007_13	
DESIGNER: <061038_V129>		DRAWING NO.	
PTD ENGINEER: <PTD_090328020>		REV D	
SIZE D	SCALE <SCALE>	SHEET 14	OF 11

POWER SUPPLIES: 1.0VD, 1.8VD

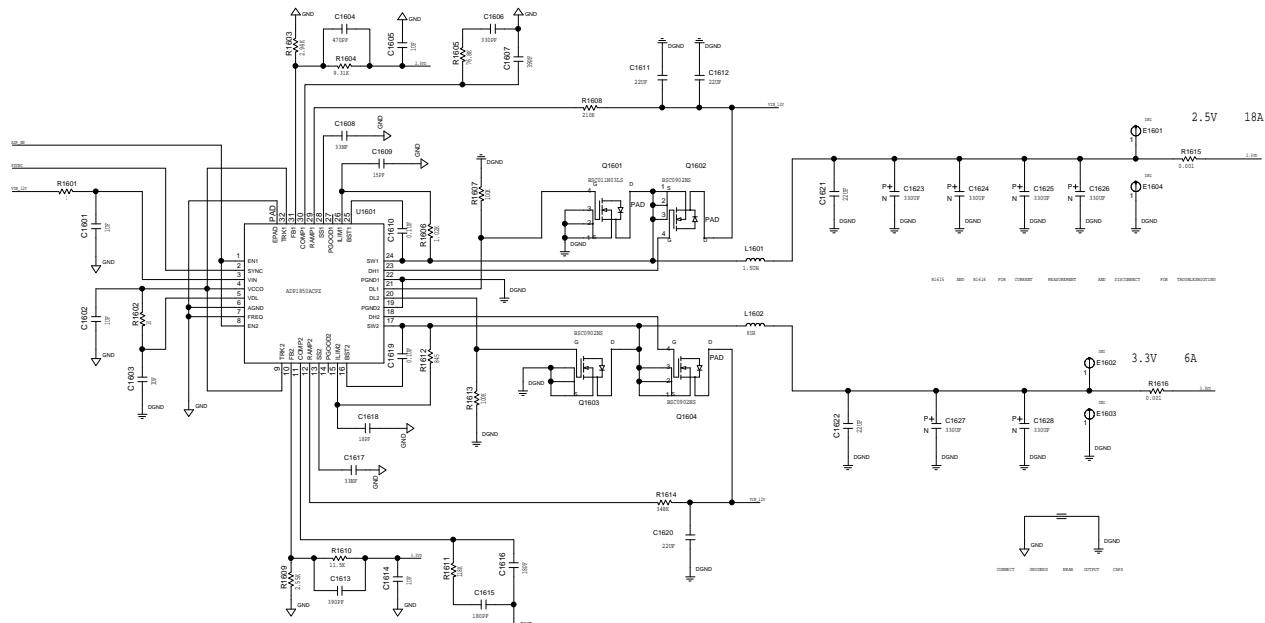
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



	SCHEMATIC		
	182715 (P930007)_1	DRAWING NO.	REV
	DESIGNER		D
	PTD ENGINEER		1
	SIZE	SCALE	SHEET
	D	(SCALE)	15 OF 17

POWER SUPPLIES: 2.5VD, 3.3VD

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

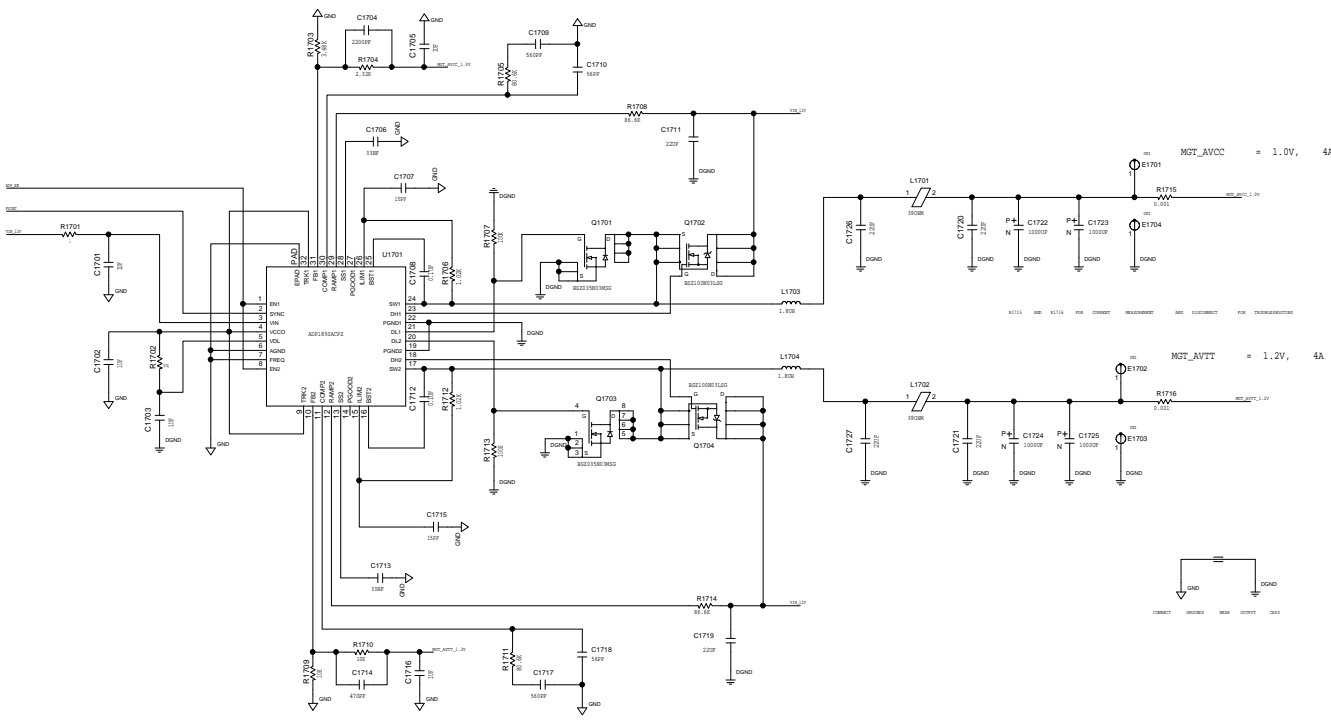


	SCHEMATIC		
	02015 09030072_13	DRAWING NO.	REV
	DESIGNER	C1613R_V129*	D
	PTD ENGINEER	*PTD_09030072	OF 11
SIZE	SCALE	SHEET	11
D	(SCALE)	11	11



# GTX POWER SUPPLIES

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



 <b>ANALOG DEVICES</b>	<b>SCHEMATIC</b>		
	18205 0905007_1 DESIGNER: <061038_V128> PTD ENGINEER <PTD_00020800>	DRAWING NO. REV D	SHEET 11 OF 11 SCALE 1:1 SIZE D