# **BUK9237-55A**

### N-channel TrenchMOS logic level FET

Rev. 3 — 9 November 2010

**Product data sheet** 

### 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

#### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant

- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching

Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \ge 25 \text{ °C}; T_j \le 175 \text{ °C}$	-	-	55	V
I <sub>D</sub>	drain current	$V_{GS} = 5 \text{ V}; T_{mb} = 25 \text{ °C};$ see <u>Figure 1</u> ; see <u>Figure 3</u>	-	-	32	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	77	W
Static chara	acteristics					
R <sub>DSon</sub>	drain-source on-state	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}$	-	28	33	mΩ
	resistance	$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 11}{\text{Figure } 12};$ see Figure 12	-	31	37	mΩ



Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Avalanche	ruggedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D = 32$ A; $V_{sup} \le 30$ V; $R_{GS} = 50$ $\Omega$ ; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped	-	-	76	mJ
Dynamic characteristics						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5 \text{ V; } I_D = 15 \text{ A;}$ $V_{DS} = 44 \text{ V; } T_j = 25 \text{ °C;}$ see Figure 13	-	9.2	-	nC

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain[1]	mb	D
3	S	source		
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT428 (DPAK)	

<sup>[1]</sup> It is not possible to make connection to pin 2 of the SOT428 package.

### 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9237-55A	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

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### 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	55	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	55	V
V <sub>GS</sub>	gate-source voltage		-15	15	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 5 V; see <u>Figure 1</u> ; see <u>Figure 3</u>	-	32	Α
		T <sub>mb</sub> = 100 °C; V <sub>GS</sub> = 5 V; see <u>Figure 1</u>	-	22	Α
I <sub>DM</sub>	peak drain current	$T_{mb}$ = 25 °C; $t_p \le 10 \mu s$ ; pulsed; see Figure 3	-	129	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	77	W
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drain	diode				
Is	source current	T <sub>mb</sub> = 25 °C	-	32	Α
I <sub>SM</sub>	peak source current	$t_p \le 10 \ \mu s$ ; pulsed; $T_{mb} = 25 \ ^{\circ}C$	-	129	Α
Avalanche rug	gedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 32 A; $V_{sup} \le$ 30 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	76	mJ

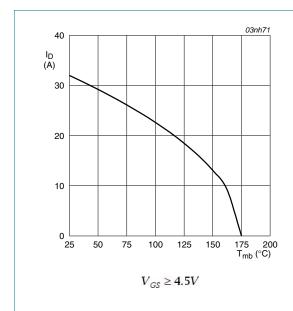


Fig 1. Continuous drain current as a function of mounting base temperature

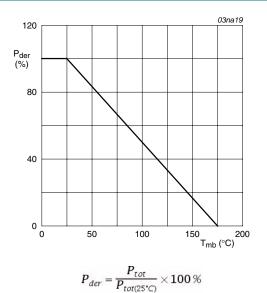
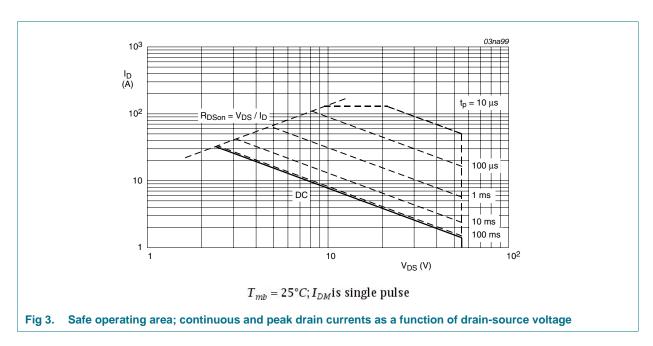


Fig 2. Normalized total power dissipation as a

function of mounting base temperature

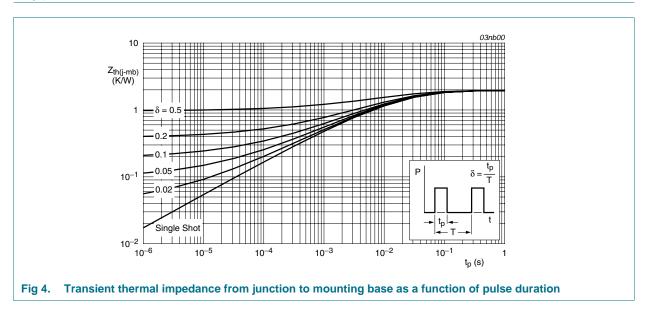
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### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	1.94	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient		-	71.4	-	K/W



### 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	racteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	55	-	-	V
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ °C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 25$ °C; see Figure 10	1	1.5	2	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see Figure 10	-	-	2.3	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = 175$ °C; see Figure 10	0.5	-	-	V
$I_{DSS}$ dr	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ °C}$	-	-	500	μA
I <sub>GSS</sub>	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{DS} = 0 \text{ V}; V_{GS} = -10 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R <sub>DSon</sub> drain-source on-sta resistance	drain-source on-state	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}$	-	-	38	mΩ
	resistance	$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	-	74	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}$	-	28	33	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 ^{\circ}\text{C};$ see <u>Figure 11</u> ; see <u>Figure 12</u>	-	31	37	mΩ
Dynamic o	characteristics					
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 44 \text{ V}; V_{GS} = 5 \text{ V};$	-	17.6	-	nC
$Q_{GS}$	gate-source charge	T <sub>j</sub> = 25 °C; see <u>Figure 13</u>	-	2.9	-	nC
$Q_{GD}$	gate-drain charge		-	9.2	-	nC
C <sub>iss</sub>	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	927	1236	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	151	181	pF
C <sub>rss</sub>	reverse transfer capacitance		-	96	131	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 5 \text{ V};$	-	6	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 10 \Omega; T_j = 25 \text{ °C}$	-	36	-	ns
$t_{d(off)}$	turn-off delay time		-	95	-	ns
t <sub>f</sub>	fall time		-	73	-	ns
L <sub>D</sub>	internal drain inductance	measured from drain to centre of die	-	2.5	-	nΗ
L <sub>S</sub>	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nΗ
Source-dra	ain diode					
$V_{SD}$	source-drain voltage	$I_S = 15 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ °C}$ ; see Figure 15	-	0.85	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ;	-	42	-	ns
Q <sub>r</sub>	recovered charge	$V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$	-	83	-	nC
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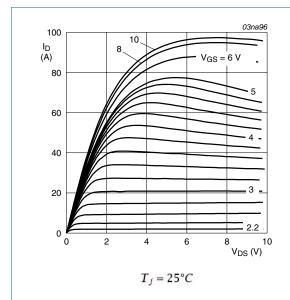


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

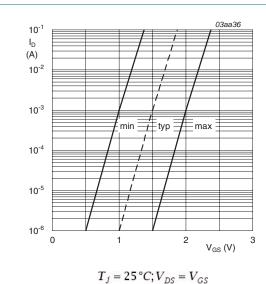
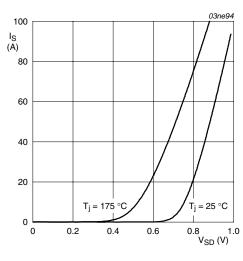
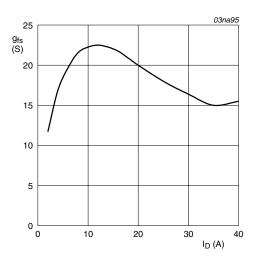


Fig 7. Sub-threshold drain current as a function of gate-source voltage



 $V_{GS} = \mathbf{0}V$ 

Fig 6. Reverse diode current as a function of reverse diode voltage; typical values



 $T_j = 25^{\circ}C; V_{DS} = 25V$ 

Fig 8. Forward transconductance as a function of drain current; typical values

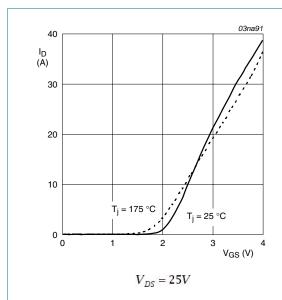
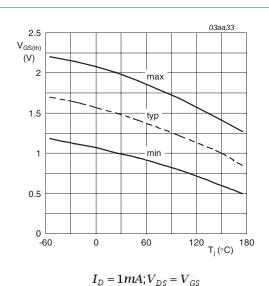
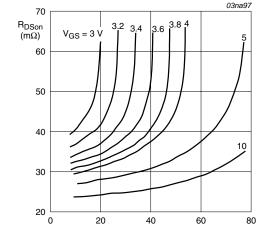


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



junction temperature

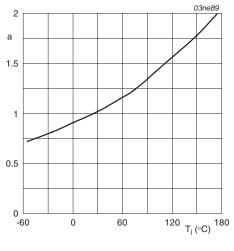
Fig 10. Gate-source threshold voltage as a function of



 $T_j = 25^{\circ}C$ 

Fig 11. Drain-source on-state resistance as a function

of drain current; typical values



 $a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$ 

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

 $I_D(A)$ 

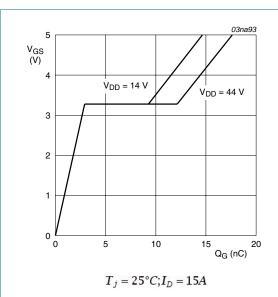
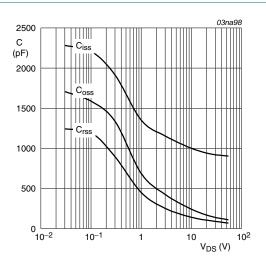


Fig 13. Gate-source voltage as a function of turn-on gate charge; typical values



$$V_{GS} = 0V; f = 1MHz$$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

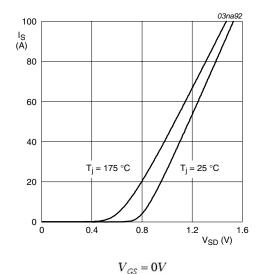


Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

### 7. Package outline

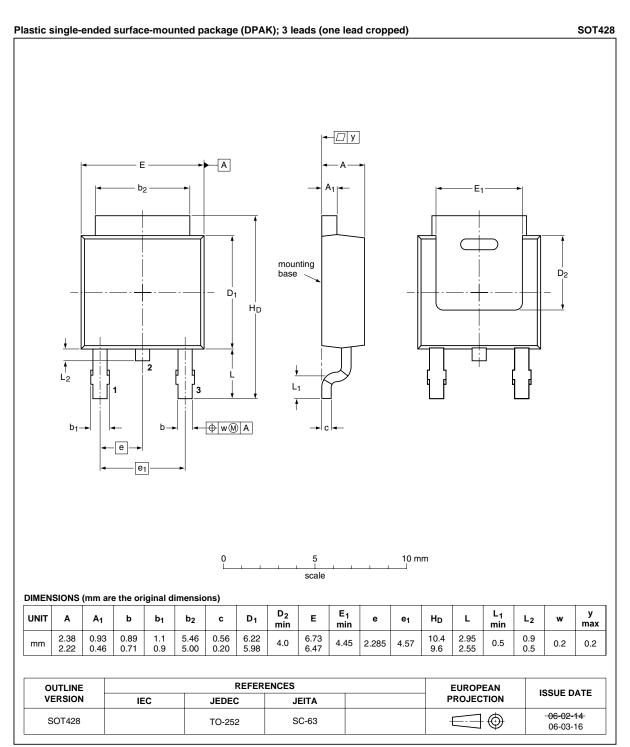


Fig 16. Package outline SOT428 (DPAK)

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## 8. Revision history

### Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9237-55A v.3	20101109	Product data sheet	-	BUK9237_55A-02
Modifications:	<ul> <li>Various chang</li> </ul>	ges to content.		
	<ul> <li>The format of of NXP Semion</li> </ul>		designed to comply wit	h the new identity guidelines
	<ul> <li>Legal texts have</li> </ul>	ave been adapted to the new	company name where	e appropriate.
BUK9237 55A-02	20020214	Product specification		BUK9237 55A-01

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#### 9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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# **BUK9237-55A**

### N-channel TrenchMOS logic level FET

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