Evaluation Board User Guide
UG-386

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Evaluating the AD9642/AD9634/AD6672 Analog-to-Digital Converters

FEATURES

Full featured evaluation board for the AD9642/AD9634/AD6672
SPI interface for setup and control
External or AD9523 clocking option
Balun/transformer or amplifier input drive option
LDO regulator power supply
VisualAnalog and SPI controller software interfaces

EQUIPMENT NEEDED

Analog signal source and antialiasing filter
Sample clock source (if not using the on-board oscillator)
2 switching power supplies (6.0 V, 2.5 A), CUI EPS060250UH-PHP-SZ, provided
PC running Windows® 98 (2nd ed.), Windows 2000, Windows ME, or Windows XP
USB 2.0 port recommended (USB 1.1 compatible)
AD9642, AD9634, or AD6672 evaluation board
HSC-ADC-EVALCZ FPGA-based data capture kit

SOFTWARE NEEDED

VisualAnalog
SPI controller

DOCUMENTS NEEDED

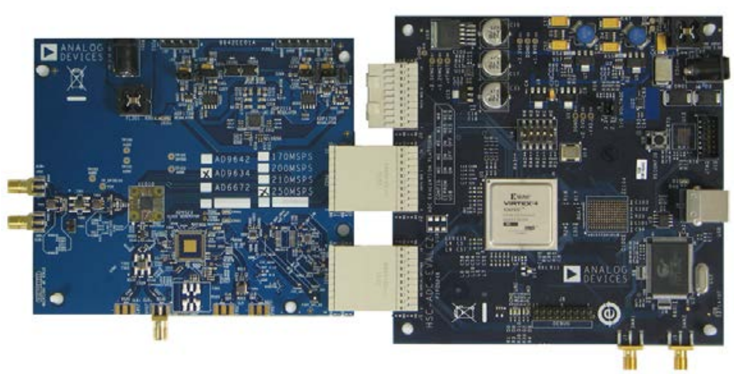
AD9642, AD9634, or AD6672 data sheet
HSC-ADC-EVALCZ data sheet
AN-905 Application Note, *VisualAnalog Converter Evaluation Tool Version 1.0 User Manual*
AN-878 Application Note, *High Speed ADC SPI Control Software*
AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*
AN-835 Application Note, *Understanding ADC Testing and Evaluation*

GENERAL DESCRIPTION

This user guide describes the AD9642, AD9634, and AD6672 evaluation board, which provides all of the support circuitry required to operate the AD9642, AD9634, and AD6672 in their various modes and configurations. The application software used to interface with the devices is also described.

The AD9642, AD9634, and AD6672 data sheets provide additional information and should be consulted when using the evaluation board. All documents and software tools are available at http://www.analog.com/fifo. For additional information or questions, send an email to highspeed.converters@analog.com.

TYPICAL MEASUREMENT SETUP



10593-001

Figure 1. AD9642, AD9634, or AD6672 Evaluation Board (on Left) and HSC-ADC-EVALCZ Data Capture Board (on Right)

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REVISION HISTORY

4/12—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The AD9642, AD9634, and AD6672 evaluation board provides all of the support circuitry required to operate these parts in their various modes and configurations. Figure 2 shows the typical bench characterization setup used to evaluate the ac performance of the AD9642, AD9634, or AD6672. It is critical that the signal sources used for the analog input and the clock have very low phase noise (<1 ps rms jitter) to realize the optimum performance of the signal chain. Proper filtering of the analog input signal to remove harmonics and lower the integrated or broadband noise at the input is necessary to achieve the specified noise performance.

See the Evaluation Board Software Quick Start Procedures section to get started, and see Figure 19 to Figure 30 for the complete schematics and layout diagrams. These diagrams demonstrate the routing and grounding techniques that should be applied at the system level when designing application boards using these converters.

POWER SUPPLIES

This evaluation board comes with a wall-mountable switching power supply that provides a 6 V, 2.5 A maximum output. Connect the supply to a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz. The output from the supply is provided through a 2.1 mm inner diameter jack that connects to the printed circuit board (PCB) at P201. The 6 V supply is fused and conditioned on the PCB before connecting to the low dropout linear regulators (default configuration) that supply the proper bias to each of the various sections on the board.

The evaluation board can be powered in a nondefault condition using external bench power supplies. To do this, remove the jumpers on the P104, P107, P108, and P105 header pins to disconnect the outputs from the on-board LDOs. This enables the user to bias each section of the board individually. Use P202 and P203 to connect a different supply for each section. A 1.8 V supply is needed with a 1 A current capability for DUT_AVDD and DRVDD; however, it is recommended that separate supplies be used for both analog and digital domains. An additional supply is also required to supply 1.8 V for digital support circuitry on the board, DVDD. This should also have a 1 A current capability and can be combined with DRVDD with little or no degradation in performance. To operate the evaluation board using the SPI and alternate clock options, a separate 3.3 V analog supply is needed in addition to the other supplies. This 3.3 V supply, or 3P3V_ANALOG, should have a 1 A current capability. This 3.3 V supply is also used to support the optional input path amplifier (ADL5201) on Channel A and Channel B.

INPUT SIGNALS

When connecting the clock and analog source, use clean signal generators with low phase noise, such as the Rohde & Schwarz SMA or HP 8644B signal generators or an equivalent. Use a 1 m shielded, RG-58, 50 Ω coaxial cable for connecting to the evaluation board. Enter the desired frequency and amplitude (see the Specifications section in the data sheet of the respective part).

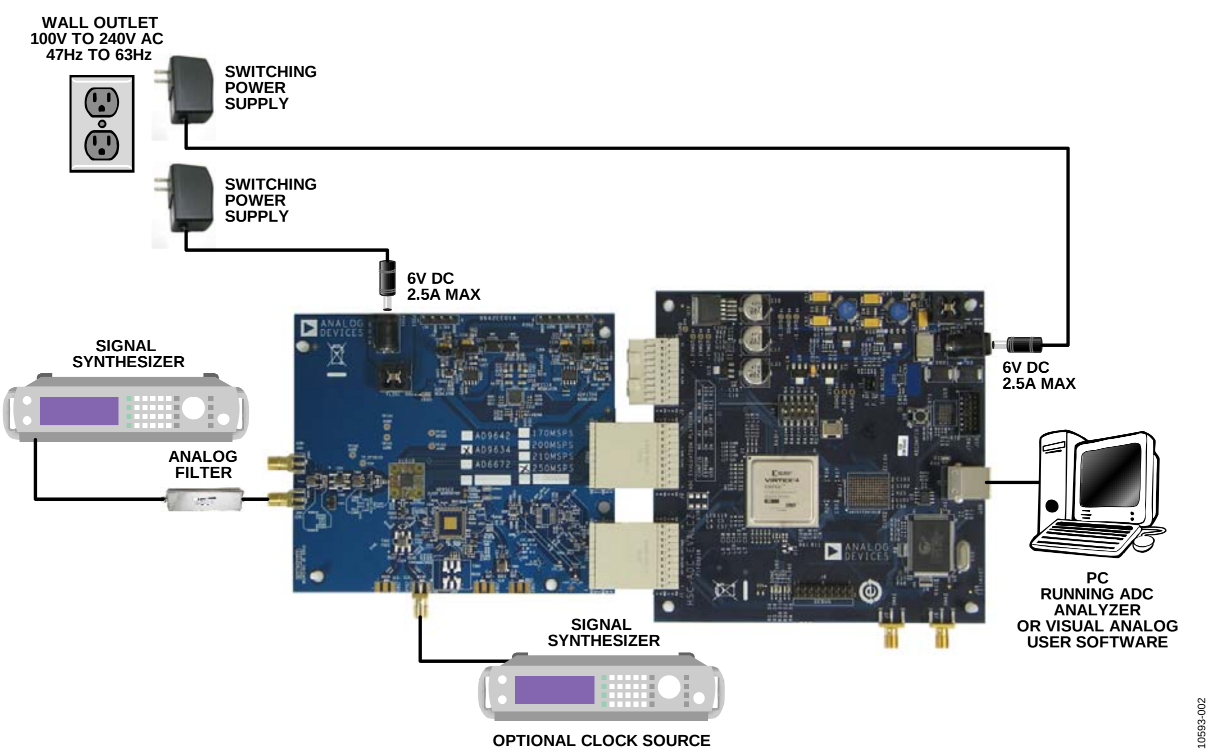

Figure 2. Evaluation Board Connection

When connecting the analog input source, use of a multipole, narrow-band, band-pass filter with 50 Ω terminations is recommended. Analog Devices, Inc., uses TTE and K&L Microwave, Inc., band-pass filters. The filters should be connected directly to the evaluation board.

If an external clock source is used, it should also be supplied with a clean signal generator as previously specified. Typically, most Analog Devices evaluation boards can accept ~2.8 V p-p or 13 dBm sine wave input for the clock.

OUTPUT SIGNALS

The default setup uses the Analog Devices high speed converter evaluation platform (HSC-ADC-EVALCZ) for data capture. The output signals from Channel A and Channel B for the AD9642, AD9634, and AD6672 are routed through P601 and P602, respectively, to the FPGA on the data capture board.

DEFAULT OPERATION AND JUMPER SELECTION SETTINGS

This section explains the default and optional settings or modes allowed on the AD9642/AD9634/AD6672 evaluation board.

Power Circuitry

Connect the switching power supply that is supplied in the evaluation kit between a rated 100 V ac to 240 V ac wall outlet at 47 Hz to 63 Hz and P201.

Analog Input

The A and B channel inputs on the evaluation board are set up for a double balun-coupled analog input with a 50 Ω impedance. This input network is optimized to support a wide frequency band. See the AD9642, AD9634, and AD6672 data sheets for additional information on the recommended networks for different input frequency ranges. The nominal input drive level is 10 dBm to achieve 2 V p-p full scale into 50 Ω. At higher input frequencies, slightly higher input drive levels are required due to losses in the front-end network.

Optionally, Channel A and Channel B inputs on the board can be configured to use the ADL5201 digitally controlled, variable gain wide bandwidth amplifier. The ADL5201 component is included on the evaluation board at U401. However, the path into and out of the ADL5201 can be configured in many different ways depending on the application; therefore, the parts in the input and output path are left unpopulated. See the ADL5201 data sheet for additional information on this part and for configuring the inputs and outputs. The ADL5201, by default, is held in power-down mode but can be enabled by adding 1 kΩ resistors at R427 and R428 to enable Channel A and Channel B, respectively.

Clock Circuitry

The default clock input circuit that is populated on the AD9642/AD9634/AD6672 evaluation board uses a simple transformer-coupled circuit with a high bandwidth 1:1 impedance ratio transformer (T503) that adds a very low amount of jitter to the clock path. The clock input is 50 Ω terminated and ac-coupled to handle single-ended sine wave types of inputs. The transformer converts the single-ended input to a differential signal that is clipped by CR503 before entering the ADC clock inputs.

The board is set by default to use an external clock generator. An external clock source capable of driving a 50 Ω terminated input should be connected to J506.

A differential LVPECL clock driver output can also be used to clock the ADC input using the AD9523 (U501). To place the AD9523 into the clock path, populate R541 and R542 with 0 Ω resistors and remove C532 and C533 to disconnect the default clock path inputs. In addition, populate R533 and R534 with 0 Ω resistors, remove R522 and R523 to disconnect the default clock path outputs, and insert AD9523 LVPECL Output 2. The AD9523 must be configured through the SPI controller software to set up the PLL and other operation modes. Consult the AD9523 data sheet for more information about these and other options.

PDWN

To enable the power-down feature, Bits[1:0] of Register 0x08 must be written for the desired power-down mode.

OEB

To disable the digital output pins and place them in a high impedance state, Bit 4 of Register 0x14 must be written.

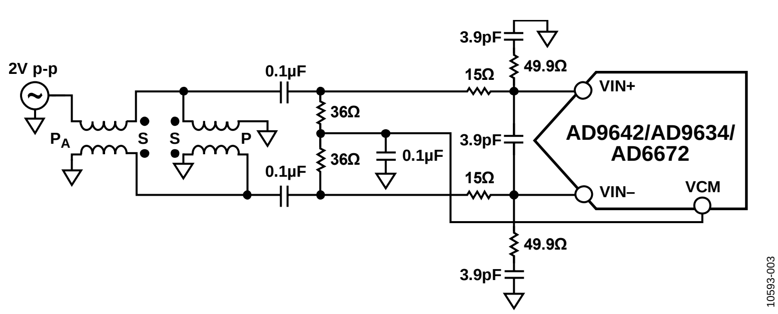

Figure 3. Default Analog Input Configuration of the AD9642/AD9634/AD6672

Switching Power Supply

Optionally, the ADC on the board can be configured to use the ADP2114 dual switching power supply to provide power to the DRVDD and AVDD rails of the ADC. To configure the board to operate from the ADP2114, the following changes must be incorporated (see the Evaluation Board Schematics and Artwork and the Bill of Materials sections for specific recommendations for part values):

1. Install R204 and R221 to enable the ADP2114.
2. Install R216 and R218.
3. Install L201 and L202.
4. Remove JP201 and JP203.
5. Remove jumpers from across Pin 1 and Pin 2 on P107 and P108, respectively.
6. Place jumpers across Pin 1 and Pin 2 of P106 and P109, respectively.

Making these changes enables the switching converter to power the ADC. Using the switching converter as the ADC power source is more efficient than using the default LDOs.

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

This section provides quick start procedures for using the AD9642/AD9634/AD6672 evaluation board. Both the default and optional settings are described.

CONFIGURING THE BOARD

Before using the software for testing, configure the evaluation board as follows:

1. Connect the evaluation board to the data capture board, as shown in Figure 1 and Figure 2.
2. Connect one 6 V, 2.5 A switching power supply (such as the CUI, Inc., EPS060250UH-PHP-SZ that is supplied) to the AD9642/AD9634/AD6672 board.
3. Connect another 6 V, 2.5 A switching power supply (such as the CUI EPS060250UH-PHP-SZ that is supplied) to the HSC-ADC-EVALCZ board.
4. Connect the HSC-ADC-EVALCZ board (J6) to the PC with a USB cable.
5. On the ADC evaluation board, confirm that jumpers are installed on the P105, P108, P104, P107, and P110 headers.
6. Connect a low jitter sample clock to Connector J506.
7. Use a clean signal generator with low phase noise to provide an input signal to the desired channel(s) at Connector J301 (Channel A) and/or Connector J303 (Channel B). Use a 1 m, shielded, RG-58, 50 Ω coaxial cable to connect the signal generator. For best results, use a narrow-band band-pass filter with 50 Ω terminations and an appropriate center frequency. (Analog Devices uses TTE, Allen Avionics, and K&L band-pass filters.)

USING THE SOFTWARE FOR TESTING

Setting Up the ADC Data Capture

After configuring the board, set up the ADC data capture using the following steps:

1. Open VisualAnalog® on the connected PC. The appropriate part type should be listed in the status bar of the **VisualAnalog – New Canvas** window. Select the template that corresponds to the type of testing to be performed (see Figure 4 where the AD9642 is shown as an example). The AD9642 is given as an example in this user guide. Similar settings are used for the AD9634. For the AD6672, the differences are noted where necessary in the steps that follow.

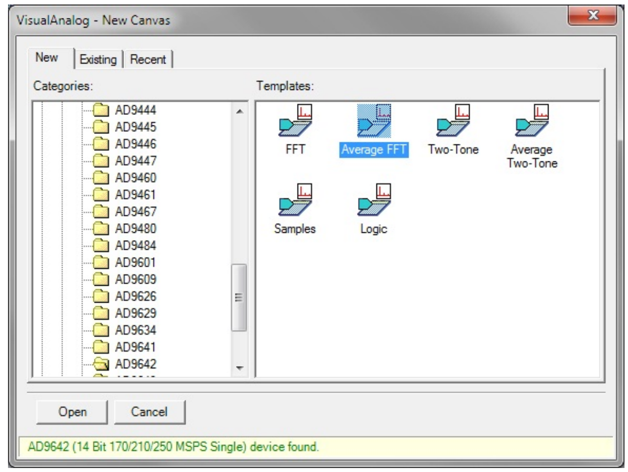

Figure 4. VisualAnalog, New Canvas Window

2. After the template is selected, a message appears asking if the default configuration can be used to program the FPGA (see Figure 5). Click **Yes**, and the window closes.

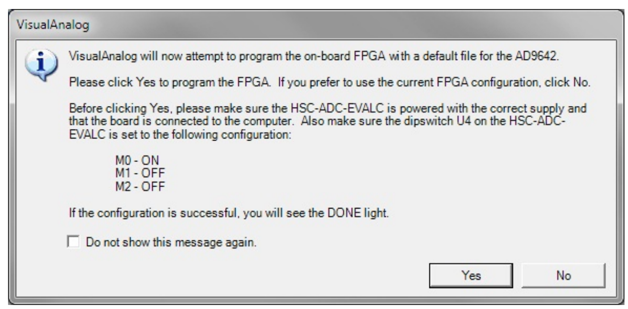

Figure 5. VisualAnalog Default Configuration Message

3. To change features to settings other than the default settings, click the **Expand Display** button, located on the bottom right corner of the window (see Figure 6) to see what is shown in Figure 7.
   Detailed instructions for changing the features and capture settings can be found in the AN-905 Application Note, *VisualAnalog™ Converter Evaluation Tool Version 1.0 User Manual*. After the changes are made to the capture settings, click the **Collapse Display** button.

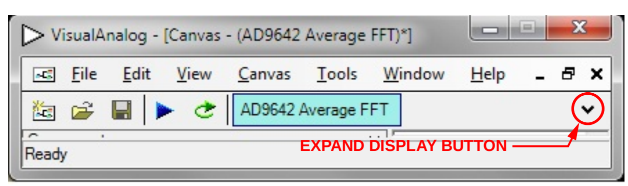

Figure 6. VisualAnalog Window Toolbar, Collapsed Display

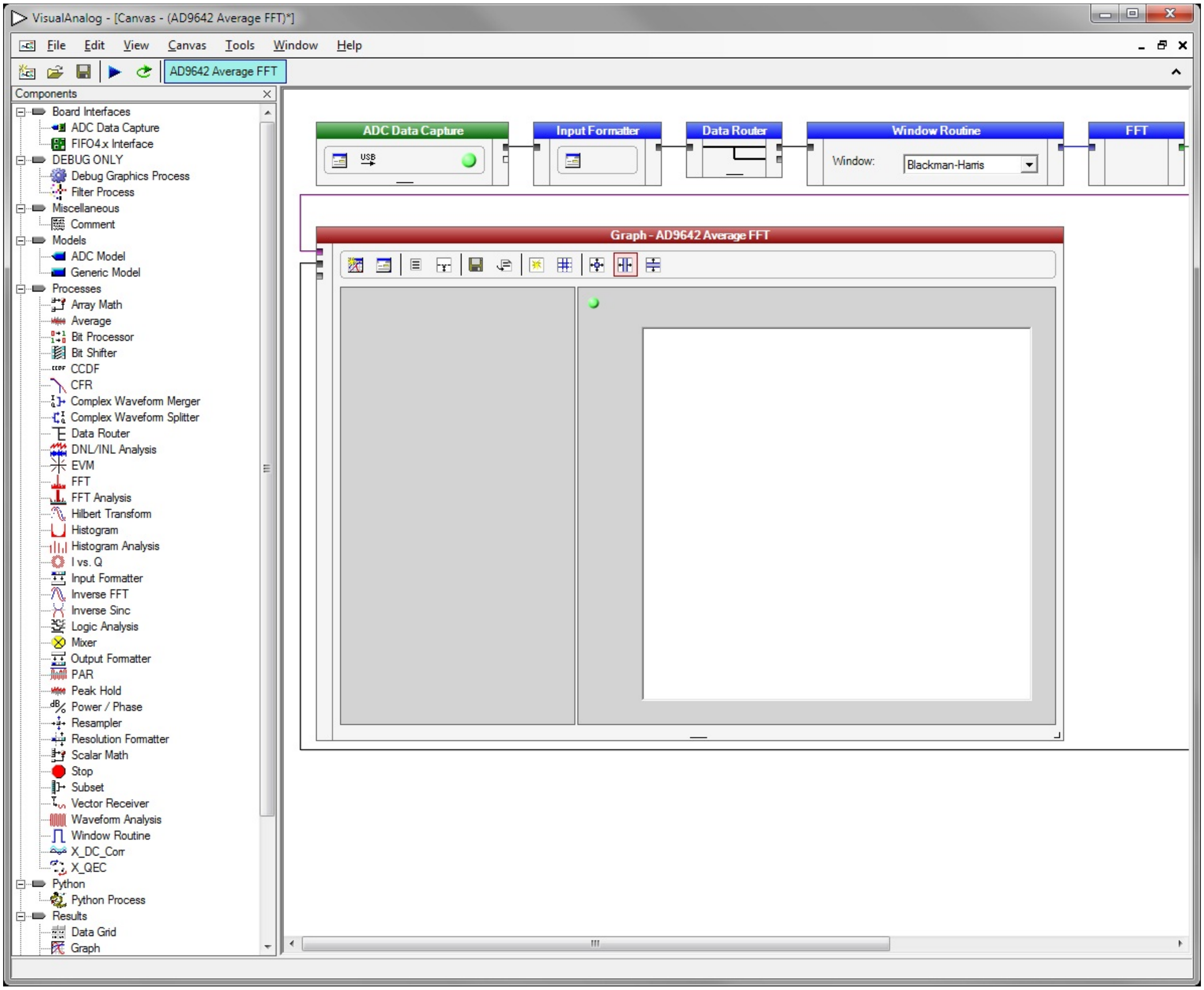

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Figure 7. VisualAnalog, Main Window

Setting Up the SPI Controller Software

After the ADC data capture board setup is complete, set up the SPI controller software using the following procedure:

1. Open the SPI controller software by going to the **Start** menu or by double-clicking the **SPIController** software desktop icon. If prompted for a configuration file, select the appropriate one. If not, check the title bar of the window to determine which configuration is loaded. If necessary, choose **Cfg Open** from the **File** menu and select the appropriate file based on your part type. Note that the **CHIP ID(1)** section should be filled to indicate whether the correct SPI controller configuration file is loaded (see Figure 8).

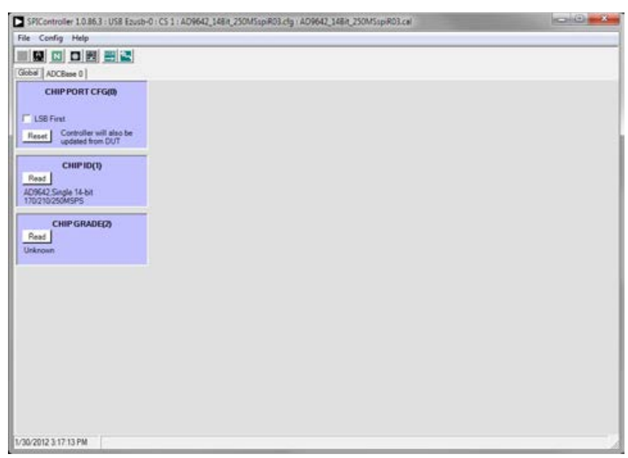

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Figure 8. SPI Controller, CHIP ID(1) Section

2. Click the **New DUT** button in the **SPIController** window (see Figure 9).

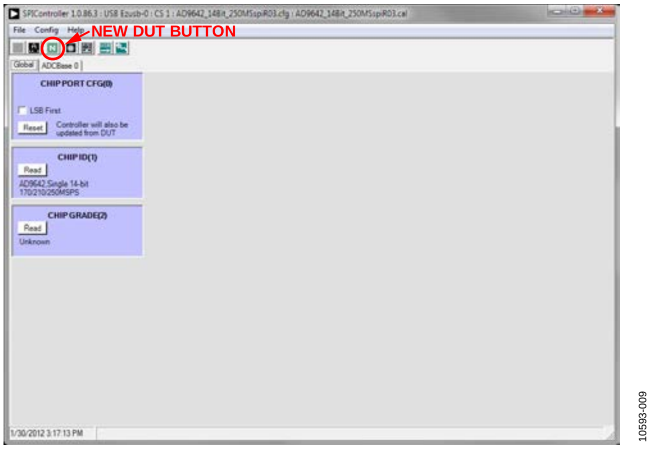

Figure 9. SPI Controller, New DUT Button

3. In the **ADCBase 0** tab of the **SPIController** window, find the **CLK DIV(B)** section (see Figure 11). If using the clock divider, use the drop-down box to select the correct clock divide ratio, if necessary. See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information.

4. In the **ADCBase 0** tab of the **SPIController** window, find the **OUTPUT DELAY(17)** box. Select the **DCO Clk Delay Enable** checkbox to enable this feature. In the drop-down box, select **600 ps additional delay on DCO pin**. These settings align the output timing with the input timing on the capture FPGA.
   Note that other settings can be changed on the **ADCBase 0** tab (see Figure 11). See the appropriate part data sheet; the AN-878 Application Note, *High Speed ADC SPI Control Software*; and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional information on the available settings.

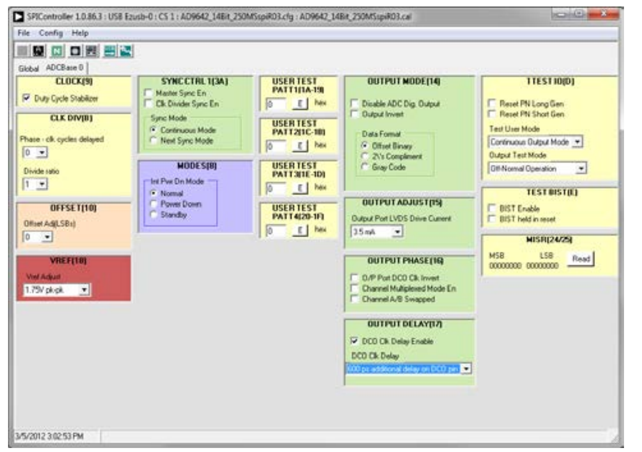

Figure 10. SPI Controller, Example ADCBase 0 Tab

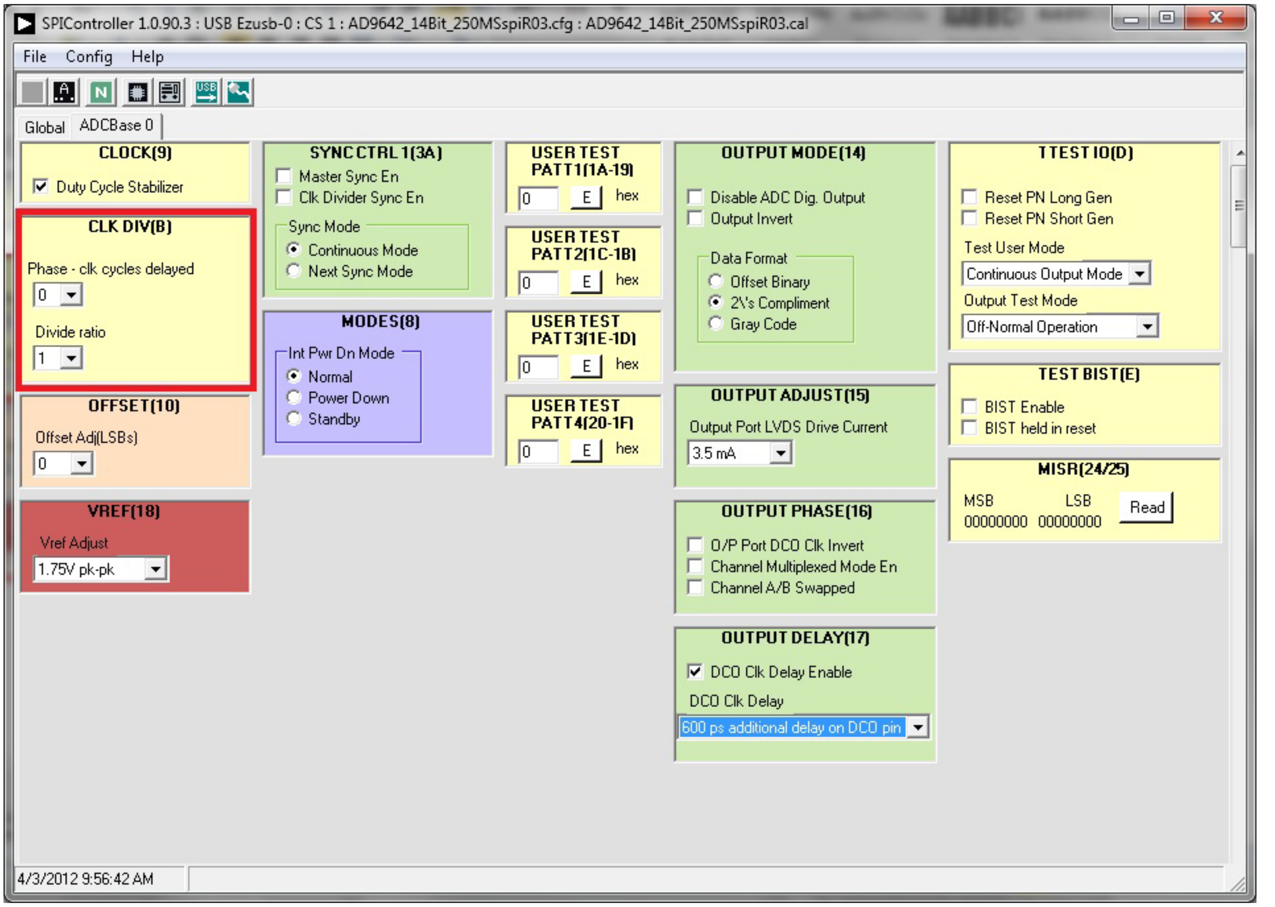

Figure 11. SPI Controller, CLK DIV(B) Section

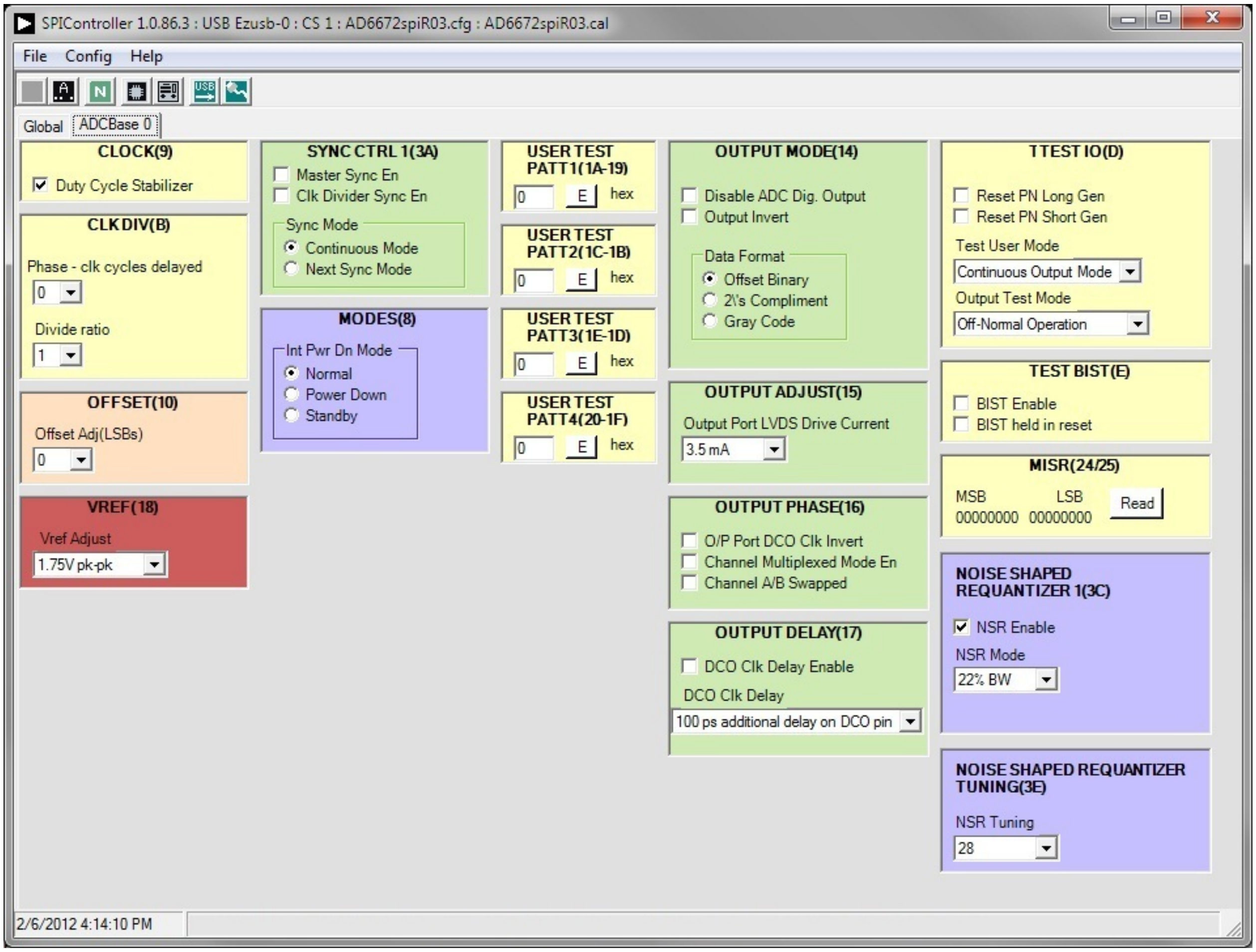

Figure 12. SPI Controller, Example ADCBase 0 Tab—NSR Settings for the AD6672

5. If using the noise shaping requantizer (NSR) feature of the AD6672, the settings in the **ADCBase 0** tab must be changed (see Figure 12). The **NSR Enable** checkbox must be selected under the **NOISE SHAPED REQUANTIZER 1(3C)** section. This enables the circuitry in the AD6672. To select the bandwidth mode, use the **NSR Mode** drop-down box in the **NOISE SHAPED REQUANTIZER 1(3C)** section. Upon selecting the bandwidth mode, select the desired tuning word in the **NSR Tuning** drop-down menu under the **NOISE SHAPED REQUANTIZER TUNING(3E)** section.
6. Click the **Run** button in the **VisualAnalog** toolbar (see Figure 13).

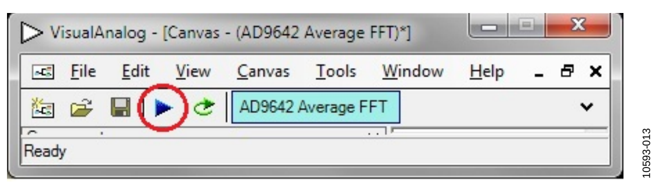

Figure 13. Run Button (Encircled in Red) in VisualAnalog Toolbar, Collapsed Display

Adjusting the Amplitude of the Input Signal

The next step is to adjust the amplitude of the input signal for each channel as follows:

1. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the **Fund Power** reading in the left panel of the VisualAnalog **Graph** window.) See Figure 15.
2. Repeat this procedure for Channel B if desired.
3. Click the **Save** disk icon within the **Graph** window to save the performance plot data as a .csv formatted file. See Figure 14 for an example.

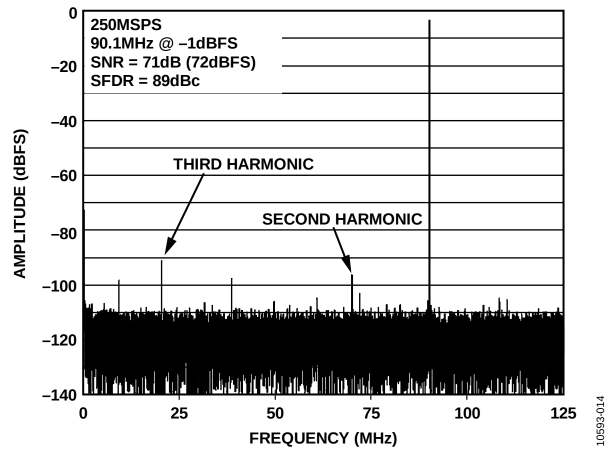

Figure 14. Typical FFT, AD9642

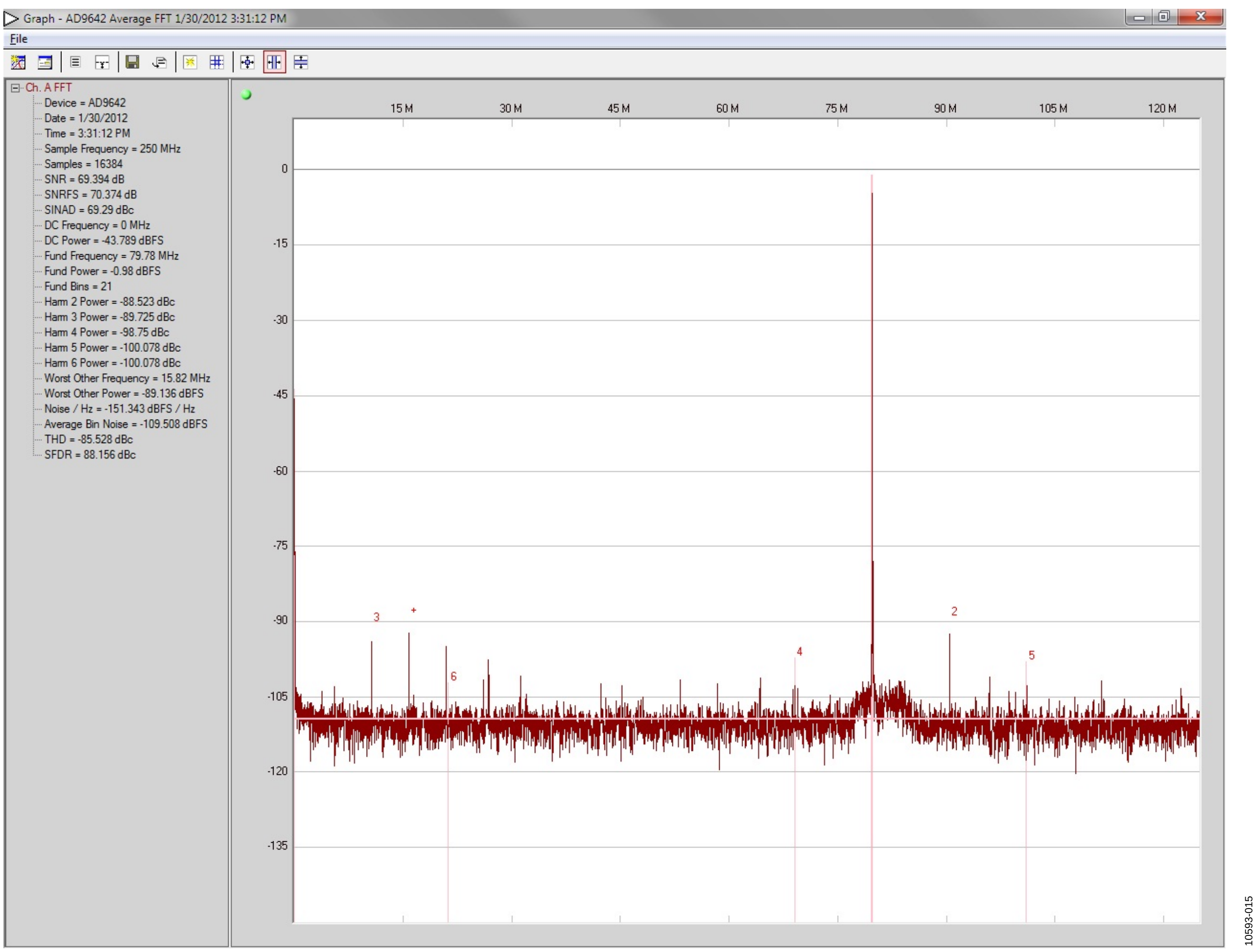

Figure 15. Graph Window of VisualAnalog (AD9642)

4. If operating the AD6672 with NSR enabled, certain options in VisualAnalog must be enabled. Click the button circled in the **FFT Analysis** box (see Figure 16) in VisualAnalog to bring up the options for setting the NSR.

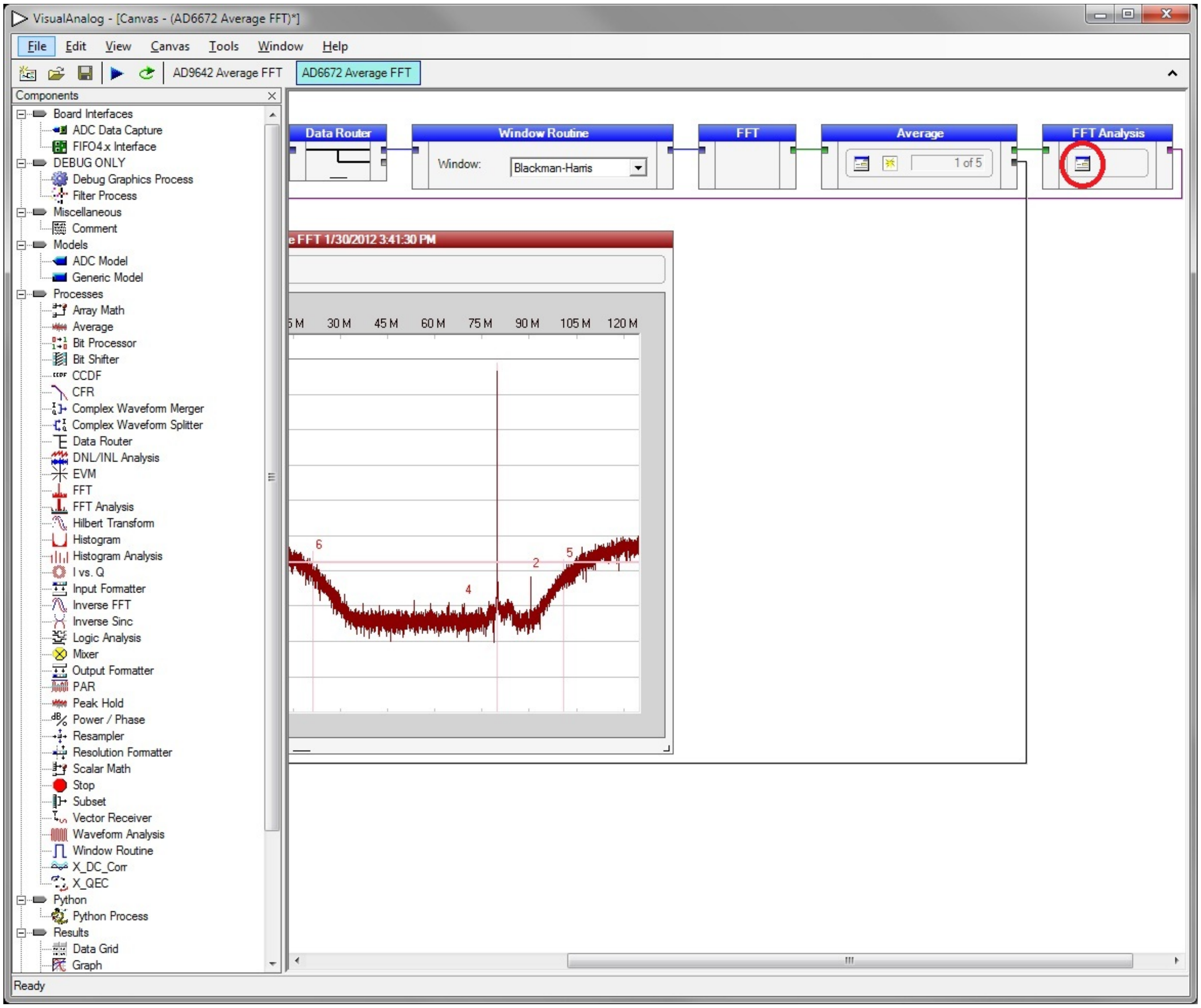

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Figure 16. VisualAnalog, Main Window—Showing FFT Analysis for AD6672

5. Configure the settings in the FFT analysis to match the settings selected for the NSR in the SPI controller (see Figure 17).

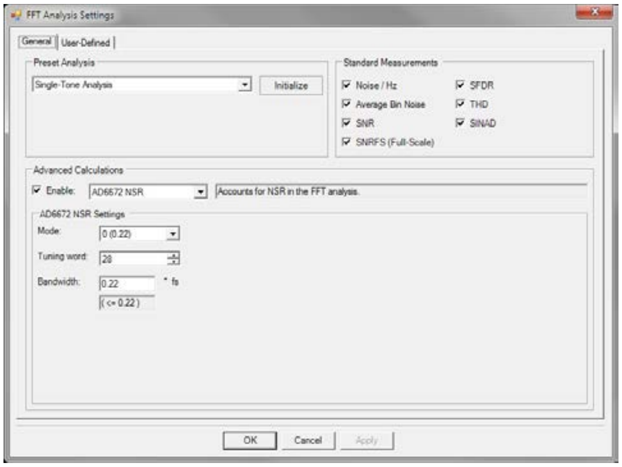

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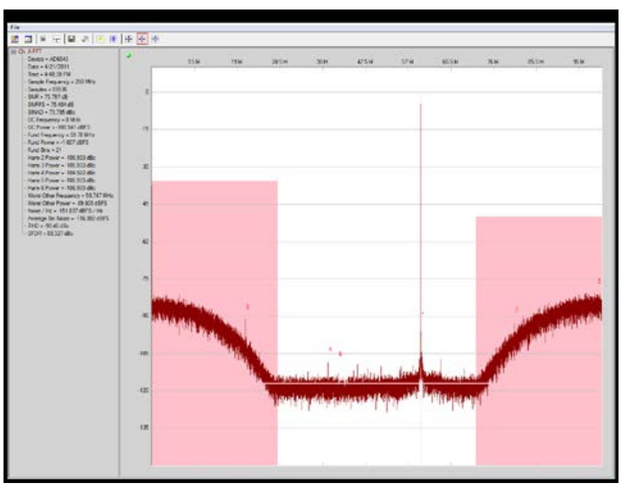
Figure 17. VisualAnalog, FFT Analysis Settings for AD6672

6. The result should show an FFT plot that looks similar to Figure 18.



10593-018

Figure 18. Graph Window of VisualAnalog, NSR Enabled, AD6672

7. The amplitude shows approximately 0.6 dB lower than when the NSR is disabled. The NSR circuitry introduces this loss. An amplitude of −1.6 dBFS with NSR enabled is analogous to an amplitude of −1.0 dBFS with NSR disabled.

8. Repeat Step 3 to save the graph in a .csv file format.

Troubleshooting Tips

If the FFT plot appears abnormal, do the following:

- If you see a normal noise floor when you disconnect the signal generator from the analog input, be sure that you are not overdriving the ADC. Reduce the input level if necessary.
- In VisualAnalog, click the **Settings** button in the **Input Formatter** block (see Figure 7). Check that **Number Format** in the settings of the **Input Formatter** block is set to the correct encoding (offset binary by default). Repeat for the other channel.

If the FFT appears normal but the performance is poor, check the following:

- Make sure that an appropriate filter is used on the analog input.
- Make sure that the signal generators for the clock and the analog input are clean (low phase noise).
- Change the analog input frequency slightly if noncoherent sampling is being used.
- Make sure that the SPI configuration file matches the product being evaluated.

If the FFT window remains blank after **Run** (see Figure 13) is clicked, do the following:

- Make sure that the evaluation board is securely connected to the HSC-ADC-EVALCZ board.
- Make sure that the FPGA has been programmed by verifying that the **DONE** LED is illuminated on the HSC-ADC-EVALCZ board. If this LED is not illuminated, make sure that the U4 switch on the board is in the correct position for USB CONFIG.
- Make sure that the correct FPGA program was installed by clicking the **Settings** button in the **ADC Data Capture** block in **VisualAnalog**. Then select the **FPGA** tab and verify that the proper FPGA bin file is selected for the part.

If VisualAnalog indicates that the data capture timed out, do the following:

- Make sure that all power and USB connections are secure.
- Probe the DCO signal at the ADC on the evaluation board and confirm that a clock signal is present at the ADC sampling rate.

EVALUATION BOARD SCHEMATICS AND ARTWORK

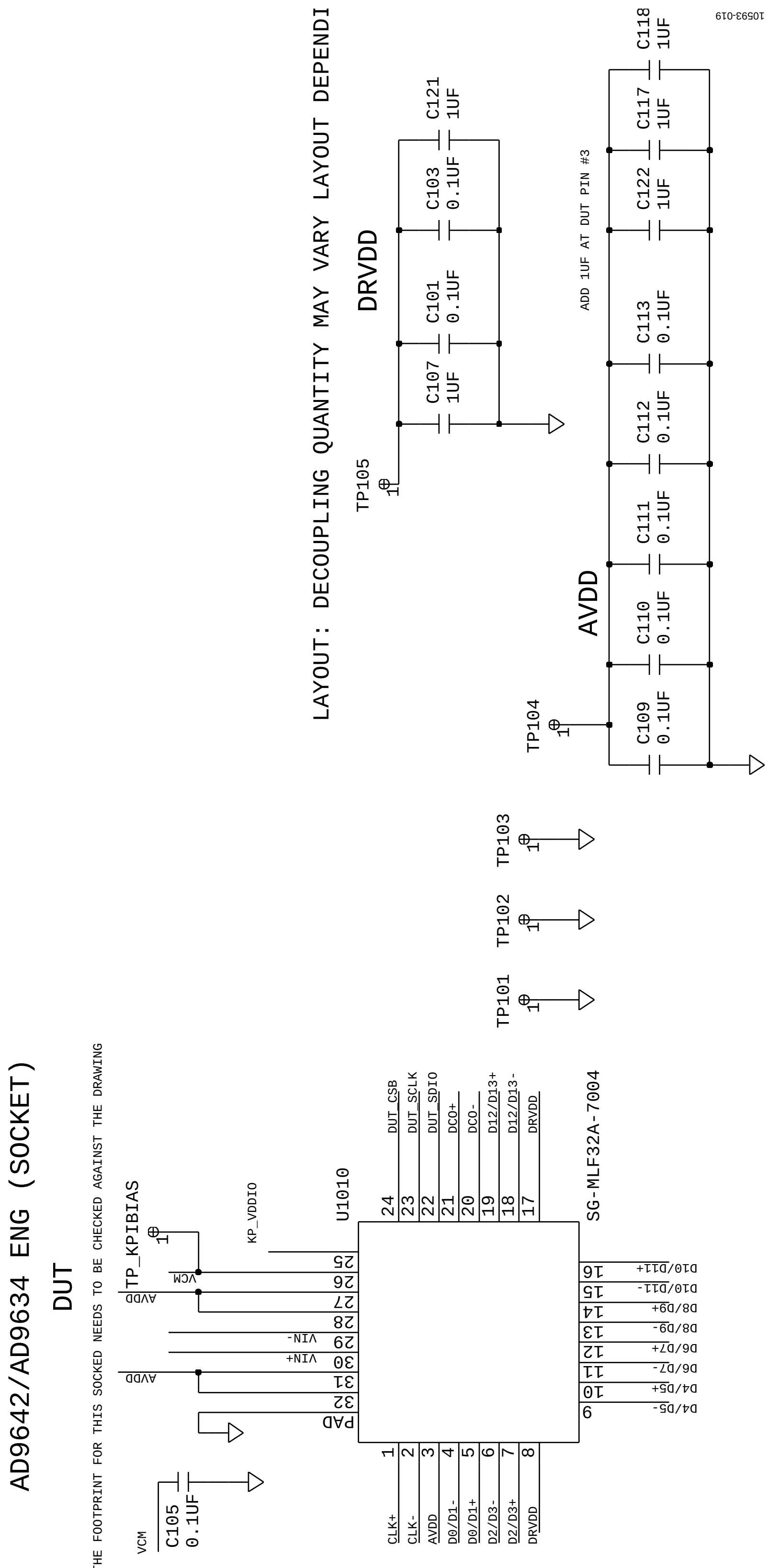


Figure 19. Device Under Test and Related Circuits

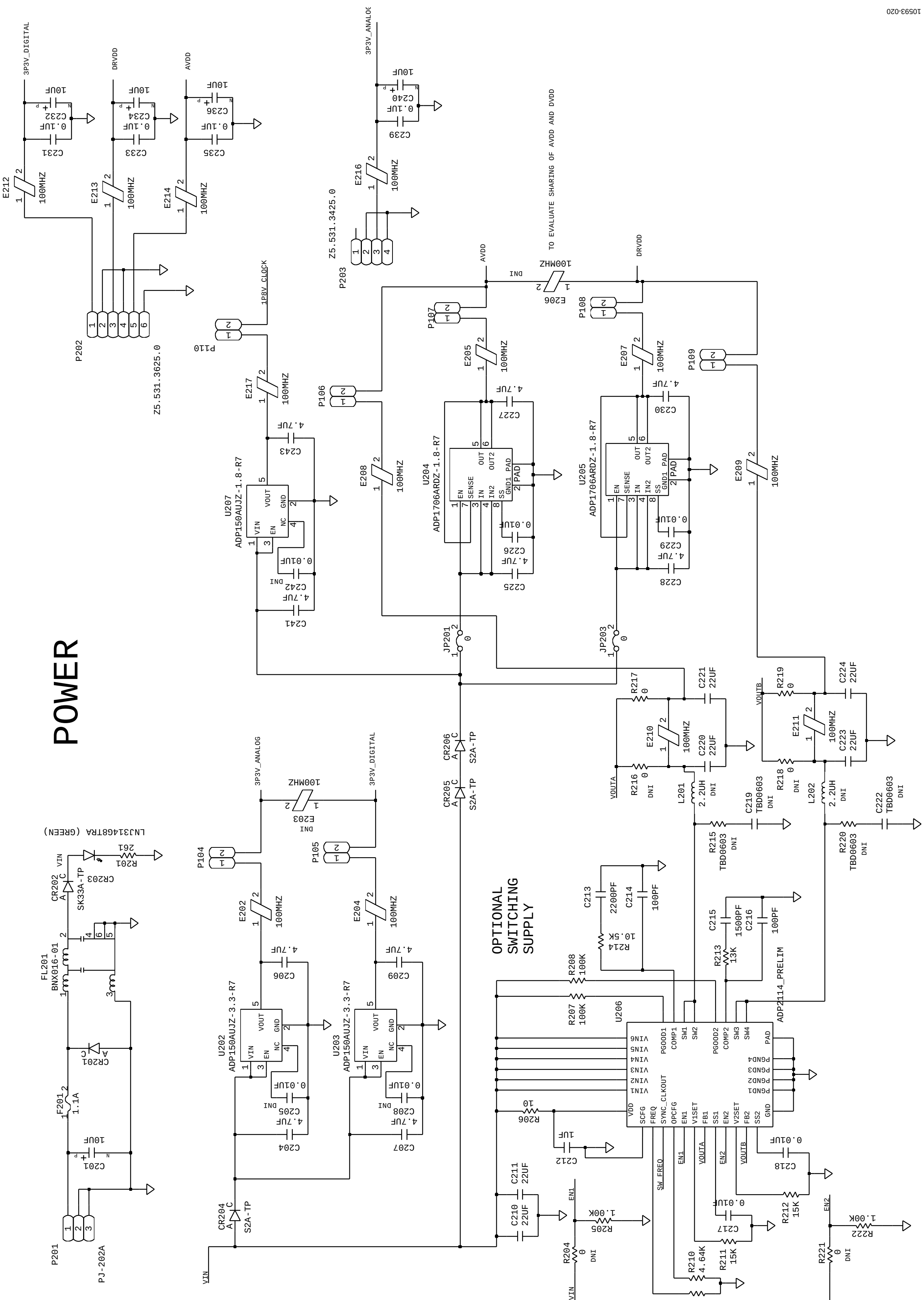


Figure 20. Board Power Input and Supply

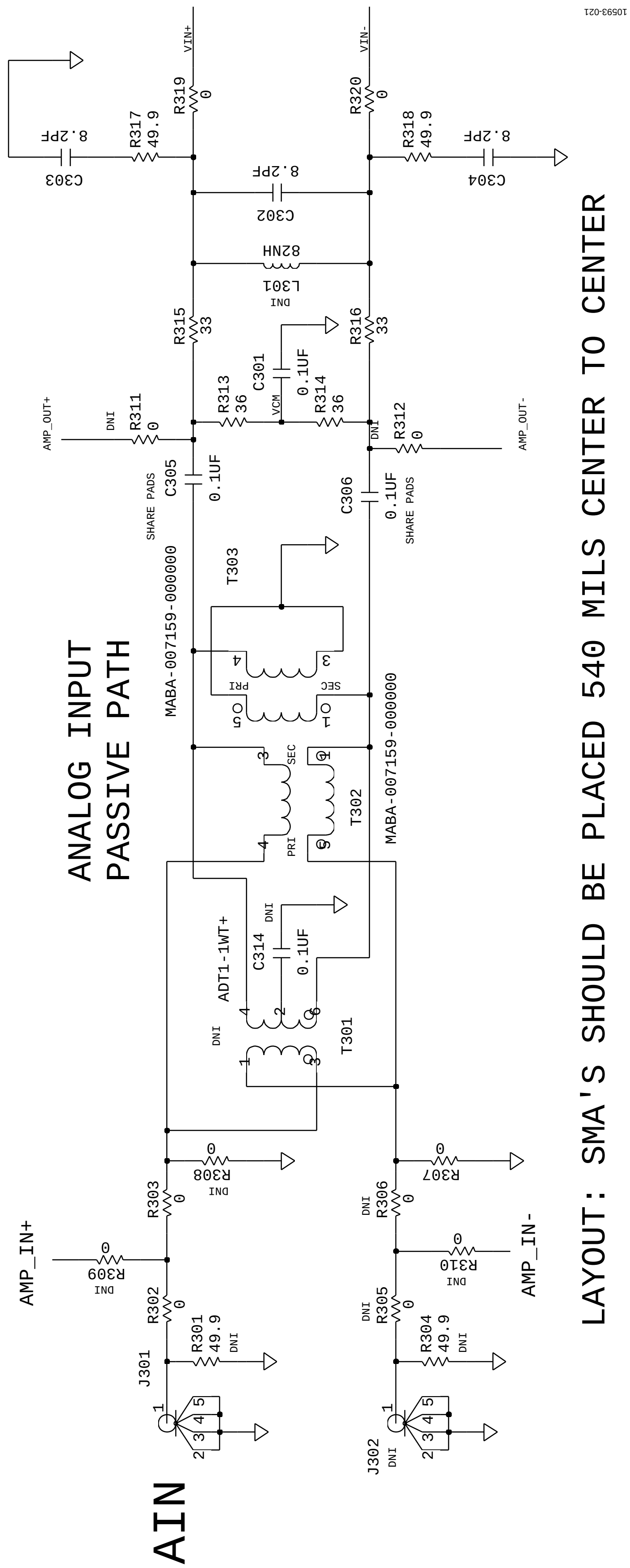


Figure 21. Passive Analog Input Circuits

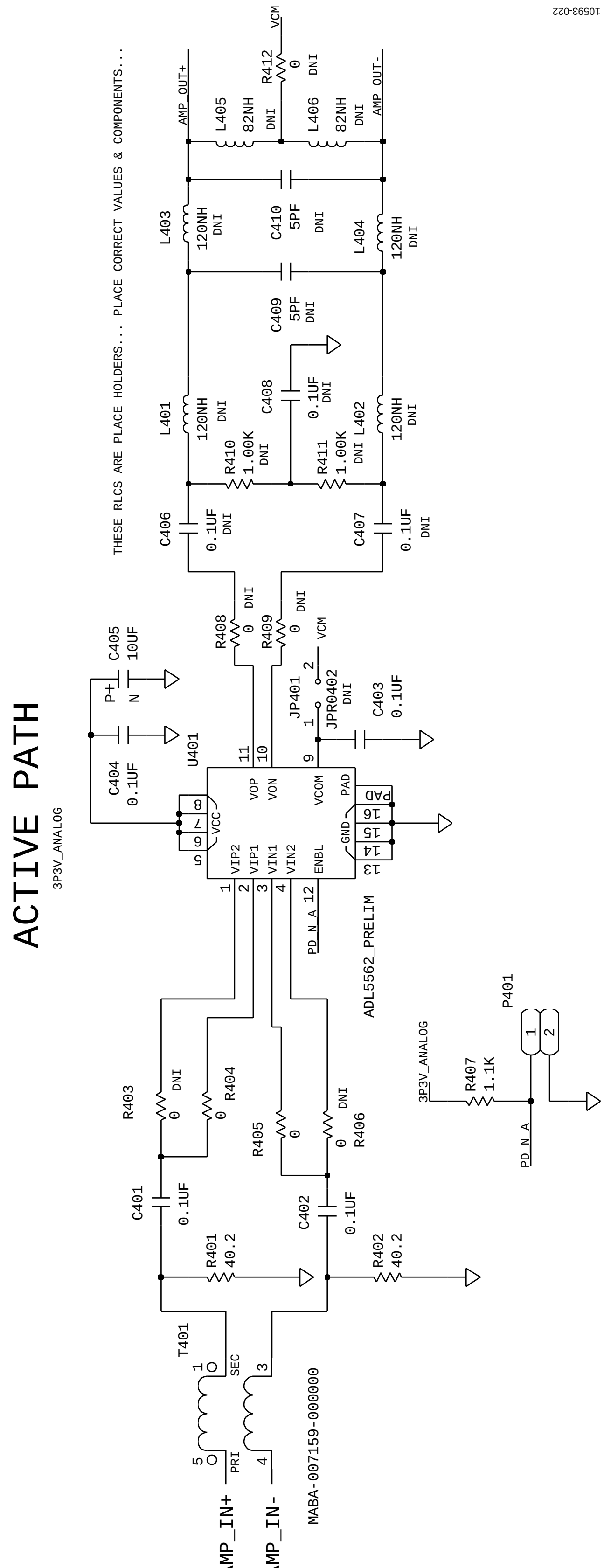


Figure 22. Optional Active Input Circuits

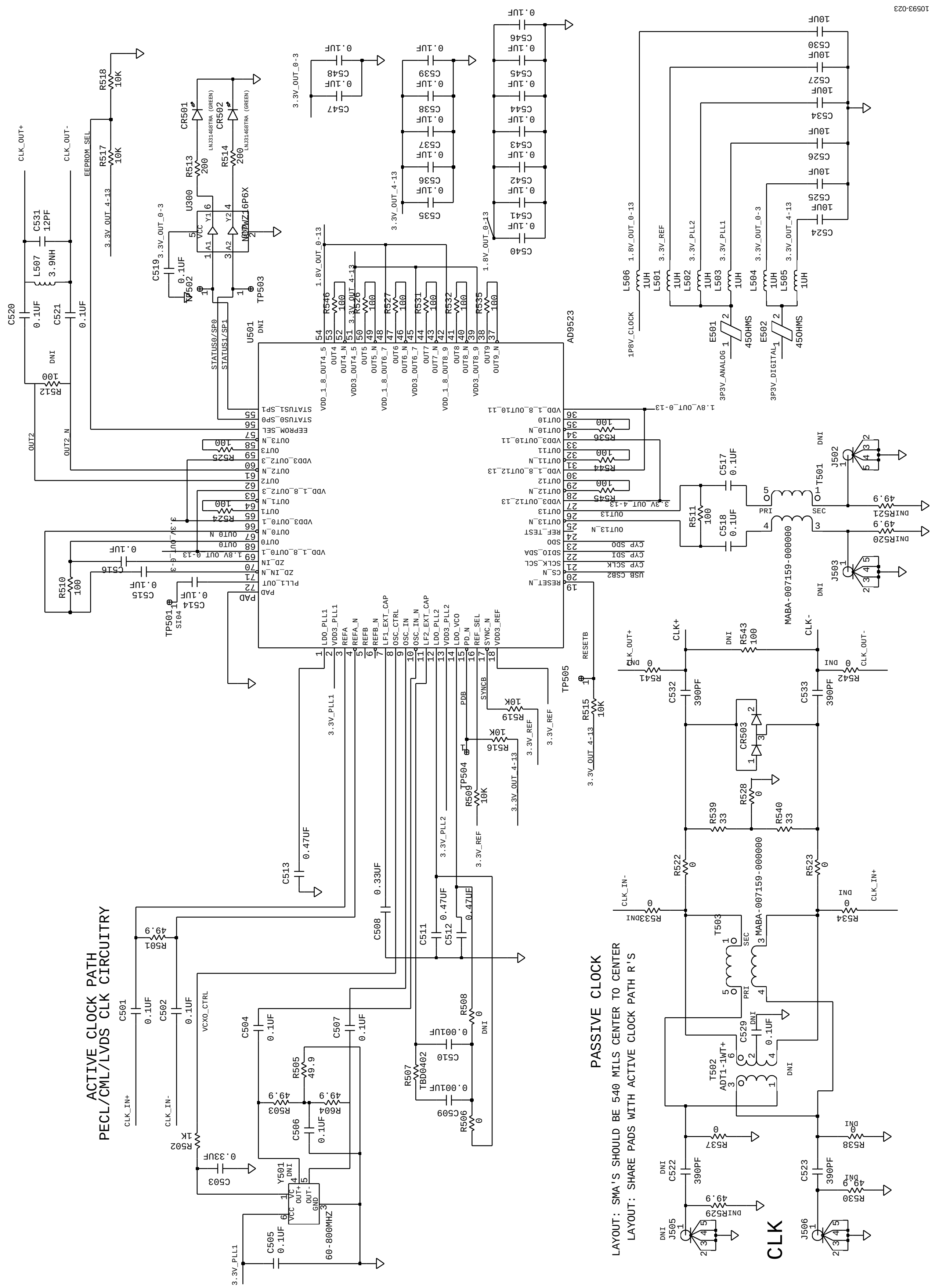


Figure 23. Default and Optional Clock Input Circuits

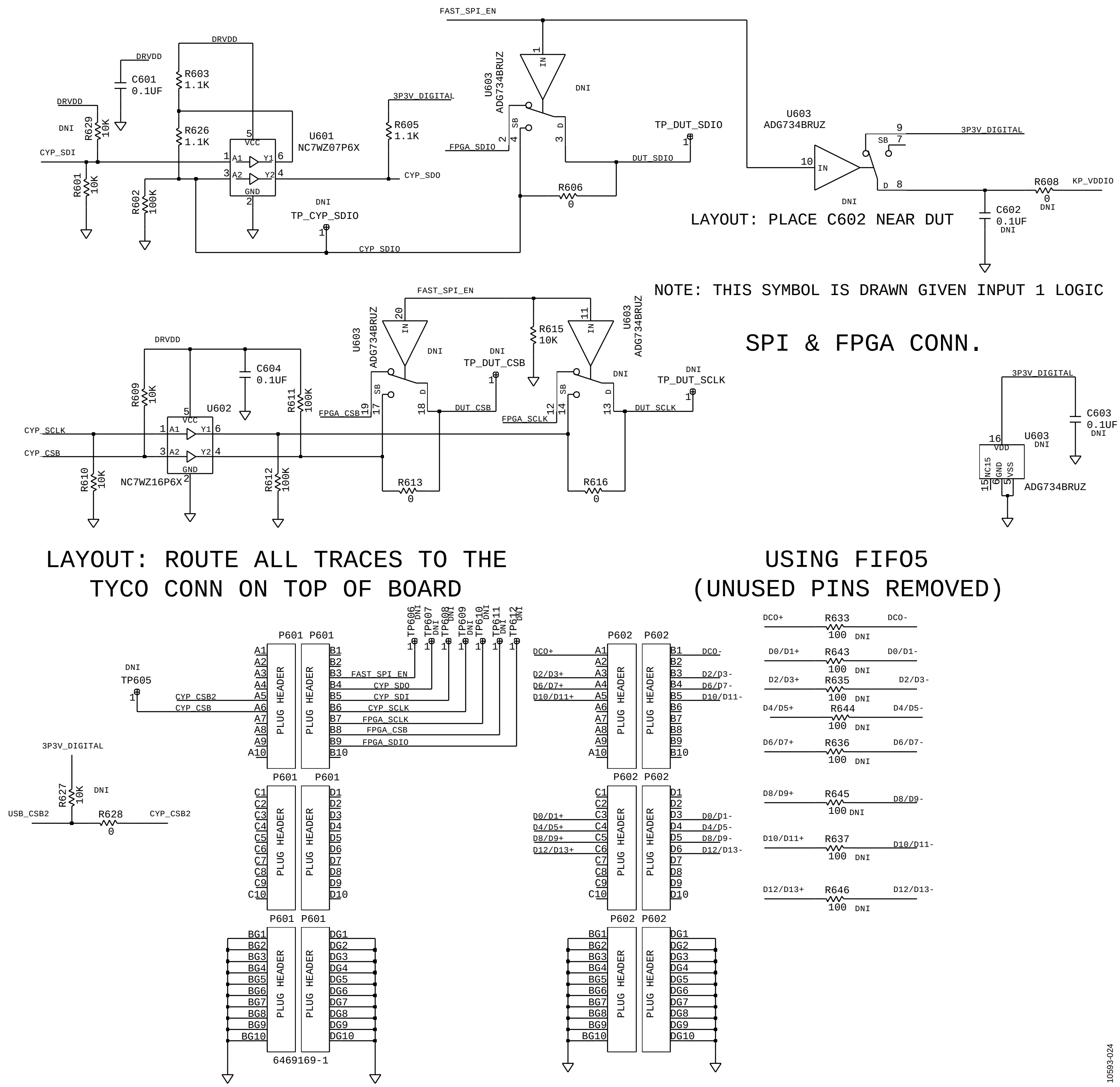


Figure 24. SPI Configuration Circuit and FIFO Board Connector Circuit

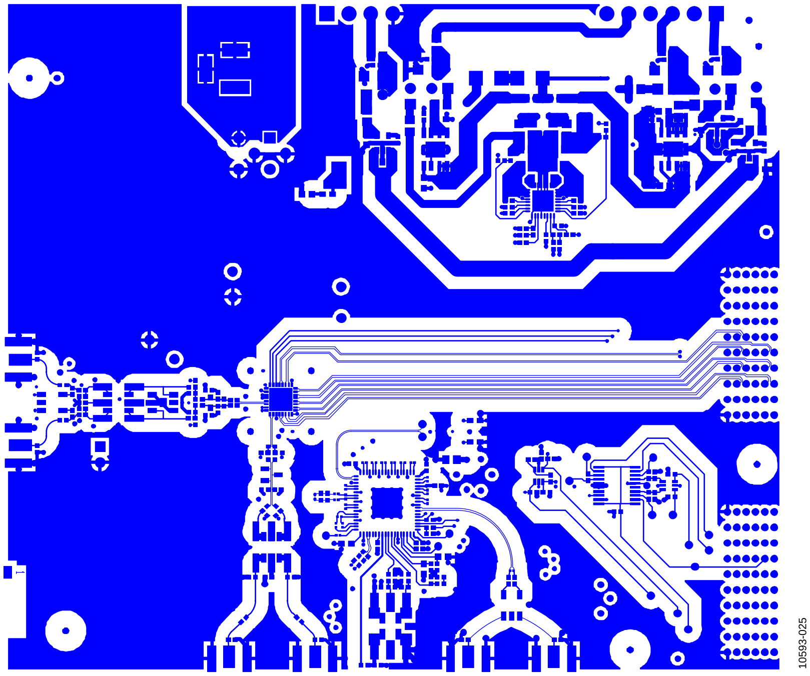


Figure 25. Top Side

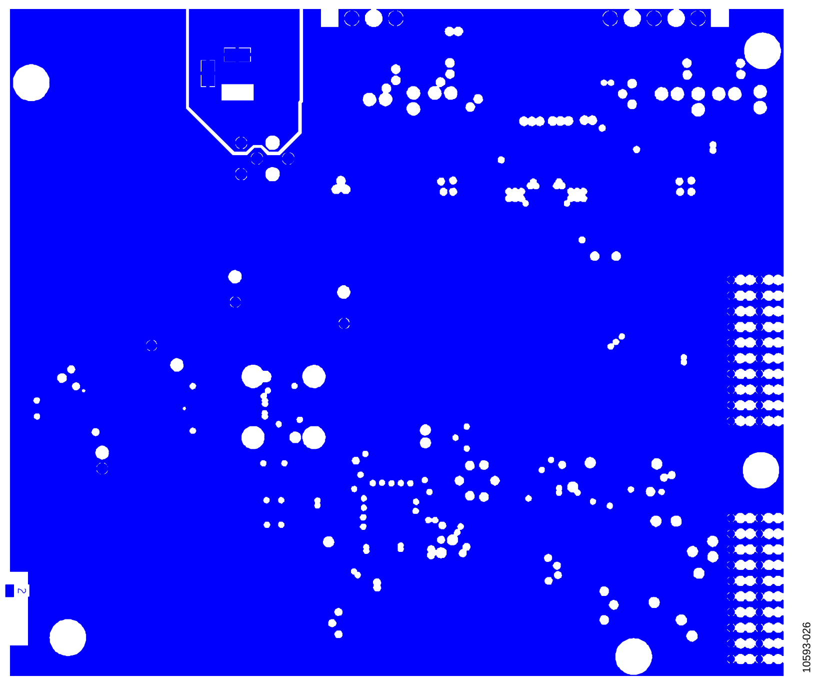


Figure 26. Ground Plane (Layer 2)

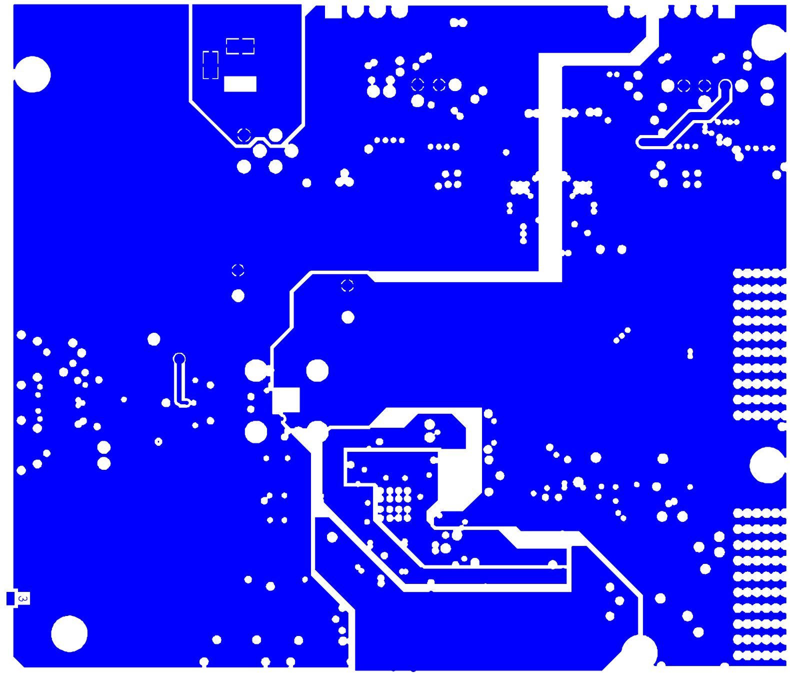


Figure 27. Power Plane (Layer 3)

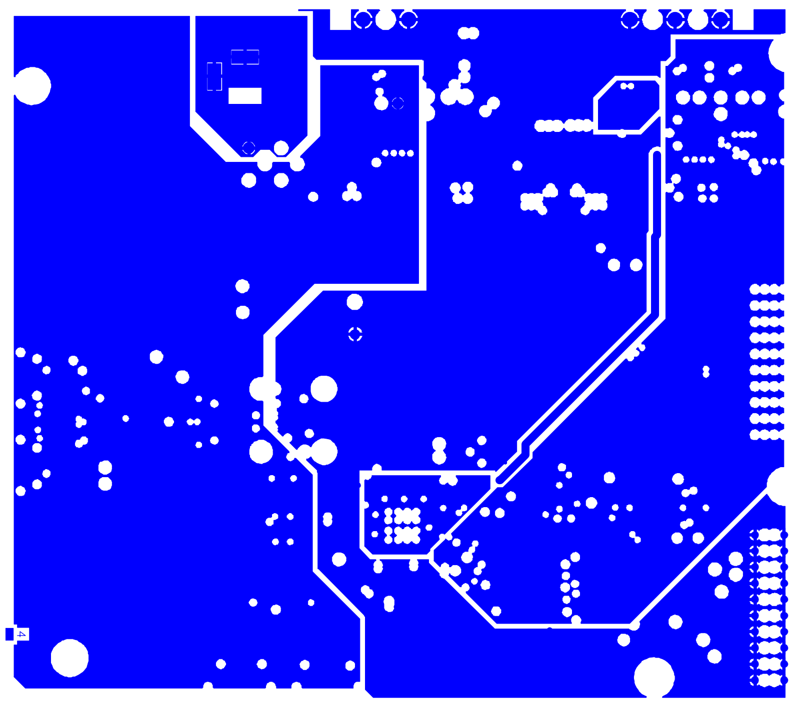


Figure 28. Power Plane (Layer 4)

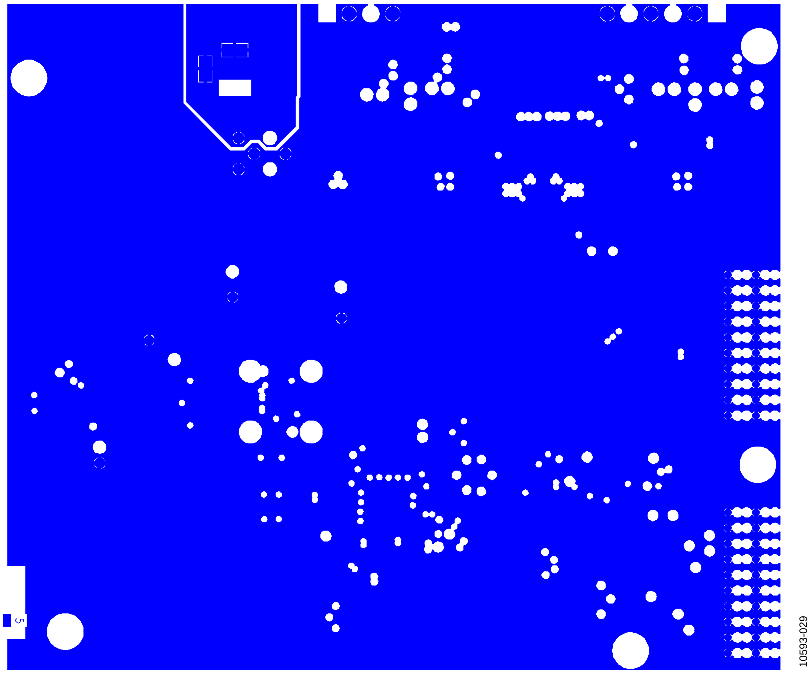


Figure 29. Ground Plane (Layer 5)

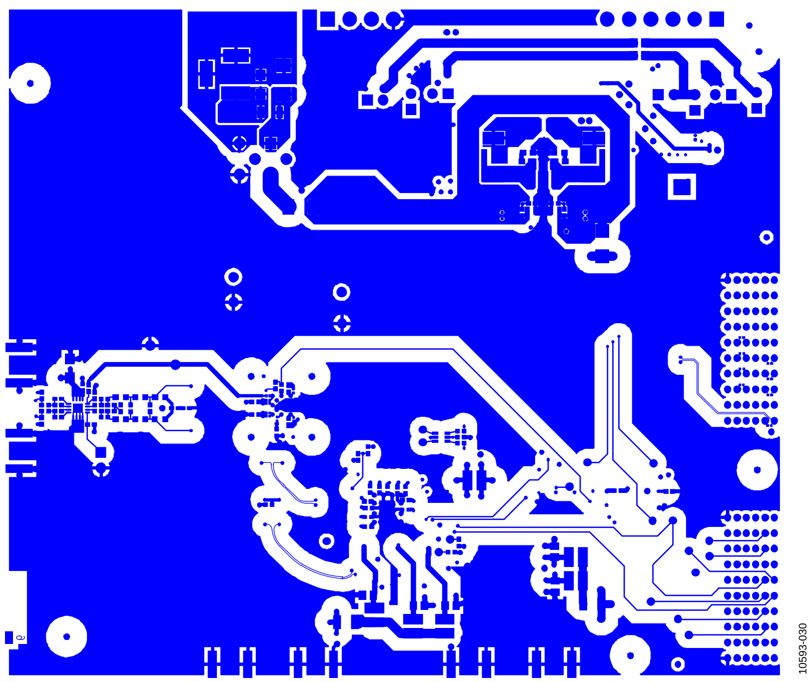


Figure 30. Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. AD9642/AD9634/AD6672 Bill of Materials

Item	Qty	Reference Designator	Description	Manufacturer/Part No.
1	1	N/A	Printed circuit board, AD9642 engineering board	AD9642EE01A
2	13	C101, C103, C105, C109 to C113, C514 to C516, C520, C521	0.1 µF capacitor ceramic X5R 0201	Murata GRM033R60J104KE19D
3	6	C107, C117, C118, C121, C122, C212	1 µF capacitor mono ceramic 0402	Murata GRM155R60J105KE19D
4	6	C201, C232, C234, C236, C240, C405	10 µF capacitor tantalum	AVX TAJA106K010RNJ
5	10	C204, C206, C207, C209, C225, C227, C228, C230, C241, C243	4.7 µF capacitor monolithic ceramic X5R	Murata GRM188R60J475KE19
6	6	C210, C211, C220, C221, C223, C224	22 µF capacitor ceramic chip	Murata GRM21BR60J226ME39L
7	1	C213	2200 pF capacitor ceramic X7R 0402	Phycomp (YAGEO) CC0402KRX7R9BB222
8	2	C214, C216	100 pF capacitor chip mono ceramic C0G 0402	Murata GRM1555C1H101JD01D
9	1	C215	1500 pF capacitor ceramic X7R 0402	Murata GRM155R71H152KA01D
10	4	C217, C218, C226, C229	0.01 µF capacitor ceramic X7R 0402	Murata GRM155R71H103KA01D
11	36	C231, C233, C235, C239, C301, C305, C306, C401 to C404, C501, C502, C504 to C507, C517 to C519, C535 to C548, C601, C604	0.1 µF capacitor ceramic X7R 0402	Murata GRM155R71C104KA88D
12	3	C302 to C304	3.9 pF capacitor ceramic NP0 0402	Murata GRM1555C1H3R9CZ01D
13	2	C503, C508	0.33 µF capacitor ceramic X5R	Murata GRM155R61A334KE15D
14	2	C509, C510	0.001 µF capacitor ceramic monolithic	Murata GRM155R71H102KA01D
15	3	C511 to C513	0.47 µF capacitor chip CER X7R 0603	Murata GCM188R71C474KA55D
16	3	C523, C532, C533	390 pF capacitor ceramic C0G 0402	Murata GRM1555C1H391JA01D
17	6	C524 to C527, C530, C534	10 µF capacitor ceramic monolithic	Murata GRM21BR61C106KE15L
18	1	C531	12 pF capacitor ceramic C0G 0402	Murata GRM1555C1H120JZ01D
19	1	CR201	S1AB-13 diode rectifier GPP SMD	Diode Incorp S1AB-13
20	1	CR202	SK33A-TP diode Schottky 3-amp rectifier	MCC SK33A-TP
21	3	CR204 to CR206	S2A-TP diode recovery rectifier	MICRO Commercial Components CORP S2A-TP
22	2	CR501, CR502	LNJ314G8TRA (green) LED green surface mount	Panasonic LNJ314G8TRA
23	1	CR503	HSMS-2812BLK diode Schottky dual series	Avago HSMS-2812BLK
24	13	E202, E204, E205, E207 to E214, E216, E217	100 MHZ inductor ferrite bead	Panasonic EXC-ML20A390U
25	2	E501, E502	45 Ω chip bead core	Panasonic EXCCL3225U1
26	1	F201	1.1 A fuse poly-switch PTC device 1812	TYCO Electronics NANOSMDC110F-2
27	1	FL201	BNX016-01 FLTR noise suppression LC combined type	Murata BNX016-01
28	2	J301, J506	SMA-J-P-X-ST-EM1 CONN-PCB SMA ST edge mount	Samtec SMA-J-P-X-ST-EM1
29	2	JP201, JP203	0 Ω resistor JMPR SMD 0805 (SHRT)	Panasonic ERJ-6GEYJ0.0
30	6	L501 to L506	1 µH inductor SMT power	Coil-Craft ME3220-102MLB
31	1	L507	3.9 nH inductor SM	Murata LQG15HN3N9S02D
32	8	P104 to P110, P401	TSW-102-08-G-S CONN-PCB header 2 POS	Samtec TSW-102-08-G-S
33	1	P201	PJ-202A CONN-PCB DC power jack SM	CUI Stack PJ-202A
34	1	P202	Z5.531.3625.0 CONN-PCB header 6-position	Wieland Z5.531.3625.0
35	1	P203	Z5.531.3425.0 CONN-PCB, pluggable header	Wieland Z5.531.3425.0

Item	Qty	Reference Designator	Description	Manufacturer/Part No.
36	2	P601, P602	6469169-1 CONN_PCB 60PIN RA connector	TYCO 6469169-1
37	1	R201	261 resistor film chip thick	NIC COMP CORP NRC06F2610TRF
38	2	R205, R222	1.00 kΩ resistor precision thick film chip R0402	Panasonic ERJ-2RKF1001X
39	1	R206	10 Ω resistor precision thick film chip R0402	Panasonic ERJ-2RKF10R0X
40	5	R207, R208, R602, R611, R612	100 kΩ resistor precision thick film chip R0402	Panasonic ERJ-2RKF1003X
41	1	R209	27 kΩ resistor chip SMD 0402	Panasonic ERJ-2RKF2702X
42	1	R210	4.64 Ω resistor precision thick film chip R0402	Panasonic ERJ-2RKF4641X
43	2	R211, R212	15 kΩ resistor chip SMD 0402	Panasonic ERJ-2RKF1502X
44	1	R213	13 kΩ resistor film SMD 0402	Yageo 9C04021A1302FLHF3
45	1	R214	10.5 kΩ resistor precision thick film chip R0402	Panasonic ERJ-2RKF1052X
46	14	R217, R219, R302, R303, R307, R319, R320, R404, R405, R506, R522, R523, R528, R537	0 Ω resistor film SMD 0402	Panasonic ERJ-2GE0R00X
47	2	R313, R314	36 Ω resistor film SMD 0402	Panasonic ERJ-2GEJ360X
48	2	R315, R316	15 Ω resistor film SMD 0402	Panasonic ERJ-2RFK15R0X
49	6	R317, R318, R501, R503, R505, R604	49.9 Ω resistor precision thick film chip R0402	Panasonic ERJ-2RKF49R9X
50	2	R401, R402	40.2 Ω resistor precision thick film chip R0402	Panasonic ERJ-2RKF40R2X
51	4	R407, R603, R605, R626	1.1 kΩ resistor film SMD 0402	Panasonic ERJ-2GEJ112X
52	1	R507	TBD0402 do not install (TBD_R0402)	TBD0402
53	10	R509, R515 to R519, R601, R609, R610, R615	10 kΩ resistor precision thick film chip R0402	Panasonic ERJ-2RKF1002X
54	13	R510, R511, R524 to R527, R531, R532, R535, R536, R544 to R546	100 Ω resistor precision thick film chip R0201	Panasonic ERJ-1GEF1000C
55	2	R513, R514	200 Ω resistor precision thick film chip R0402	Panasonic ERJ-2RKF2000X
56	4	R606, R613, R616, R628	0 Ω resistor thick film chip	Multicomp 0402WGF0000TCE
57	5	T302, T303, T401, T501, T503	MABA-007159-000000 XFMR RF 1:1	MACOM MABA-007159-000000
58	1	U1010	SG-MLF32A-7004 socket 32P MLF direct mount	Ironwood Electronics SG-MLF32A-7004
59	2	U202, U203	ADP150AUJZ-3.3-R7 IC CMOS linear regulator LDO 3.3 V	Analog Devices ADP150AUJZ-3.3-R7
60	2	U204, U205	ADP1706ARDZ-1.8-R7 IC low dropout CMOS linear regulator	Analog Devices ADP1706ARDZ-1.8-R7
61	1	U206	ADP2114 IC dual configurable synchronous PWM step-down regulator	Analog Devices ADP2114
62	1	U207	ADP150AUJZ-1.8-R7 IC CMOS linear regulator LDO 1.8 V	Analog Devices ADP150AUJZ-1.8-R7
63	2	U300, U602	NC7WZ16P6X IC tiny logic UHS dual buffer	Fairchild NC7WZ16P6X
64	1	U401	ADL5562 IC 2.6 GHZ ultralow distortion DIFF IF/RF amp	Analog Devices ADL5562
65	1	U601	NC7WZ07P6X IC tiny logic UHS dual buffer	Fairchild NC7WZ07P6X
66	1	C602	0.1 µF capacitor ceramic X7R 0402	Murata GRM155R71C104KA88D
67	1	CR203	LNJ314G8TRA (green) LED green surface mount	Panasonic LNJ314G8TRA
68	1	R502	1 kΩ resistor ultraprecision ultrareliability MF chip	SUSUMU RG1005P-102-B-T5
69	2	R539, R540	33 Ω resistor high PRES, high stability	Yageo RT0402DRE0733RL
70	1	U501	AD9523 IC	Analog Devices AD9523
71[1]		C205, C208, C242	0.01 µF capacitor ceramic X7R 0402	Murata GRM155R71H103KA01D
72[1]		C219, C222	TBD0603 do not install (TBD_C0603)	TBD0603

Item	Qty	Reference Designator	Description	Manufacturer/Part No.
73[1]		C314, C406 to C408, C529, C603	0.1 µF capacitor ceramic X7R 0402	Murata GRM155R71C104KA88D
74[1]		C409, C410	5 pF capacitor	Panasonic ECU-E1H050CCQ
75[1]		C522	390 pF capacitor ceramic C0G 0402	Murata GRM1555C1H391JA01D
76[1]		E203, E206	100 MHZ inductor ferrite bead	Panasonic EXC-ML20A390U
77[1]		J302, J502, J503, J505	SMA-J-P-X-ST-EM1 CONN-PCB SMA ST edge mount	Samtec SMA-J-P-X-ST-EM1
78[1]		L201, L202	2.2 µH inductor SM	Toko FDV0630-2R2M
79[1]		L301, L405, L406	82 nH inductor SM	Murata LQW18AN82NG00D
80[1]		L401 to L404	120 nH inductor SM	Panasonic ELJ-RER12JF3
81[1]		R204, R216, R218, R221, R305, R306, R308 to R312, R403, R406, R408, R409, R412, R508, R533, R534, R538, R541, R542, R608	0 Ω resistor film SMD 0402	Panasonic ERJ-2GE0R00X
82[1]		R215, R220	TBD0603 do not install (TBD_R0603)	TBD0603
83[1]		R301, R304, R520, R521, R529, R530	49.9 Ω resistor PREC thick film chip R0402	Panasonic ERJ-2RKF49R9X
84[1]		R410, R411	1.00 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1001X
85[1]		R512, R633, R635 to R637, R643 to R646	100 Ω resistor PREC thick film chip R0201	Panasonic ERJ-1GEF1000C
86[1]		R543	100 Ω resistor film SMD 0402	Venkel CR0402-16W-1000FPT
87[1]		R627, R629	10 kΩ resistor PREC thick film chip R0402	Panasonic ERJ-2RKF1002X
88[1]		T301, T502	ADT1-1WT+ XFMR RF	Mini Circuits ADT1-1WT+
89[1]		U603	Quad SPDT switches IC CMOS	Analog Devices ADG734BRUZ
90[1]		Y501	60 MHz to 800 MHz IC oscillator voltage controlled OSC	Epson Toyocom TCO-2111

[1] Do not install.

RELATED LINKS

Resource	Description
AD6672	Product Page, 11-Bit, 250 MSPS, 1.8 V IF Diversity Receiver
AD9634	Product Page, 12-bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter (ADC)
AD9642	Product Page, 14-Bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V Analog-to-Digital Converter (ADC)
ADP2114	Product Page, Configurable, Dual 2 A/Single 4 A, Synchronous Step-Down DC-to-DC Regulator
AD9523	Product Page, 14-Output, Low Jitter Clock generator
ADG734	Product Page, CMOS, 2.5 Ω Low Voltage, Quad SPDT Switch
AN-878	Application Note, High Speed ADC SPI Control Software
AN-877	Application Note, Interfacing to High Speed ADCs via SPI
AN-835	Application Note, Understanding High Speed ADC Testing and Evaluation
AN-905	Application Note, VisualAnalog™ Converter Evaluation Tool Version 1.0 User Manual

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ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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