

Vishay High Power Products

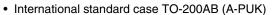
Phase Control Thyristors (Hockey PUK Version), 350 A



TO-200AB (A-PUK)

FEATURES

- · Center amplifying gate
- Metal case with ceramic insulator





• Designed and qualified for industrial level



ROHS

PRODUCT SUMMARY			
I _{T(AV)}	350 A		

TYPICAL APPLICATIONS

- · DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS						
PARAMETER	TEST CONDITIONS	VALUES	UNITS			
1		350	A			
I _{T(AV)}	T _{hs}	55	°C			
1		660	A			
I _T (RMS)	T _{hs}	25	°C			
	50 Hz	5000	Α Α			
I _{TSM}	60 Hz	5230	^			
17.	50 Hz	125	- kA ² s			
l ² t	60 Hz	114	- KA-S			
V _{DRM} /V _{RRM}		400 to 2000	V			
tq	Typical	100	μs			
TJ		- 40 to 125	°C			

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS								
TYPE NUMBER	VOLTAGE CODE	V _{DRM} /V _{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$\begin{aligned} I_{DRM}/I_{RRM} & \text{MAXIMUM} \\ \text{AT T}_{J} &= T_{J} & \text{MAXIMUM} \\ & \text{mA} \end{aligned}$				
	04	400	500					
	08	800	900					
ST180CC	12	1200	1300	30				
16		1600	1700					
		1800	1900					
	20	2000	2100					

ST180CPbF Series

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ABSOLUTE MAXIMUM RATIN	GS					
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current		180° condu	ction, half sine v	vave	350 (140)	Α
at heatsink temperature	I _{T(AV)}	double side	(single side) co	oled	55 (85)	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 25 °C	heatsink tempe	erature double side cooled	660	
		t = 10 ms	No voltage		5000	
Maximum peak, one-cycle		t = 8.3 ms	reapplied		5230	A kA ² s
non-repetitive surge current	I _{TSM}	t = 10 ms	100 % V _{RRM}	Sinusoidal half wave, initial $T_J = T_J$ maximum	4200	
		t = 8.3 ms	reapplied		4400	
Maximum I ² t for fusing	l ² t	t = 10 ms	No voltage		125	
		t = 8.3 ms	reapplied		114	
		t = 10 ms	100 % V _{RRM}		88	
		t = 8.3 ms	reapplied		81	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10	t = 0.1 to 10 ms, no voltage reapplied			kA²√s
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % x π	x I _{T(AV)} < I < π x	$I_{T(AV)}$, $T_J = T_J$ maximum	1.08	V
High level value of threshold voltage	V _{T(TO)2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			1.14	V
Low level value of on-state slope resistance	r _{t1}	$(16.7 \% \text{ x } \pi \text{ x } I_{T(AV)} < I < \pi \text{ x } I_{T(AV)}), T_J = T_J \text{ maximum}$			1.18	0
High level value of on-state slope resistance	r _{t2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$			1.14	mΩ
Maximum on-state voltage	V_{TM}	$I_{pk} = 750 \text{ A}, T_J = T_J \text{ maximum}, t_p = 10 \text{ ms sine pulse}$			1.96	٧
Maximum holding current	I _H	T 05.00			600	A
Maximum (typical) latching current	ΙL	T _J = 25 °C, anode supply 12 V resistive load			1000 (300)	mA

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω , $t_r \le 1~\mu s$ $T_J = T_J$ maximum, anode voltage $\le 80~\%~V_{DRM}$	1000	A/µs
Typical delay time	t _d	Gate current 1 A, $dl_g/dt = 1$ A/ μ s $V_d = 0.67 \% V_{DRM}$, $T_J = 25 \ ^{\circ}C$	1.0	
Typical turn-off time	tq	$I_{TM} = 300 \text{ A, } T_J = T_J \text{ maximum, } dI/dt = 20 \text{ A/}\mu\text{s,}$ $V_R = 50 \text{ V, } dV/dt = 20 \text{ V/}\mu\text{s, } \text{gate } 0 \text{ V } 100 \Omega, t_p = 500 \mu\text{s}$	100	μs

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 80 % rated V_{DRM}	500	V/µs
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	30	mA



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TRIGGERING						
PARAMETER	SYMBOL		TEGT COURTIONS			
PARAMETER	STWIBUL	'	TEST CONDITIONS	TYP.	MAX.	UNITS
Maximum peak gate power	P _{GM}	$T_J = T_J$ maximum,	$t_p \le 5 \text{ ms}$	1	0	W
Maximum average gate power	P _{G(AV)}	$T_J = T_J$ maximum,	f = 50 Hz, d% = 50	2	.0] vv
Maximum peak positive gate current	I _{GM}			3	.0	Α
Maximum peak positive gate voltage	+ V _{GM}	$T_J = T_J$ maximum, $t_p \le 5$ ms		20	V	
Maximum peak negative gate voltage	- V _{GM}					ן י ן
	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/	180	-	
DC gate current required to trigger		T _J = 25 °C		90	150	mA
		T _J = 125 °C	current/voltage are the lowest value	40	-	
		T _J = - 40 °C	which will trigger all units 12 V	2.9	-	
DC gate voltage required to trigger	V_{GT}	T _J = 25 °C	anode to cathode applied	1.8	3.0	V
		T _J = 125 °C		1.2	-	
DC gate current not to trigger	I _{GD}	$T_{.1} = T_{.1} \text{ maximum}$	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with	10		mA
DC gate voltage not to trigger	V _{GD}	ij = ijmaximum	rated V _{DRM} anode to cathode applied	0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum operating junction temperature range	TJ		- 40 to 125	°C		
Maximum storage temperature range	T _{Stg}		- 40 to 150			
Maximum thermal resistance,	R _{th,J-hs}	DC operation single side cooled	0.17			
junction to heatsink	□thJ-hs	DC operation double side cooled	0.08	K/W		
Maximum thermal resistance,	В	DC operation single side cooled	0.033	10,00		
case to heatsink	R _{thC-hs}	DC operation double side cooled	0.017			
Mounting force, ± 10 %			4900 (500)	N (kg)		
Approximate weight			50	g		
Case style		See dimensions - link at the end of datasheet	TO-200AB (/	A-PUK)		

△R _{thJC} CONDUCTION							
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		CONDUCTION		TEST CONDITIONS	UNITS	
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE			
180°	0.015	0.015	0.011	0.011			
120°	0.018	0.019	0.019	0.019	$T_J = T_J$ maximum		
90°	0.024	0.024	0.026	0.026		K/W	
60°	0.035	0.035	0.036	0.037			
30°	0.060	0.060	0.060	0.061			

Note

• The table above shows the increment of thermal resistance RthJC when devices operate at different conduction angles than DC

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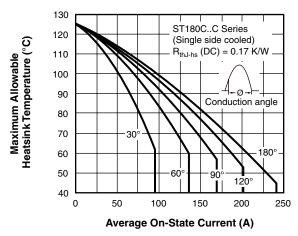


Fig. 1 - Current Ratings Characteristics

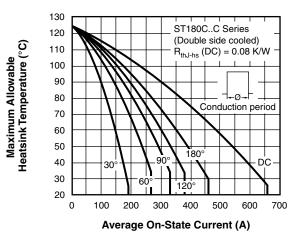


Fig. 4 - Current Ratings Characteristics

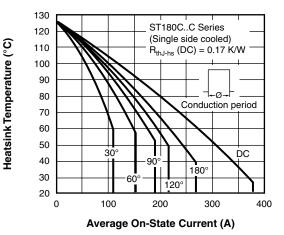


Fig. 2 - Current Ratings Characteristics

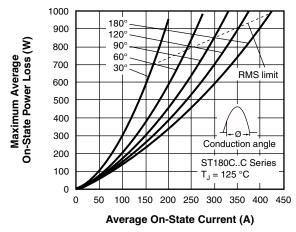


Fig. 5 - On-State Power Loss Characteristics

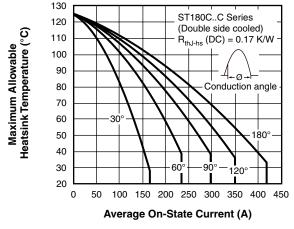


Fig. 3 - Current Ratings Characteristics

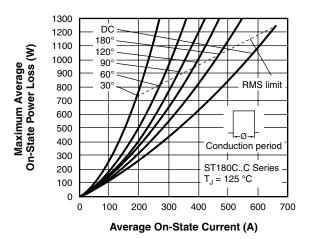


Fig. 6 - On-State Power Loss Characteristics

Maximum Allowable



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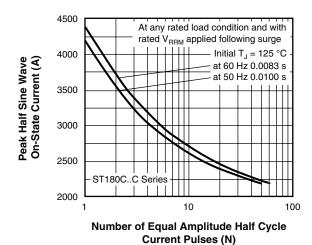


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

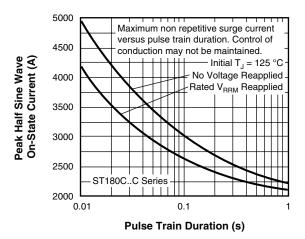


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

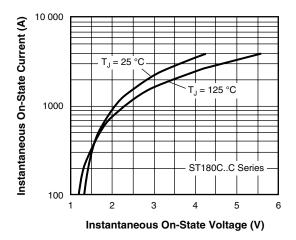


Fig. 9 - On-State Voltage Drop Characteristics

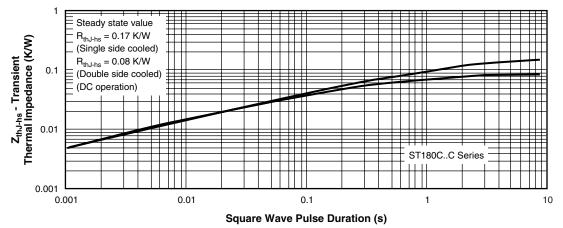


Fig. 10 - Thermal Impedance $Z_{thJ\text{-}hs}$ Characteristics

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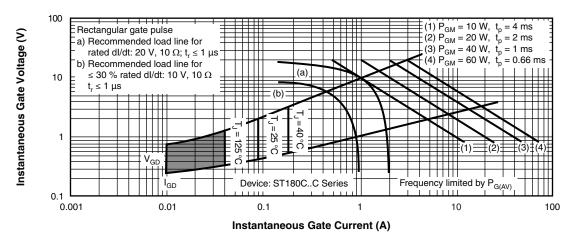
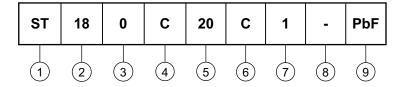


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code



- **Thyristor**
- Essential part number
- 0 = Converter grade
- C = Ceramic PUK
- Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- C = PUK case TO-200AB (A-PUK)
- 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
 - 1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
 - 2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
 - 3 = Fast-on terminals (gate and auxiliary cathode soldered leads)
- 8 Critical dV/dt: • None = 500 V/µs (standard selection)
 - L = 1000 V/µs (special selection)
- 9 Lead (Pb)-free

LINKS TO RELATED DOCUMENTS				
Dimensions	http://www.vishay.com/doc?95074			



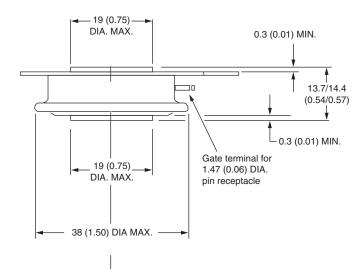
Vishay Semiconductors

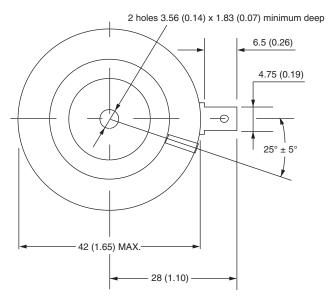
TO-200AB (A-PUK)

DIMENSIONS in millimeters (inches)

Anode to gate

Creepage distance: 7.62 (0.30) minimum Strike distance: 7.12 (0.28) minimum





Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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