



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ High input impedance and high gain
- ▶ Excellent thermal stability
- ▶ Integral source-to-drain diode

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### General Description

The Supertex VP0550 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package	Wafer / Die Options		
	TO-92	NW (Die in wafer form)	NJ (Die on adhesive tape)	ND (Die in waffle pack)
VP0550	VP0550N3-G	VP1550NW	VP1550NJ	VP1550ND

For packaged products, -G indicates package is RoHS compliant ('Green'). Devices in Wafer / Die form are RoHS compliant ('Green'). Refer to Die Specification VF15 for layout and dimensions.

### Product Summary

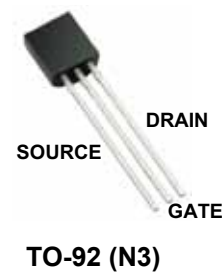
Device	$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$I_{D(ON)}$ (min) (mA)
VP0550N3-G	-500	125	-100

### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

### Pin Configuration



### Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

**TO-92 (N3)**

### Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (mA)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{ja}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}^\dagger$ (mA)	$I_{DRM}$ (mA)
TO-92	-54	-250	1.0	125	170	-54	-250

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

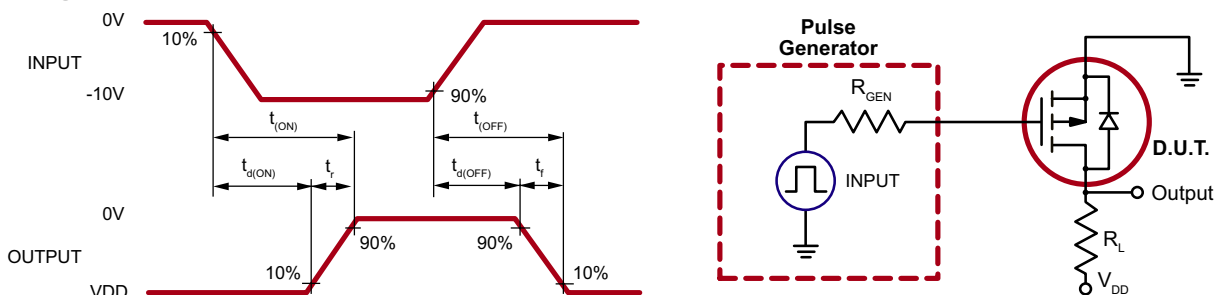
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	-500	-	-	V	$V_{GS} = 0V, I_D = -1.0mA$
$V_{GS(th)}$	Gate threshold voltage	-2.0	-	-4.5	V	$V_{GS} = V_{DS}, I_D = -1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	3.5	6.0	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = -1.0mA$
$I_{GSS}$	Gate body leakage current	-	-	-100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
$I_{DSS}$	Zero gate voltage drain current	-	-	-10	$\mu\text{A}$	$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
		-	-	-1000		$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	-	-90	-	mA	$V_{GS} = -5.0V, V_{DS} = -25V$
		-100	-240	-		$V_{GS} = -10V, V_{DS} = -25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	85	-	$\Omega$	$V_{GS} = -5.0V, I_D = -5mA$
		-	80	125		$V_{GS} = -10V, I_D = -10mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.85	-	%/ $^\circ\text{C}$	$V_{GS} = -10V, I_D = -10mA$
$G_{FS}$	Forward transconductance	25	40	-	mmho	$V_{DS} = -25V, I_D = -10mA$
$C_{ISS}$	Input capacitance	-	40	70	pF	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	10	20		
$C_{RSS}$	Reverse transfer capacitance	-	3.0	10		
$t_{d(ON)}$	Turn-on delay time	-	5.0	10	ns	$V_{DD} = -25V, I_D = -100mA, R_{GEN} = 25\Omega$
$t_r$	Rise time	-	8.0	10		
$t_{d(OFF)}$	Turn-off delay time	-	8.0	15		
$t_f$	Fall time	-	5.0	16		
$V_{SD}$	Diode forward voltage drop	-	-0.8	-1.5	V	$V_{GS} = 0V, I_{SD} = -0.1A$
$t_{rr}$	Reverse recovery time	-	200	-	ns	$V_{GS} = 0V, I_{SD} = -0.1A$

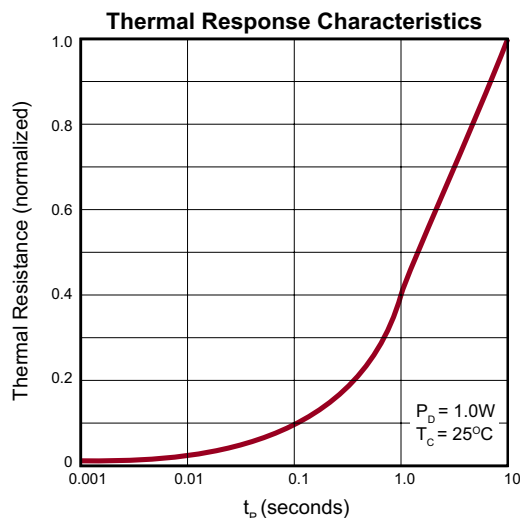
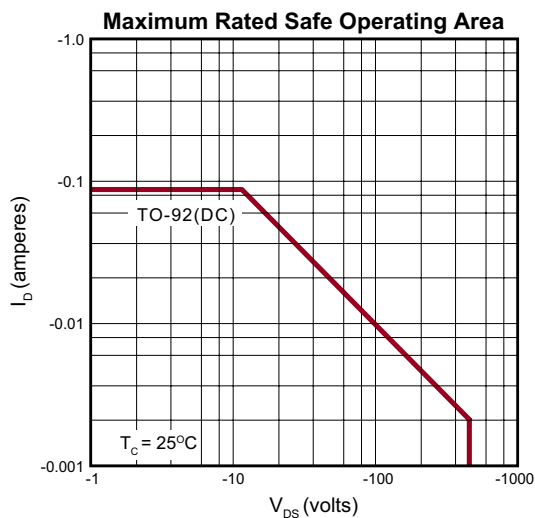
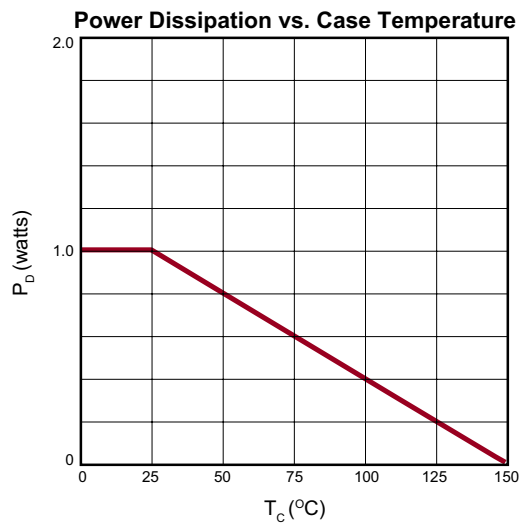
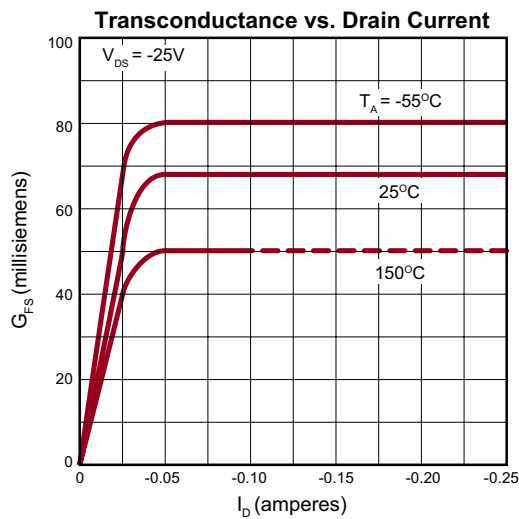
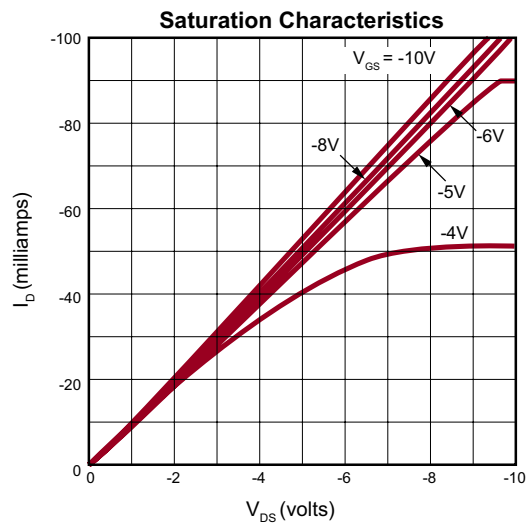
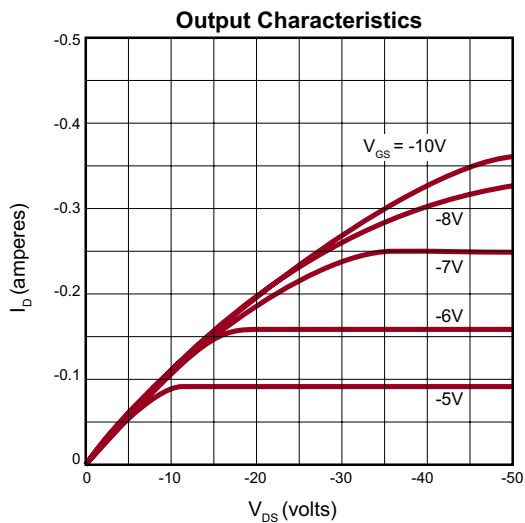
**Notes:**

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

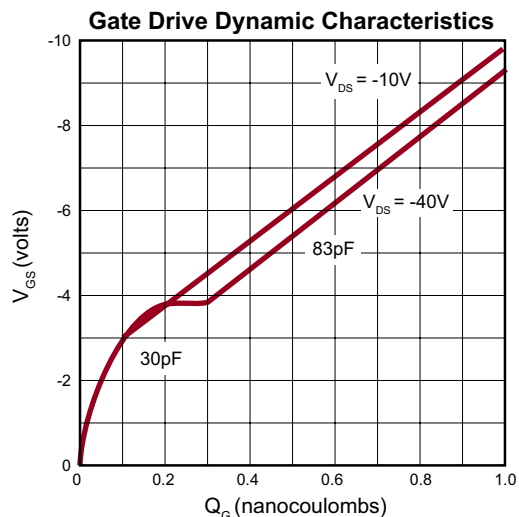
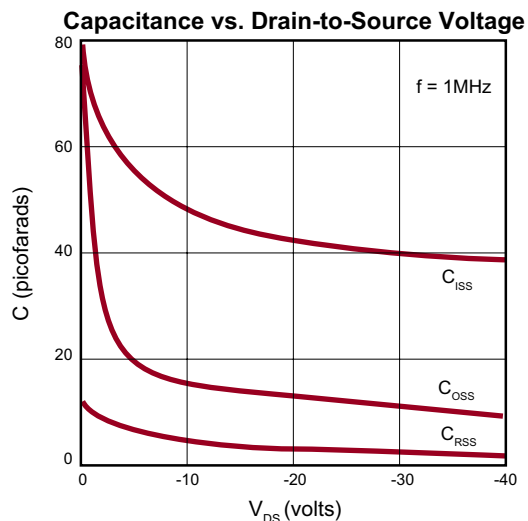
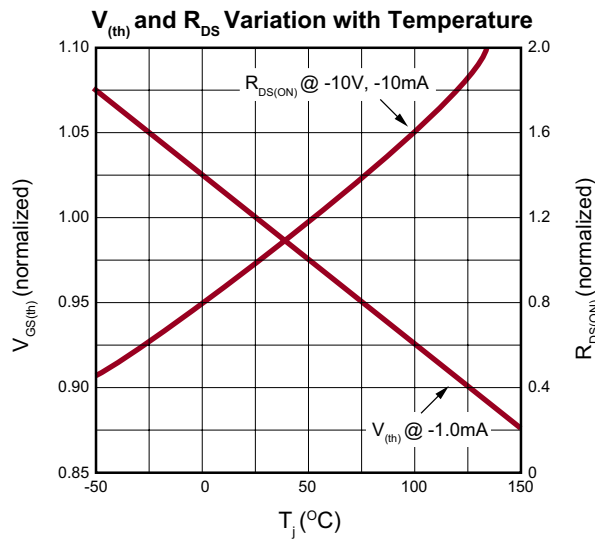
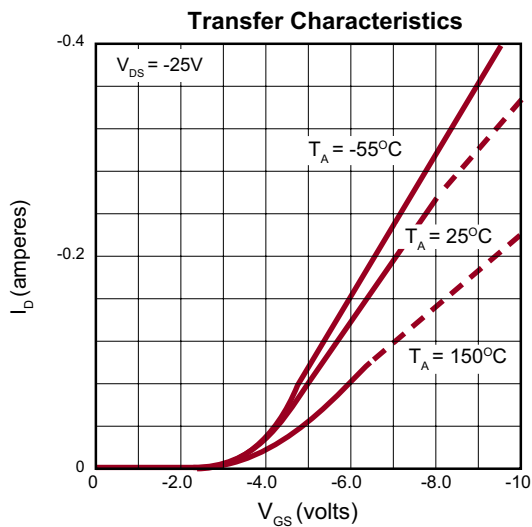
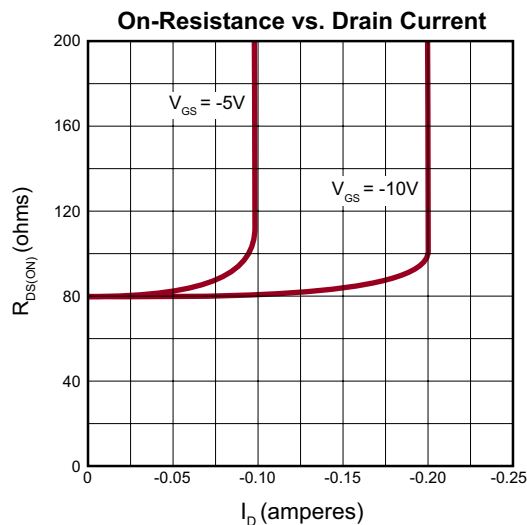
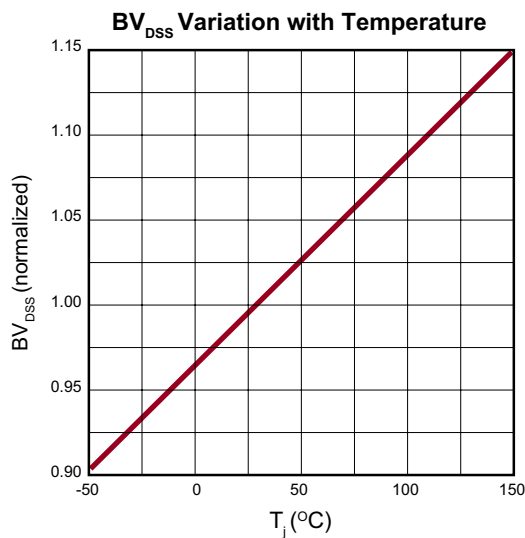
### Switching Waveforms and Test Circuit



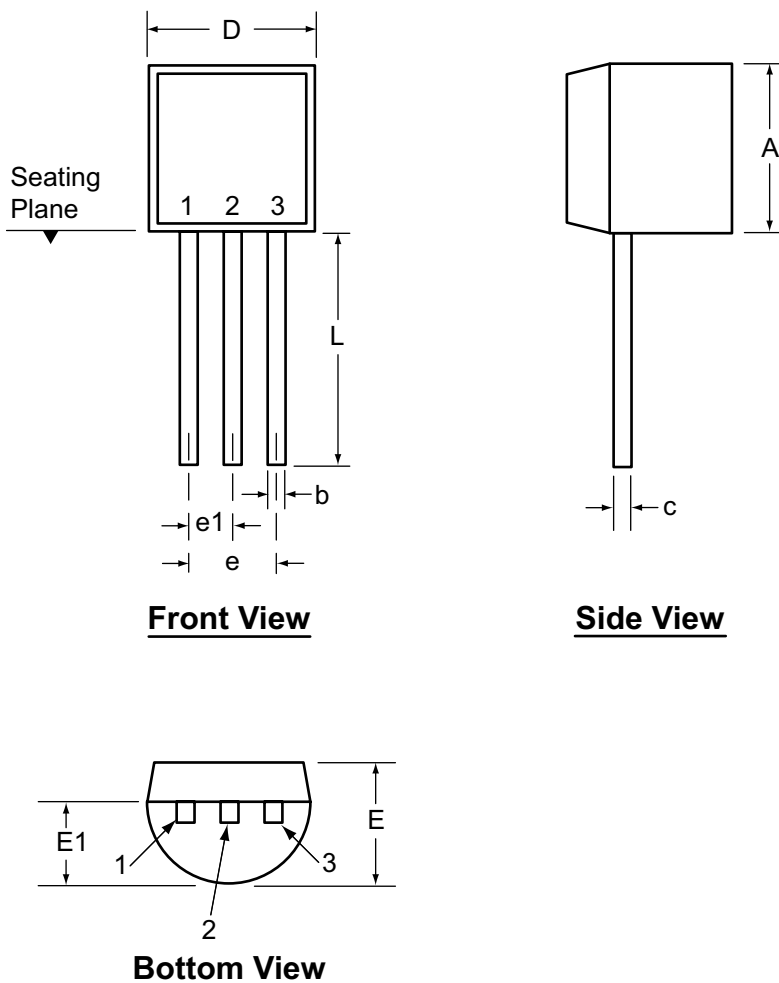
## Typical Performance Curves



Typical Performance Curves (cont.)



### 3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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