Temperature Sensing MOSFET, N-Channel 40-V (D-S)

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
40	0.009 at V_{GS} = 10 V	60[a]
	0.012 at V_{GS} = 4.5 V	60

Notes:
a. Package Limited.

DESCRIPTION

The SUM60N04-12LT is a 40 V N-Channel, 15 mΩ logic level MOSFET in a 5-lead D^2PAK package built on the Vishay Siliconix proprietary high-cell density TrenchFET technology.

Two anti-parallel electrically isolated poly-silicon diodes are used to sense the temperature changes in the MOSFET.

The gate of the MOSFET is protected from high voltage transients by two back-to-back poly-silicon zener diodes.

FEATURES

- Temperature-Sense Diodes for Thermal Shutdown
- TrenchFET® Power MOSFET
- 175 °C Maximum Junction Temperature
- ESD Protected: 2000 V
- Logic-Level Low On-Resistance
- Avalanche Rated
- Low Gate Charge
- Fast Turn-On Time
- 100 % R_g Tested
- 5 Lead D^2PAK

Pb Available

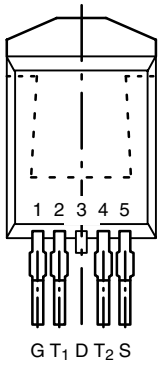
RoHS* COMPLIANT

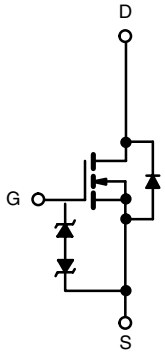
APPLICATIONS

- Industrial

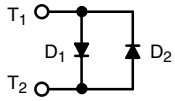
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

D^2Pak
TO-263, 5 Leads





N-Channel MOSFET



Ordering Information: SUM60N04-12LT
SUM60N04-12LT-E3 (Lead (Pb)-free)

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	
V_{GS} Clamp Current		I_G	50	mA
Continuous Drain Current (T_J = 175 °C)	T_C = 25 °C	I_D	60[a]	A
	T_C = 100 °C		50	
Avalanche Current		I_{AR}	50	
Repetitive Avalanche Energy	L = 0.1 mH	E_{AR}	125	mJ
Source-to-Anode Voltage		V_{SA}	100	V
Source-to-Cathode Voltage		V_{SC}	100	
Maximum Power Dissipation[a]	T_C = 25 °C	P_D	110	W
	T_A = 25 °C[d]		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	**Symbol**	**Limit**	**Unit**
Junction-to-Ambient[d]	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	1.35	

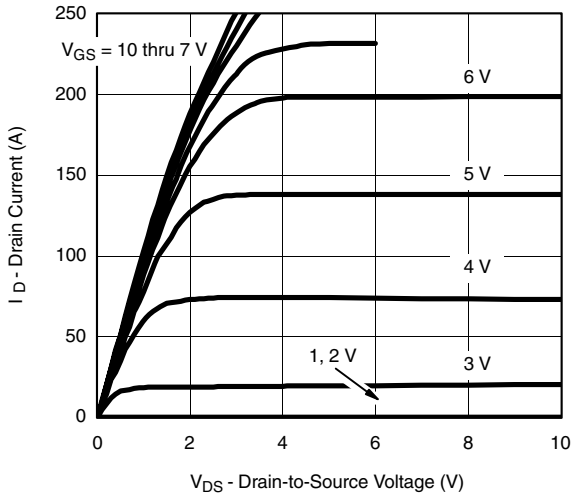
Notes:
a. Package limited.
b. Duty Cycle ≤ 1 %.
c. See SOA curve for voltage derating.
d. When Mounted on 1" square PCB FR4.

MOSFET SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	40			V
V_{GS} Clamp Voltage	V_{GS}	V_{DS} = 0 V, I_G = 20 µA	10		20	
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_{DS} = 1 mA	1		2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 5 V			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 175 °C			250	
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0075	0.009	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 °C			0.0135	
		V_{GS} = 10 V, I_D = 20 A, T_J = 175 °C			0.018	
		V_{GS} = 4.5 V, I_D = 20 A		0.0095	0.012	
Sense Diode Forward Voltage	V_{FD1}	I_F = 250 µA	675		735	mV
	V_{FD2}	I_F = 250 µA	675		735	
Sense Diode Forward Voltage Increase	ΔV_F	From I_F = 125 µA to I_F = 250 µA	25		50	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 20 A		35		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1920		pF
Output Capacitance	C_{oss}			560		
Reverse Transfer Capacitance	C_{rss}			210		
Total Gate Charge[c]	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 25 A		51	70	nC
Gate-Source Charge[c]	Q_{gs}			5.5		
Gate-Drain Charge[c]	Q_{gd}			12		
Gate Resistance	R_g		1.2		4.1	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 20 V, R_L = 0.8 Ω $I_D \cong$ 25 A, V_{GEN} = 10 V, R_g = 2.5 Ω		20	40	ns
Rise Time[c]	t_r			70	120	
Turn-Off Delay Time[c]	$t_{d(off)}$			35	70	
Fall Time[c]	t_f			20	40	
Source-Drain Diode Ratings and Characteristics T_C = 25 °C[b]						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[a]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			1.4	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, di/dt = 100 A/µs		40	60	ns

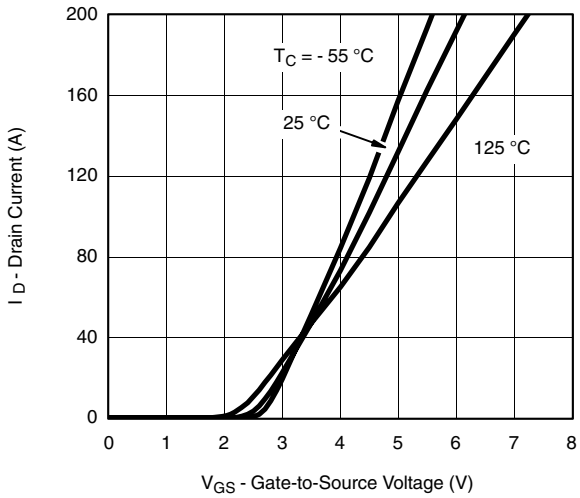
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

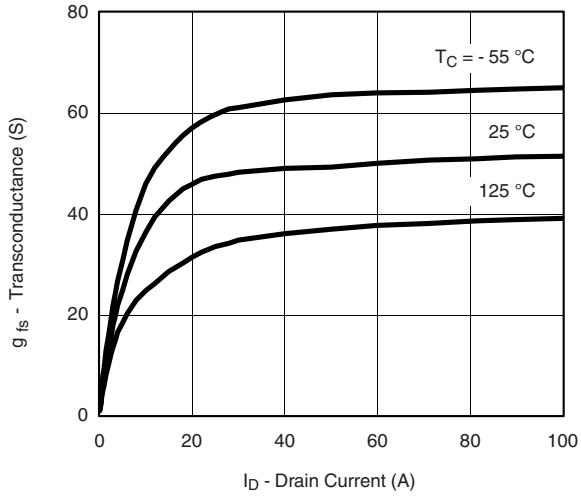
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



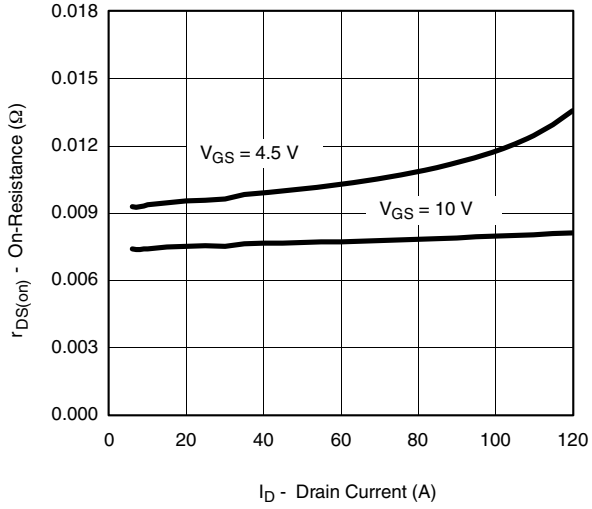
Output Characteristics



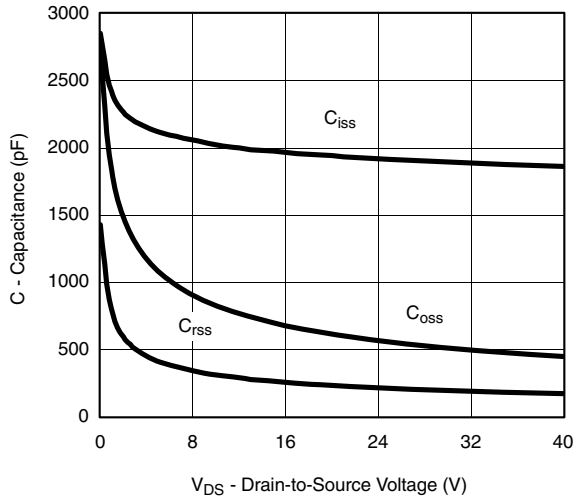
Transfer Characteristics



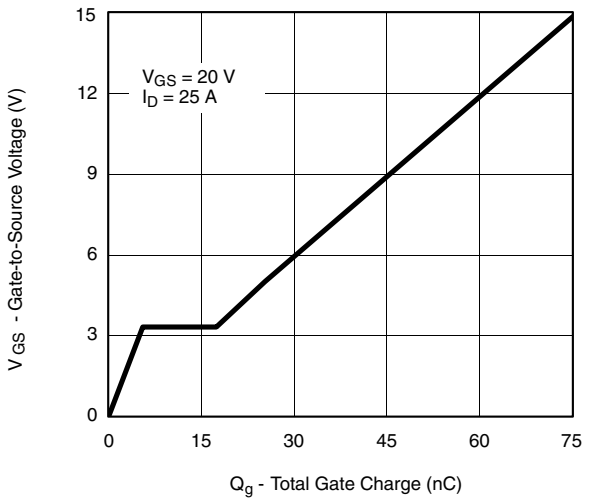
Transconductance



On-Resistance vs. Drain Current

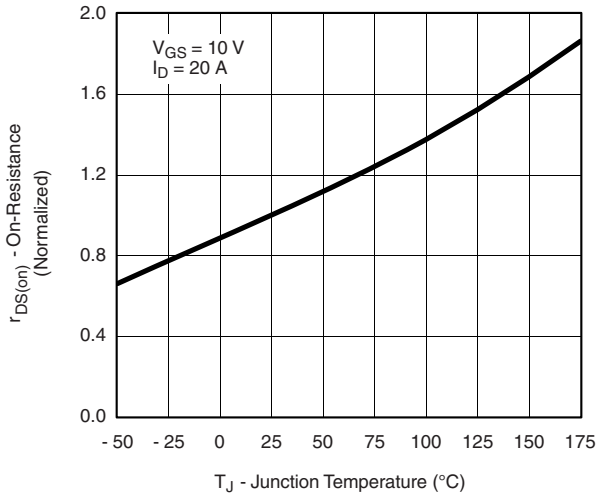


Capacitance

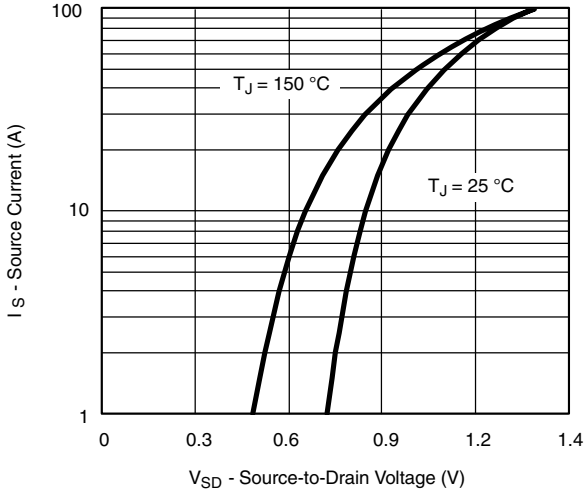


Gate Charge

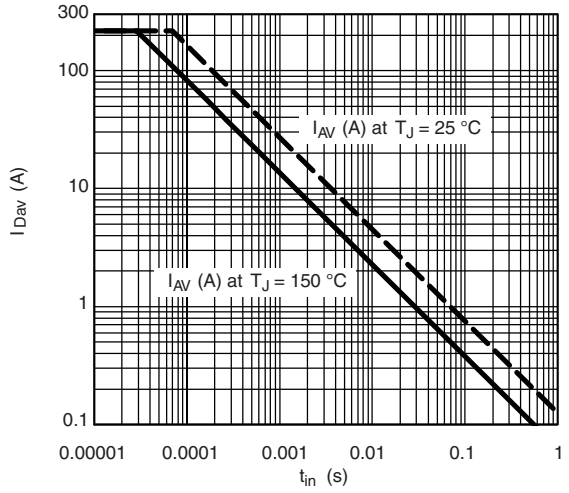
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



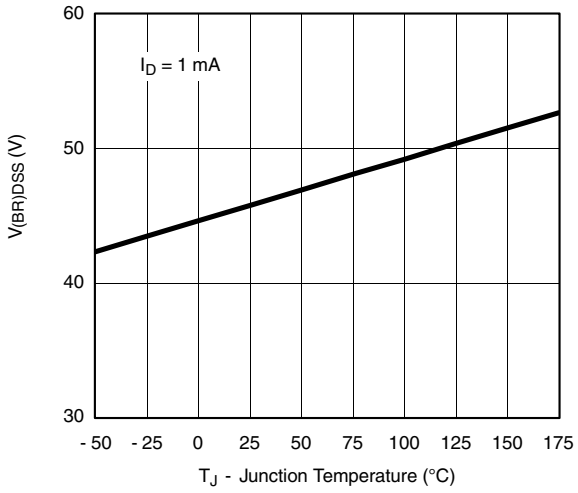
On-Resistance vs. Junction Temperature



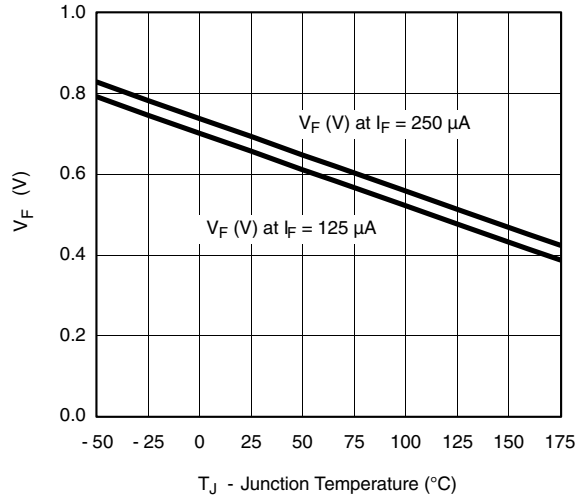
Source-Drain Diode Forward Voltage



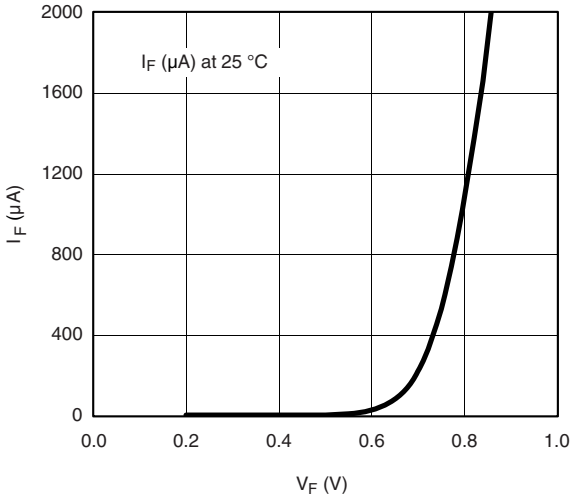
Avalanche Current vs. Time



Drain-Source Breakdown vs. Junction Temperature

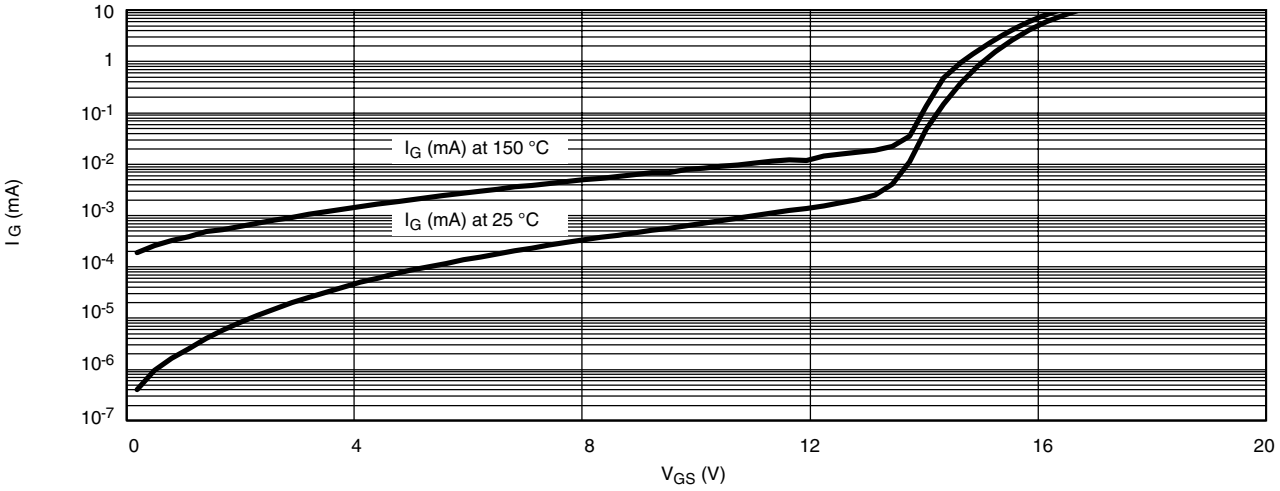


Sense Diode Forward Voltage vs. Temperature



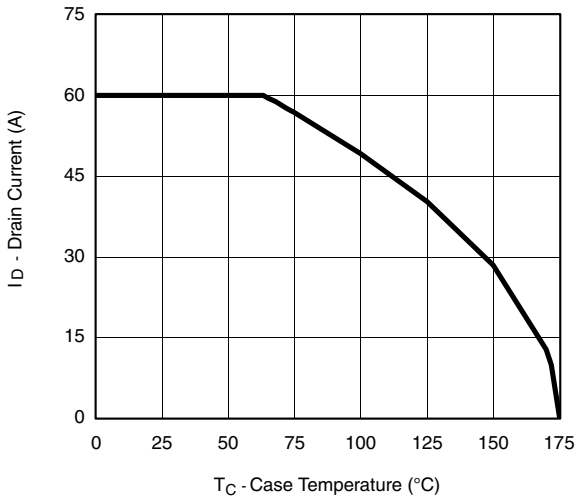
Sense Diode Forward Voltage

TYPICAL CHARACTERISTICS OF G-S CLAMPING DIODES 25 °C, unless otherwise noted

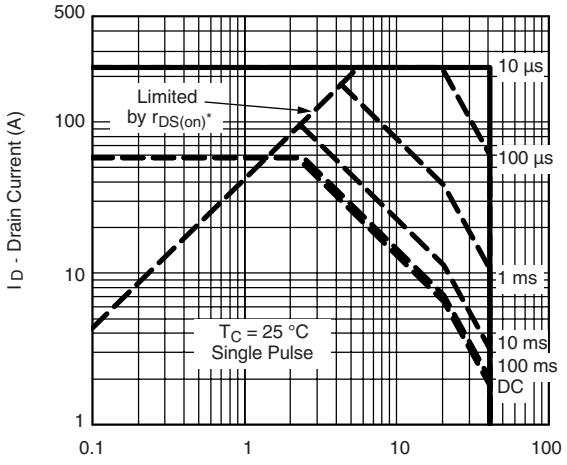


Gate-Source Voltage vs. Gate Current

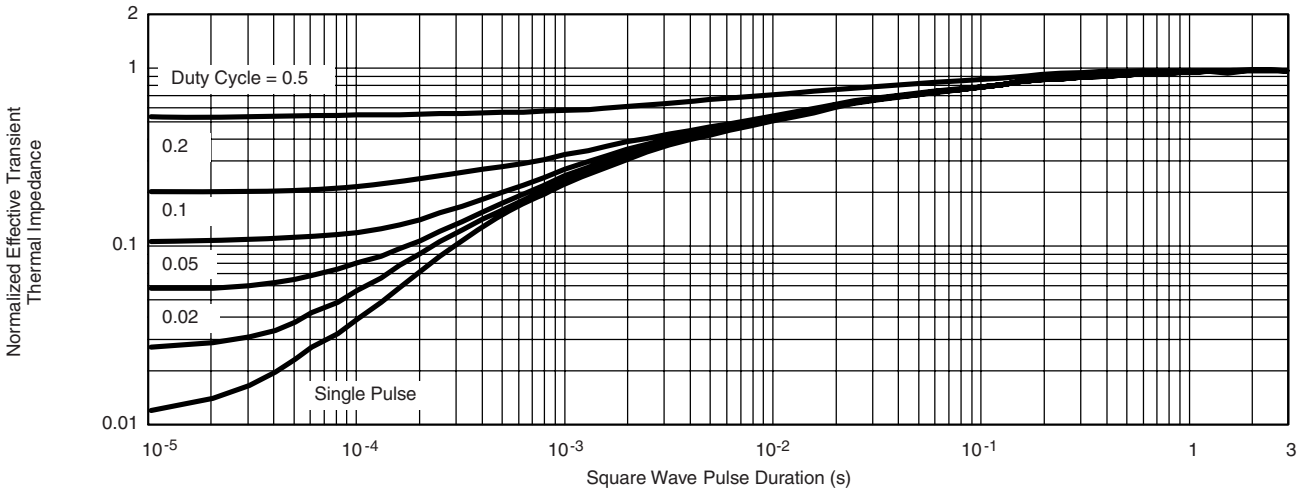
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

APPLICATIONS

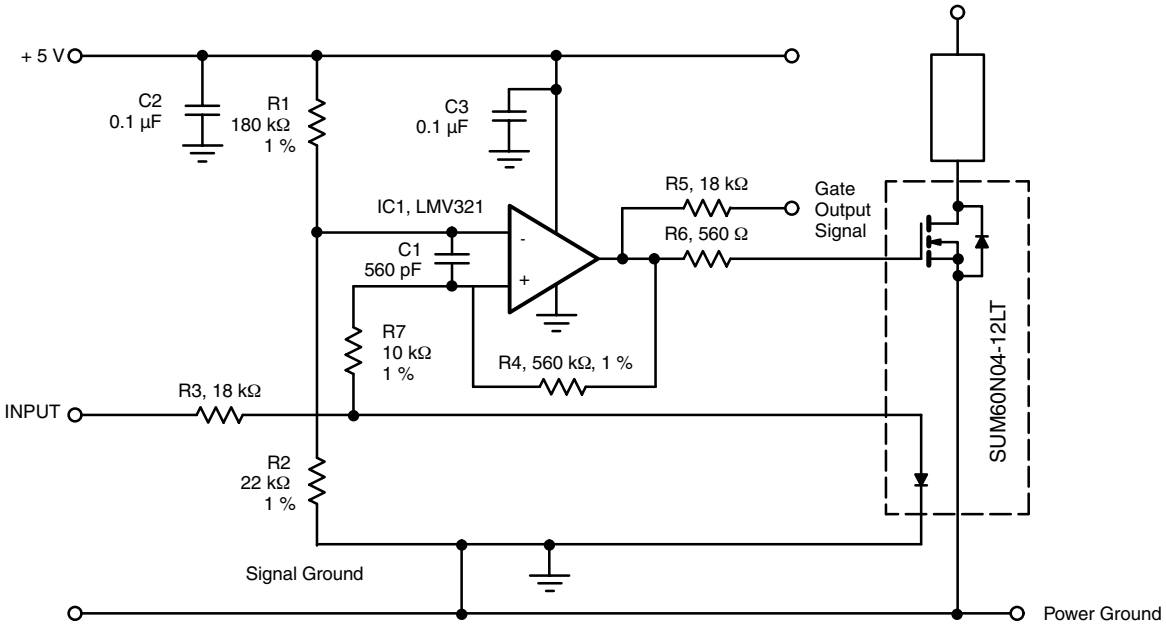


Figure 1.

The SUM60N04-12LT provides a non-committed diode to allow temperature sensing of the actual MOSFET chip. The addition of one simple comparator and a few other components is all that is required to implement a temperature protected MOSFET. Since it has a very tight tolerance on forward voltage, the forward voltage of the diode can be used to provide to shutdown signal. The diode forward voltage falls to around 0.4 V with a bias current of 250 µA when the MOSFET chip is close to the maximum permitted temperature value. The external comparator used to detect over temperature can also be used as a driver stage for the MOSFET, meaning that the on/off input is logic compatible, and can be driven from a logic gate.

A typical circuit is shown in Figure 1. Here a LMV321 operational amplifier is used to drive the MOSFET, and as a comparator to when the maximum junction temperature is reached. The circuit will turn on once more when the chip has cooled to approximately 110 °C, and can cycle on and off until the fault is cleared or the power is removed. This circuit has assumed a 5 V rail is available, but the circuit could easily be adapted for a 12 V rail, for example.

The LMV321 op amp was selected to give reasonable output current to drive the MOSFET at a reasonable price. The SC-70 package means that the protection circuit uses very little board space. However the limited output current means that it can only be used in slow switching applications, where one microsecond switching time and limited dv/dt immunity can be accepted. For PWM and other faster applications, a buffer should be added to drive the MOSFET, or the schematic in Figure 2 used to give fast switching speed.

The reference voltage for the trip point is derived from the 5 V rail, which should have reasonable voltage accuracy and stability (± 0.5 V). A voltage reference could be added if required, but the circuit is only intended to make the MOSFET invulnerable to drastic faults that might otherwise cause it to fail, not to give a precise shutdown point. 1 % resistors are used to provide a reference voltage of 0.545 V, giving a nominal rising trip point of around 155 °C, allowing for the hysteresis drop over R7.

A 560 pF capacitor across the inputs of the comparator provides some noise immunity and gives a response time of around a micro second, just faster than the switching speed of the MOSFET in this circuit (faster response has diminishing returns as the turn-off time is fixed). This does have a side effect of introducing such a delay at turn-on. If this is an issue (although if this delay is an issue, the switching time should be reviewed also), a separate driver could be added using a comparator for over temperature detection only as shown in Figure 2. The diode is then left biased whenever the power is applied to the load and there is no turn-on delay. In a very noisy environment C1 should be increased and additional capacitors may also be required from each input of the comparator to ground and on the logic input.

The bias current of 250 µA nominal is derived from the input signal. In this manner, a simple comparator can be used as a driver for normal on/off operation and a fault detector circuit. The circuit used to provide the input signal must therefore be able to source 0.25 mA with no significant voltage drop.

The LMV321 can provide a output current of 60 mA typical, which provides reasonable switching time for non-PWM applications. A 560 Ω resistor is added in series to protect the op amp and to prevent instability, but will result in switching times of several micro seconds. A lower value may be possible depending on layout, but may violate conditions recommended by the op amp manufacturer.

Hysteresis is added by means of a resistor network around the comparator. Approximately 40 °C hysteresis is added using the components shown. This hysteresis could be reduced if necessary by increasing the value of R4. Another means of implementing hysteresis is to use the output of the comparator to provide some of the bias current for the sensing diode. When the comparator output is low (tripped/off), the bias current is reduced by, say, 150 µA, causing the forward voltage to drop by around 50 mV. This concept would also allow a lower sourcing capability in the logic circuit providing the on/off signal and therefore should be used if input current requirements become a problem.

With the input high, bias current flows and as long as the forward voltage of the diode is higher than 0.465 V, the comparator output is high and the MOSFET is on. If the forward voltage of the diode drops below 0.465 V, the comparator output goes low and the MOSFET is turned off. The gate drive voltage can also be used as an output signal (if required) for logic to interpret and to signify that there is a fault. Note the cathode of the sensing diode should NOT be connected directly to the source of the MOSFET as the noise introduced by high currents in the source loop could affect operation of the sensing circuit. A separate signal ground should be used and connect to power ground at one point only.

A variation on this schematic is shown in Figure 2. Here a low cost comparator (again in a SOT-23 or SC-70) is used to provide a fault output signal only. The diode bias current is taken from the 5 V. In this manner the diode bias is applied at all times, so the noise filtering capacitor, C1 will not introduce a turn-on delay. The fault output signal could be used to enable the gate driver as shown, or fed to larger monitoring circuit to shutdown the MOSFET.

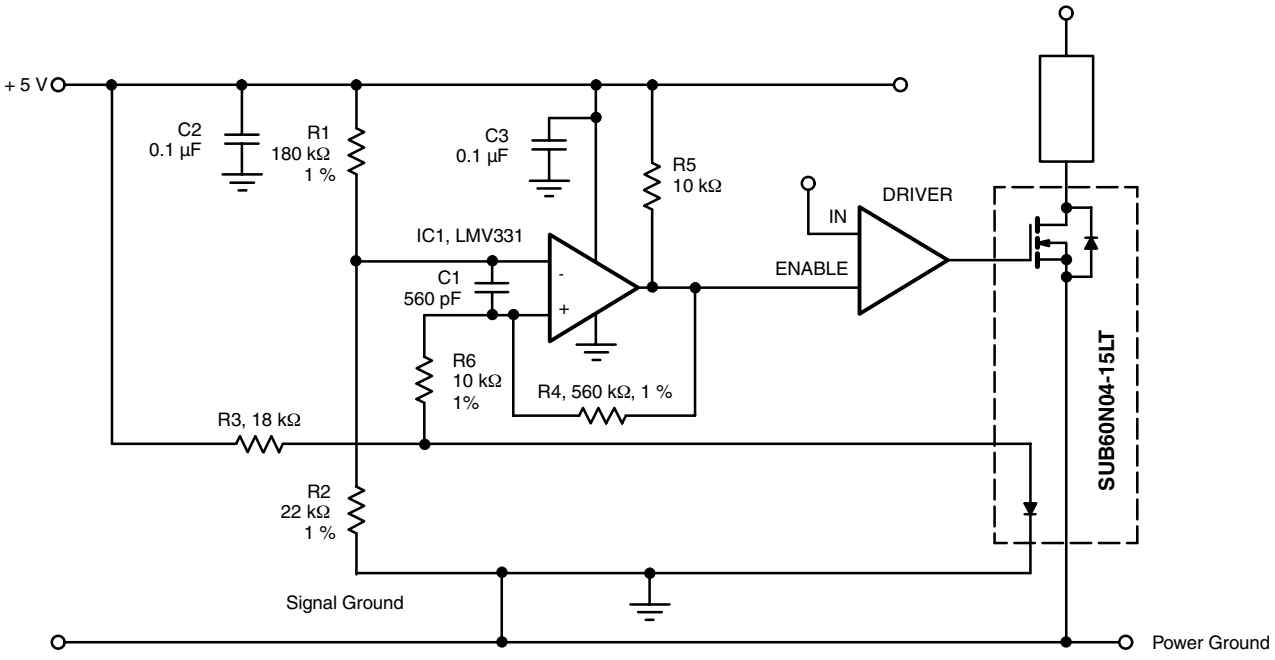
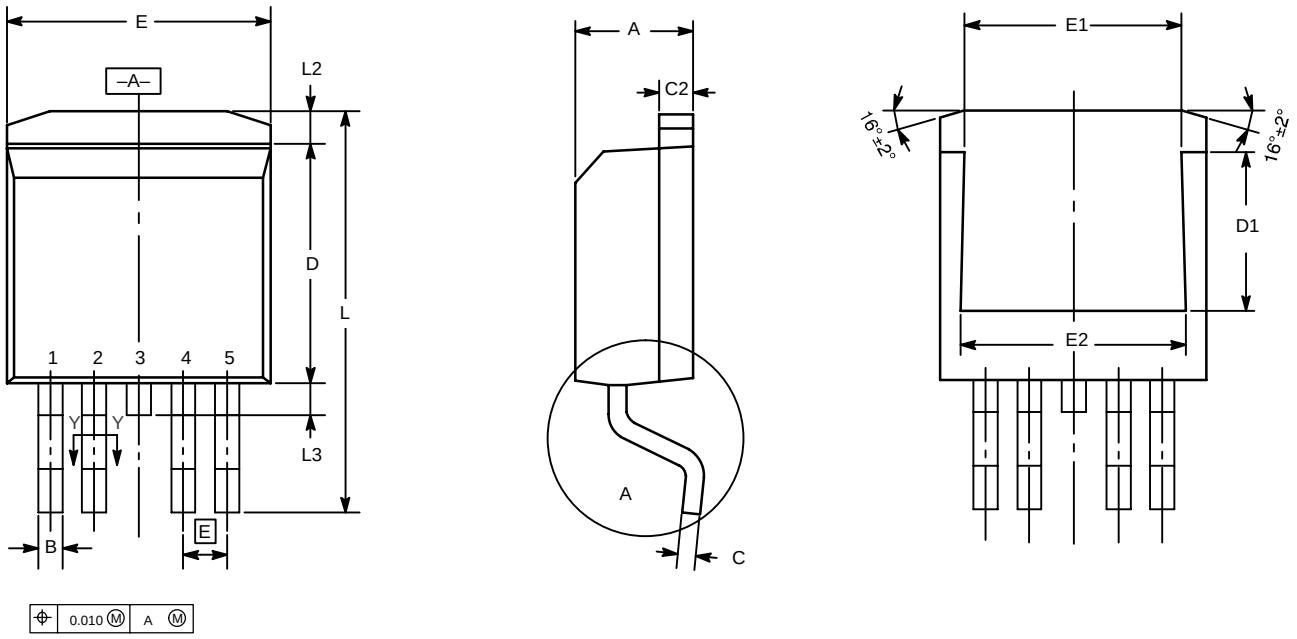


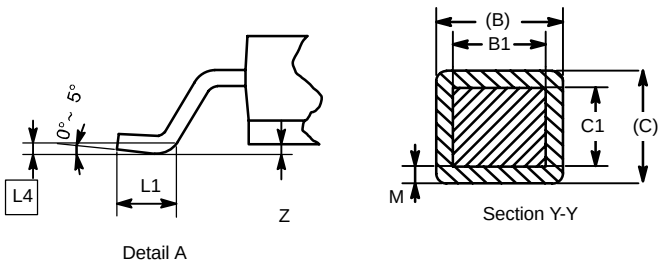
Figure 2.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?71620.

TO-263 (D^2PAK): 5 LEADS

(For Lead Thickness 25 mil)





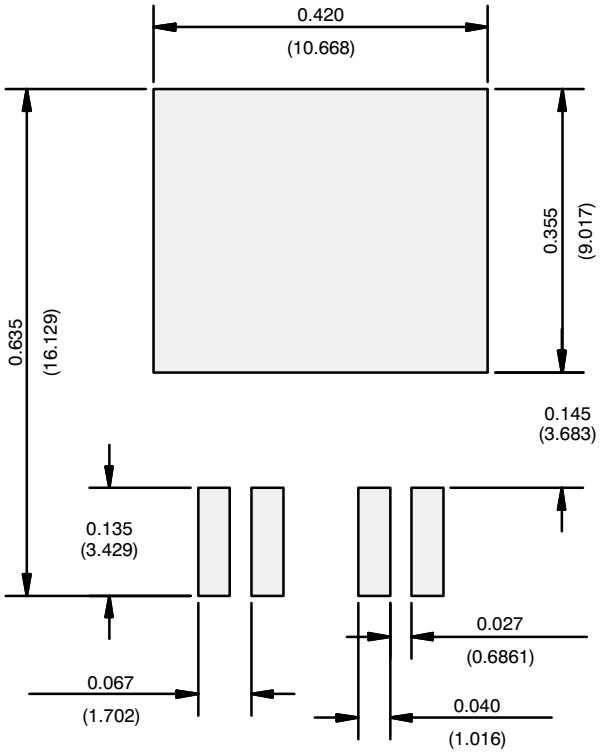
Dim	INCHES	
	Min	Max
A	0.170	0.185
B	0.028	0.039
B1	0.028	0.035
C	0.018	0.028
C1	0.018	0.025
C2	0.045	0.055
D	0.340	0.380
D1	0.220	0.255
E	0.385	0.405
E1	0.310	0.340
E2	0.355	0.375
[E]	0.067 BSC	
L	0.575	0.625
L1	0.090	0.110
L2	0.040	0.055
L3	0.050	0.070
[L4]	0.010 BSC	
M	–	0.002

ECN: T-01063—Rev. B, 07-May-01
DWG: 5864

NOTES:

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25% of L1 can fall above seating plane by maximum 8 mils.
3. Pin-to-pin coplanarity maximum 4 mils.
4. Z not to exceed 10 mils.

RECOMMENDED MINIMUM PADS FOR D²PAK: 5-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.