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Designer's Guide to the ISL55210-ABEVAL1Z Active Balun Evaluation Board

Using the Active Balun Board to Test Design Options

This relatively simple board is intended to provide a quick means to test the performance of the active balun configuration using the ISL55210. While all wideband, voltage feedback (VFA), fully differential amplifiers (FDA) can perform a single ended input to differential output operation, the frequency span for acceptable input match (or low return loss) is greatly enhanced by the >1.5GHz common mode loop bandwidth internal to the ISL55210. The input and gain setting elements for this board are very simple, while the output side includes 3 possible output interfaces. As delivered, the differential output is converted to single ended through a very wideband transmission line transformer. This allows easy response shape measurements with minimal transformer rolloff effects. The two other output options include a 200Ω load differential to single ended path for OIP3 measurements with lighter loads and a differential 50Ω output path for direct measurement of just the ISL55210 response using a 4 port network analyzer.

While the board itself is completely flexible for input impedance setting and gain by changing only 4 resistor elements, the default circuit for the board as delivered implements a 50Ω input match with a 16.4dB gain to the FDA output pins. The simulation circuit for this configuration is shown in Figure 1.

The operation of this circuit is well modeled using the spice model for the ISL55210 within the free iSim PE simulator[1]. The board input is C2 while the output is the balun output pin. Only +3.3V supply is required where the ISL55210 delivers exceptional performance using only ≈34mA supply current. The resistors here have been snapped to 1% standard values. To get a desired input impedance matched to R_S, and gain (Av) from the input of R_{g1} to the differential outputs, the exact element values are given by these two simple equations (Equations 1 and 2)[2].

The two feedback resistors should be equal and set to:

$$R_f = \frac{Av(Av+4)R_S}{2(Av+2)} \quad \text{(EQ. 1)}$$

Then R_{g1} will be set to:

$$R_{g1} = \frac{R_S}{1+\frac{A_V}{2}} \quad \text{(EQ. 2)}$$

And R_{g2} will be set to the sum of R_{g1} and the R_S element to get balance in the differential feedback loop. The blocking caps are set as necessary to pass the lowest frequency of interest. Using this simple blocking cap approach places all the DC operating voltages on the two input and output pins at the default internal Vcm voltage = 1.2V for the ISL55210. This circuit can implement a DC-coupled signal path if the supplies are set to +2.5V and -1.2V to keep the I/O headroom requirements satisfied but that is not supported by this board

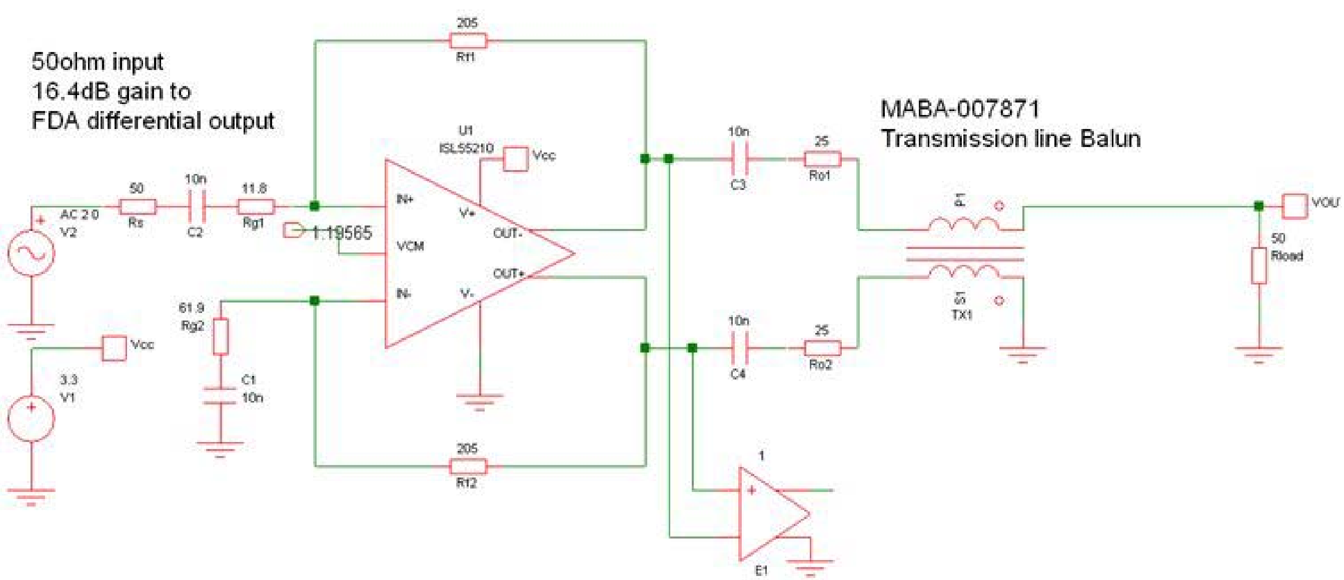

FIGURE 1. iSim PE SIMULATION CIRCUIT FOR THE DEFAULT CONFIGURATION OF THE ACTIVE BALUN EVM

where only AC-coupled designs can be tested. Running a set of parametric frequency response curves vs Av to the FDA output pins in ADS, with the input impedances targeted to match an R_S = 50Ω, gives the expected parametric response curves of Figure 2 where the blocking capacitors have been set to 10µF in simulation to eliminate their effect.

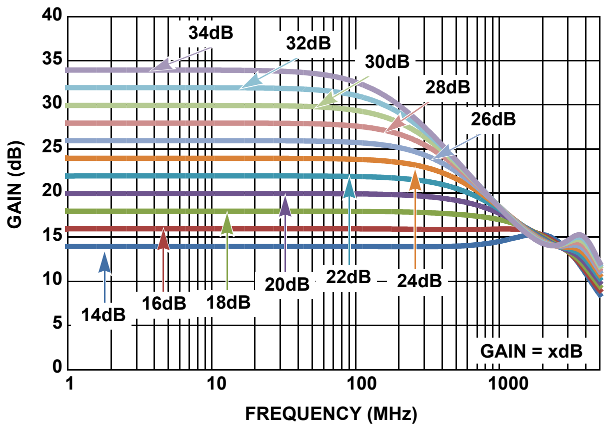

FIGURE 2. RESPONSE CURVES vs AV FOR THE ACTIVE BALUN WITH 50Ω INPUT

TABLE 1.

GAIN V/V	GAIN (dB)	Rf	Rg1	Rg2	SIMULATED BW (MHz)
5.00	14	160.71	14.29	64.29	3900
6.29	16	195.31	12.06	62.06	3155
7.92	18	238.04	10.08	60.08	2037
9.98	20	291.06	8.35	58.35	1200
12.56	22	357.12	6.87	56.87	811
15.81	24	439.67	5.61	55.61	588
19.91	26	543.07	4.57	54.57	445
25.06	28	672.79	3.70	53.70	330
31.55	30	835.72	2.98	52.98	260
39.72	32	1040.51	2.40	52.40	205
50.00	34	1298.08	1.92	51.92	158

This sweep is stepping the gain up in 2dB steps showing the required resistor values and the expected F-3dB bandwidths. Since the ISL55210 is a 4GHz gain bandwidth VFA based FDA, the response bandwidth decreases with gain. The significant benefit of using the common mode feedback loop to set the input match is the vastly reduced resistor values. The action of the common mode loop develops the input impedance largely through feedback requiring very low input resistors to achieve the match. This gives input noise figures <7dB for gains > 18dB using the low noise ISL55210 in this circuit. The closed loop bandwidths are also extended over typical approaches with a resistor to ground since the noise gain will be 1 + Av/2.The bandwidths at lower gains do not strictly follow a gain bandwidth product type response showing significant bandwidth extension at lower gains due to reduced phase margin effects.

The 16.4dB gain used as the setting for the active balun evaluation board simulates very flat through 1GHz with approximately 4GHz F-3dB bandwidth for the response to the ISL55210 outputs. In fact the board shows a response shape set by the blocking capacitors on the low end and the output transformer on the high end. All of these elements are well modeled and running a response simulation of Figure 1 gives the expected shape of Figure 3 where the 6dB matching loss at the output is modeled but the insertion loss of the output transformer is not. That insertion loss is specified as 0.4dB (hence the 16.4dB gain setting) but measures only 0.2dB. The measured response on the board will have a nominal midband gain of 10.2dB with a response shape very close to this simulation. The simulation is predicting -0.5dB response flatness from approximately 2MHz to 500MHz.

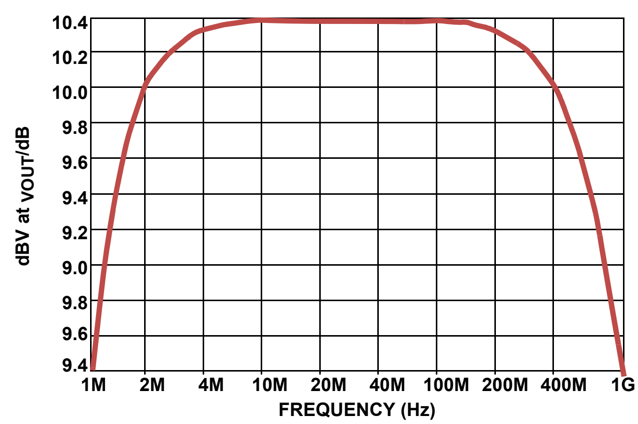

FIGURE 3. FOR THE CIRCUIT ON THE ACTIVE BALUN BOARD OF FIGURE 1

Full Evaluation Board Schematic

The schematic with power supply decoupling and the optional output interfaces is shown in Figure 4.

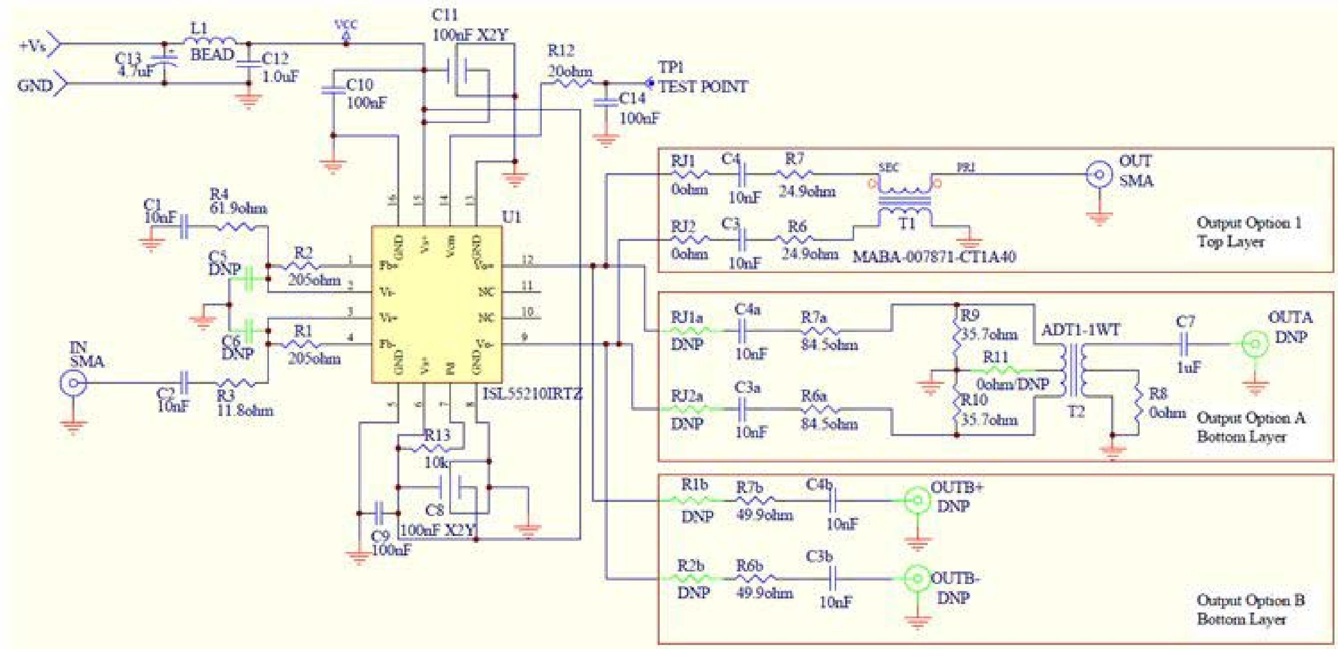

FIGURE 4. FULL BOARD SCHEMATIC

The supply decoupling and Vcm decoupling is the same used as for the standard ISL55210 evaluation board except R12 is reduced from 200Ω to 20Ω to reduce noise into the Vcm reference path. The optional elements (green) not populated in the board as delivered include:

1. Two capacitors on the inverting summing junctions (C5 and C6). These can be used to peak the response at higher gains to hold flatness to higher frequencies but will be peaking the output noise.
2. The 2 lower output networks are not fully populated. The ADT1-1WT path is intended for distortion measurements where the values shown would be a 200Ω load at the FDA outputs but 50Ω source to the spectrum analyzer. This is intended to emulate the lighter load of a typical ADC interface circuit. To use this path, the output SMA needs to be removed and reversed to pick up this output path on the lower side of the board. The lowest optional output interface would be used to measure the response to the FDA output pins when a 4 port network analyzer is available.
3. To select either of these alternate output paths, populate the connecting resistors for only one path at a time.

All of the signal path capacitors are set to pass the lowest intended frequencies and were set to 10nF values in the board as delivered. Figure 5 shows the populated board as delivered.

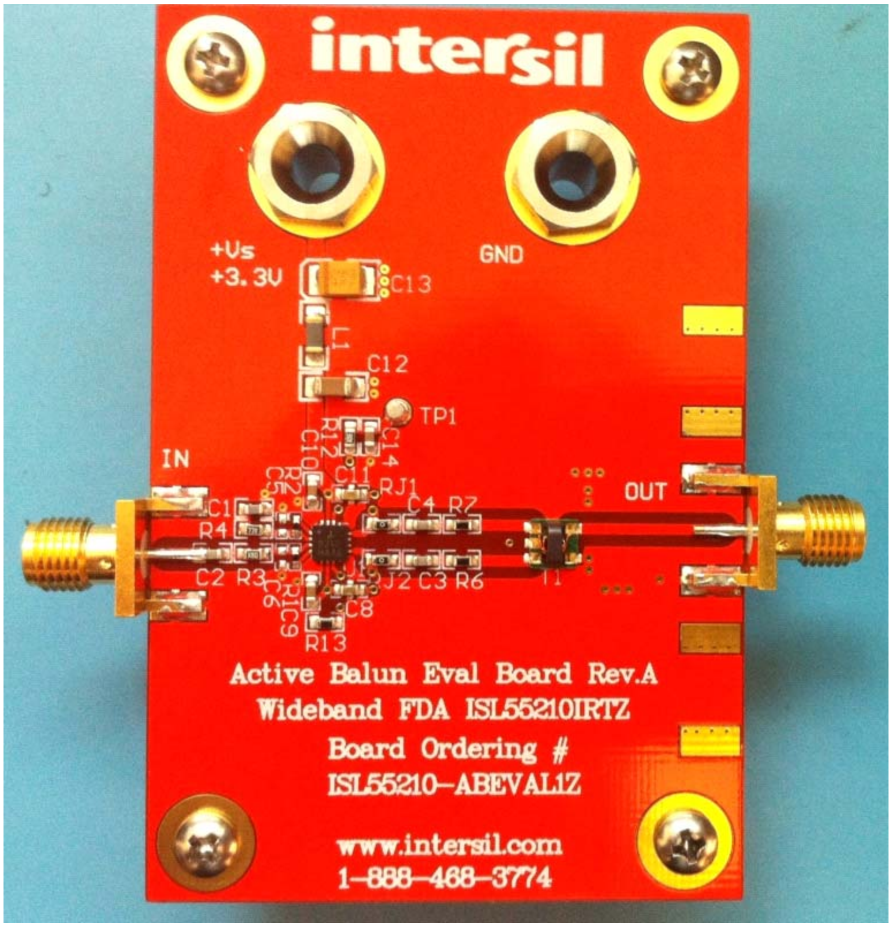

FIGURE 5. POPULATED BOARD AS DELIVERED FROM INTERSIL

Measured Performance On The Active Balun Board

Taking the default configuration of Figure 1 implemented as the top output interface of Figure 4 and measuring the S21 response from 1MHz to 2GHz gives the exceptionally flat response of Figure 6. Two different sets of blocking caps where used here where the increase from 1nF to 10nF moved the high pass corner down with no adverse self resonance at higher frequencies. Even with the 10nF caps, part of the high pass corner is being set by the MABA- 007871 where the true low end corner to the FDA outputs is shown in the green curve. The high frequency rolloff follows the simulation of Figure 3 up through about 600MHz then a slight peaking in the ISL55210 response is pulling it back up. This is showing a 10.2dB midband gain to a matched load (the two series output resistors set the output impedance since the ISL55210 is a broadband low impedance output itself) with ≤1dB gain rolloff from 3MHz to 1GHz. Figure 6 also shows the response to the differential output using a 4 port network analyzer and two 50Ω series output element of the lowest output interface option in Figure 4. This gives more insertion loss but does show the ISL55210 by itself is peaking to the output above 900MHz at this lower gain, so the rolloff with the transformer output is actually the transformer itself.

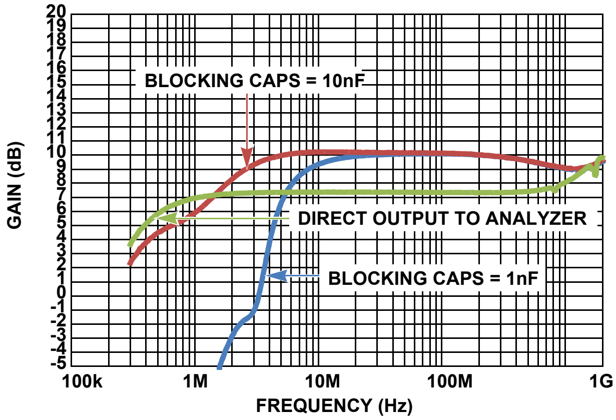

FIGURE 6. MEASURED RESPONSE SHAPES

The two upper curves of Figure 6 through the transmission line transformer are emulating the available response at this gain with some added rolloff due to the transformer. These are giving a 50Ω single ended input to differential output stage that is delivering the equivalent of a 1:3.3 turns ratio step up in gain with a flatness span far exceeding any balun of that turns ratio (1:11Ω ratio).

For this design point, only an 11.8Ω physical input resistor was required to show a nominal 50Ω input match to the source. Measuring that input impedance from 1MHz to 500MHz using an HP4195 analyzer set up for impedance measurement gives the screen picture of Figure 7.

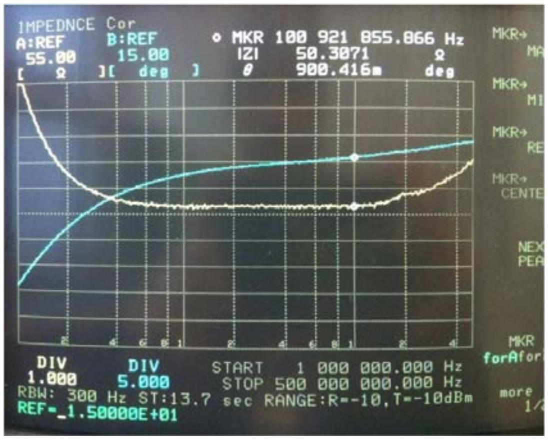

FIGURE 7. MEASURED INPUT IMPEDANCE FOR THE CIRCUIT OF FIGURE 1

This is showing <±2Ω deviation from 2MHz to 500MHz (≤28dB return loss) with nearly exact match over a broad range from 3MHz to 300MHz. The markers at 100MHz are showing an input magnitude of 50.3Ω with 0.9° phase. This voltage feedback based FDA is doing a remarkable job of transforming that 11.8Ω R3 element in Figure 4 into a 50Ω match using its very wideband common mode feedback loop.

The Noise Figure (NF) in this relatively low gain setting calculates to approximately 7dB. This low NF is depending on the low 0.85nV/√Hz differential input spot noise for the ISL55210 and the reduced resistor values enabled by this active input match capability. Going to higher gain settings will reduce the input NF where for gains >22dB it drops below 6dB; a remarkable number for a 115mW amplifier. These numbers are from an analysis using only the differential path noise numbers. Since this topology will also have a common mode noise component, the measured NF will be slightly higher due to component mismatches converting a small portion of the common mode noise to differential. Measuring the spot output noise for the default configuration of the active balun board with a 50Ω termination on the input and referring that measurement to the FDA differential output pins gives the plot of Figure 8.

This low output spot noise can be input referred by the 6.6V/V gain setting and converted to a Noise Figure, as shown in Figure 9. The Vcm control input has an internal 30MHz filter that might explain the decrease in noise going up through 40MHz. That bandlimiting is only on the buffer stage to the internal reference for the Vcm loop. The internal loop bandwidth is the much higher >1.5GHz required for this circuit to operate successfully. The midrange 7.9dB noise figure exceeds the expected 7dB noise figure probably due to common mode to differential conversion and more precise matching in the external resistors might move this closer to theoretical. No effort here was made for extremely precise matching and simple 1% resistors were loaded.

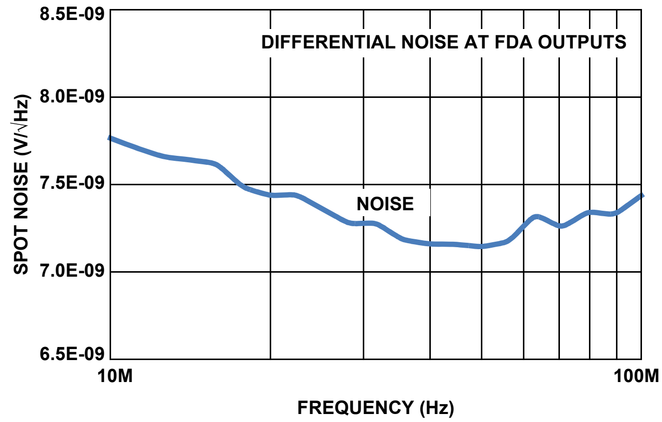

FIGURE 8. MEASURED OUTPUT NOISE FOR THE CIRCUIT OF FIGURE 4

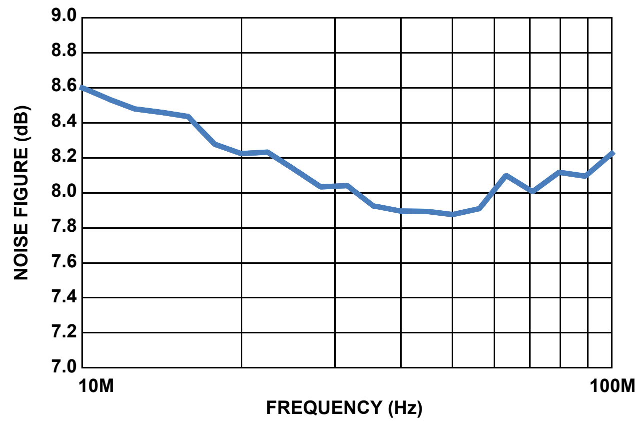

FIGURE 9. MEASURED SPOT NOISE CONVERTED TO A NOISE FIGURE

The output 3rd order intercept for the circuit of Figure 1 may also be measured. The typical definition for the OIP3 is from a matched source to a matched load. With the 6dB loss inserted by the matching elements that drops the reported OIP3 from the FDA output pins to the matched load by 6dBm. Using two 25Ω series outputs to a 50Ω load shows a total 100Ω differential load across the FDA output pins. Emulating that with the ADT1-1WT output option of Figure 4 by putting another 200Ω load directly across the FDA output pins (the ADT1-1WT path is set up to look like a 200Ω load) gives the higher frequency OIP3 measurements of Figure 10 with the straight line a superimposed line fit [3]. Again, this is a worst case for an application of this net gain of 10.4dB circuit as if it were driving through 2 - 25Ω series output to a single differential 50Ω load of some following element. Driving into an ADC or interstage filter to an ADC, taking less insertion loss, and/or a lighter load will give higher OIP3 than shown in Figure 10.

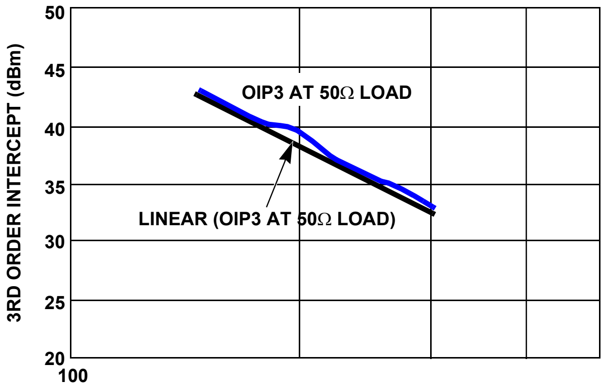

FIGURE 10. MEASURED AND LINE FIT OIP3 FOR THE CIRCUIT OF FIGURE 1 DRIVING A DOUBLY TERMINATED 50Ω LOAD

The ISL55210 does show true intercept performance on the 3rd order terms and Figure 10 is showing the expected rolloff in the intercept for this low power device as the loop gain rolls off. Going to higher gains will move this curve down while going to lighter loads will move it up. Offering >39dBm OIP3 through 200MHz is exceptional for a 115mW device. Below 100MHz the 3rd order intermodulation tones become very difficult to measure where the intercept is exceeding 50dBm.

Options and Summary

This simple building block can be tested for any target input impedance and gain setting to get its performance prior to combining with other system elements before and after this stage. It does depend on the source impedance being close to the expected value in the desired frequency band. If that source impedance deviates widely out of band, a passive bandpass filter at the output is recommended in the design to limit out of band noise peaking issues [4]. The ISL55210 is, however, internally compensated to remain stable for any source impedance. It does need to avoid direct capacitive loads at the outputs but adding at least 10Ω series output elements is adequate to isolate that effect. While the ISL55210 includes input protection diodes across the input, high overdrives have been found to latch the device into a low loop gain condition. This can be reset using the disable function of the device but if possible avoid high overdrive conditions.

This board can be set literally for any input impedance and gain by changing the R1 'R4 values in Figure 4 using Equations 1 and 2. For example, a set of values for a 75Ω input are shown in Table 1 with estimated F-3dB bandwidths to the FDA output pins.

TABLE 2. RESISTOR VALUES AND SIMULATED F-3DB FOR SWEPT GAIN 75Ω INPUT IMPEDANCE

GAIN V/V	GAIN (dB)	Rf	Rg1	Rg2	SIMULATED BW (MHz)
5.01	14	161.0353	14.26153	64.26153	3900
6.31	16	195.705	12.03431	62.03431	3155
7.94	18	238.525	10.05704	60.05704	2037
10.00	20	291.6667	8.333333	58.33333	1200
12.59	22	357.877	6.85436	56.85436	811
15.85	24	440.6207	5.602576	55.60258	588
19.95	26	544.2603	4.555264	54.55526	445
25.12	28	674.2841	3.68747	53.68747	330
31.62	30	837.5952	2.974174	52.97417	260
39.81	32	1042.876	2.391731	52.39173	205
50.12	34	1301.049	1.918696	51.9187	158

The parametric response curves from iSim PE are shown in Figure 11 for these settings and a 75Ω source into this active balun configuration of the ISL55210. These response curves are from the input of R_{g1} to the differential output pins of the amplifier.

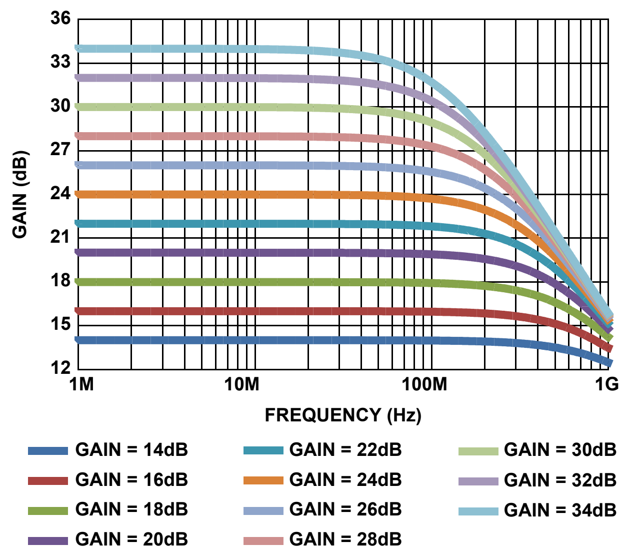

FIGURE 11. PARAMETRIC RESPONSE CURVES FOR 75Ω INPUT DESIGNS

References

[1] These simulations are in the free Intersil Spice and power simulation package available as a download at http://www.intersil.com/content/intersil/en/tools/isim.html

[2] These are presented in a 2 part EDN article where Part 1 is here. http://www.edn.com/design/analog/4410567/Wideband-matched-input-impedance-with-ultra-low-noise-using-the-active-match-capability-of-a-new-type-of-amplifier–part-1-of-2–

[3] This plot actually comes from an article using this active balun stage with a bandwidth extension technique for the ADT1-1WT. http://www.eetimes.com/design/test-and-measurement/4402894/Extending-the-Useable-Frequency-Span-of-1-1-Wideband-Transformers-Used-for-Distortion-Measurements?Ecosystem=analog-design

[4] See this example bandpass filter design example from a 2 part article on very high IM3 ADC interface designs. http://www.eetimes.com/design/analog-design/4375208/Developing-an-Ultra-High-Intercept-Last-Gain-Stage-to-a-14-Bit-High-SFDR-ADC–Part-1-of-2-

Board Details

The false color silkscreen for this board appears in Figure 12.

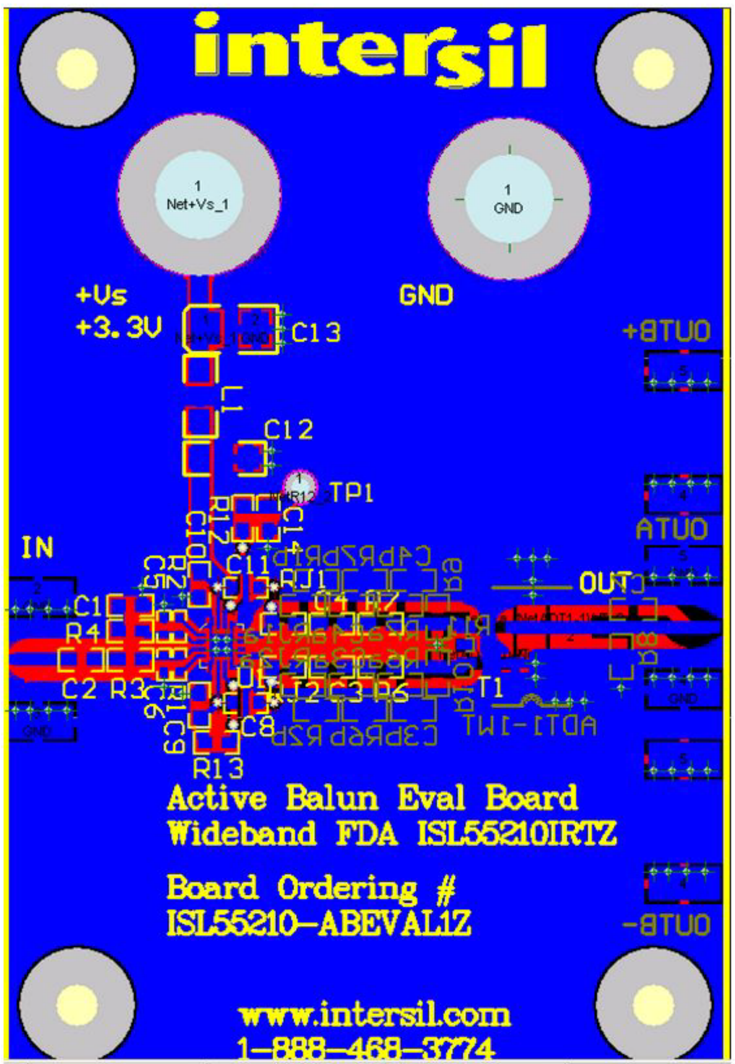

FIGURE 12. SILKSCREEN FOR TOP AND BOTTOM

ISL55210-ABEVAL1Z Bill of Materials

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
ISL55210-ABEVAL1ZREVAPCB	1	ea		PWB-PCB,ISL55210-ABEVAL1Z,REVA,ROHS	IMAGINEERING INC	ISL55210-ABEVAL1ZREVAPCB
100X14W104MV4T-T	2	ea	C8, C11	CAP-X2Y, SMD, 0603, 0.1µF, 10V, 20%, X7R, ROHS	JOHANSON DIELECTRICS INC	100X14W104MV4T
C1608C0G1H103J-T	8	ea	C1, C2, C3, C4, C3a, C4a, C3b, C4b	CAP, SMD, 0603, 0.01µF, 50V, 5%, C0G/NP0, ROHS	TDK	C1608C0G1H103J
H1044-DNP	0	ea	C5, C6	CAP, SMD, 0402, DNP-PLACE HOLDER, ROHS		
H1045-00104-50V10-T	4	ea	C7, C9, C10, C14	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	AVX	06035C104KAT2A
H1065-00105-50V10-T	1	ea	C12	CAP, SMD, 1206, 1µF, 50V, 10%, X7R, ROHS	VENKEL	C1206X7R500-105KNE
H1121-00475-10V10-B-T	1	ea	C13	CAP-TANT, LOW ESR, SMD, B, 4.7µF, 10V, 10%, 3.5Ω, ROHS	KEMET	T491B475K010AT
108-0740-001	2	ea	GND, +Vs	CONN-JACK, BANANA-SS-SDRLESS, VERTICAL, ROHS	JOHNSON COMPONENTS	108-0740-001
142-0701-801	2	ea	IN,OUT	CONN-RF, END LAUNCH SMA JACK, TH, 50Ω, ROUND, ROHS	JOHNSON COMPONENTS	142-0701-851
2110-2-00-80-00-00-07-0	1	ea	TP1	CONN-TURRET, TH, SWAGE MNT, 0.230LENGTH, ROHS	MILL-MAX	2110-2-00-80-00-00-07-0
EXC-ML32A680U-T	1	ea	L1	FERRITE BEAD, SMD, 1206, 68Ω, 3A, 100MHz, ROHS	PANASONIC	EXC-ML32A680U
ISL55210IRTZ	1	ea	U1	IC-DIFFERENTIAL AMP, 16P, TQFN, 3x3, ROHS	INTERSIL	ISL55210IRTZ
H2510-02050-1/16W1-T	2	ea	R1,R2	RES, SMD, 0402, 205Ω, 1/16W, 1%, TF, ROHS	VISHAY/DALE	CRCW0402205RFKED
H2510-DNP	0	ea	R11	RES, SMD, 0402, DNP, DNP, DNP, TF, ROHS		
H2511-00200-1/10W1-T	1	ea	R12	RES, SMD, 0603, 20Ω, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF20R0V
H2511-00R00-1/10W-T	3	ea	R8,RJ1,RJ2	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
H2511-01002-1/10W1-T	1	ea	R13	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	KOA	RK73H1JT1002F
H2511-011R8-1/10W1-T	1	ea	R3	RES, SMD, 0603, 11.8Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-11R8FT(PBFREE)
H2511-024R9-1/10W1-T	2	ea	R6,R7	RES, SMD, 0603, 24.9Ω, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF24R9V
H2511-035R7-1/10W1-T	2	ea	R9, R10	RES, SMD, 0603, 35.7Ω, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF35R7V

ISL55210-ABEVAL1Z Bill of Materials (Continued)

PART NUMBER	QTY	UNITS	REFERENCE DESIGNATOR	DESCRIPTION	MANUFACTURER	MANUFACTURER PART
H2511-049R9-1/10W1-T	2	ea	R6b, R7b	RES, SMD, 0603, 49.9Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-49R9FT
H2511-061R9-1/10W1-T	1	ea	R4	RES, SMD, 0603, 61.9Ω, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-61R9FT
H2511-084R5-1/10W1-T	2	ea	R6a, R7a	RES, SMD, 0603, 84.5Ω, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF84R5V
H2511-DNP	0	ea	R1b, R2b, RJ1a, RJ2a	RES, SMD,0603, DNP-PLACE HOLDER, ROHS		
ADT1-1WT+	1	ea	ADT1-1WT	TRANSFORMER-RF, SMD, 6P, CASE CD542, 0.5W, 30mA, ROHS	MINI-CIRCUITS	ADT1-1WT+
MABA-007871-CT1A40-T	1	ea	T1	TRANSFORMER-BALUN, 1:1 RF, SMD, 6P, 4.21x4.83, 200mA, 200mW, ROHS	M/A-COM TECHNOLOGY	MABA-007871-CT1A40
5X8-STATIC-BAG	1	ea	Place assy in bag	BAG, STATIC, 5x8, ZIPLOC, ROHS	INTERSIL	212403-013
LABEL-DATE CODE	1	ea	AFFIX TO BACK OF PCB	LABEL-DATE CODE_BOM REV#_SERIAL# LABEL ON ZIL & QUEL	INTERSIL	LABEL-DATE CODE