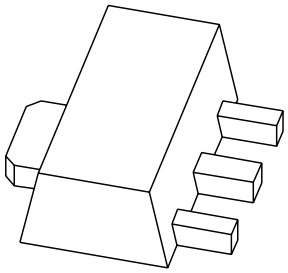
DATA SHEET



BSS192
P-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of 1997 Jun 20

2002 May 22

Philips Semiconductors

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P-channel enhancement mode vertical D-MOS transistor

BSS192

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high-speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT89 package.

PINNING - SOT89

PIN	SYMBOL	DESCRIPTION
1	s	source
2	d	drain
3	g	gate

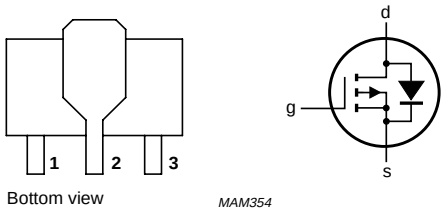

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Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–240	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{GS} = V_{DS}	–2.8	V
I_D	drain current (DC)		–200	mA
R_{DSon}	drain-source on-state resistance	I_D = –200 mA; V_{GS} = –10 V	12	Ω

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–240	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–200	mA
I_{DM}	peak drain current		–	–600	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C

Note

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note

1. Device mounted on a ceramic substrate; area 2.5 cm^2; thickness 0.7 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 µA	–240	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}$; I_D = –1 mA	–0.8	–	–2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –60 V	–	–	–200	nA
		V_{GS} = –0.2 V; V_{DS} = –200 V	–	–0.1	–60	µA
I_{GSS}	gate leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –200 mA	–	10	12	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –200 mA	60	200	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	55	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	20	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	5	15	pF
Switching times (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	20	30	ns

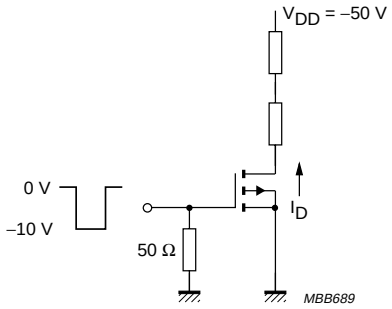


Fig.2 Switching times test circuit.

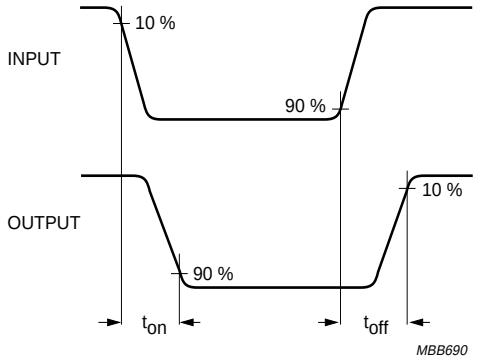


Fig.3 Input and output waveforms.

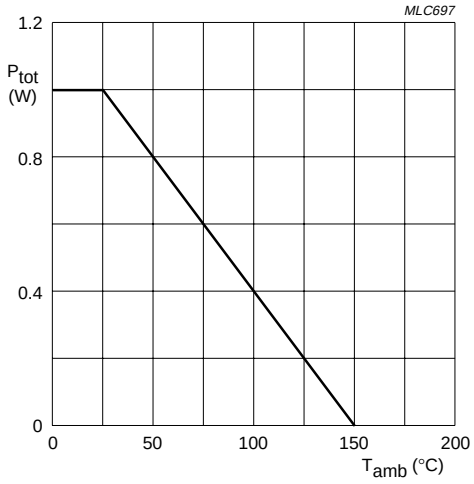
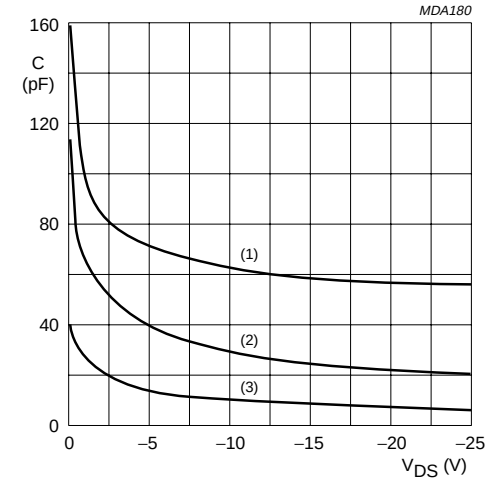
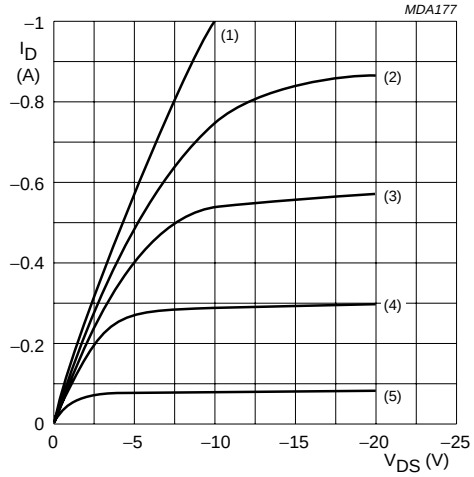


Fig.4 Power derating curve.



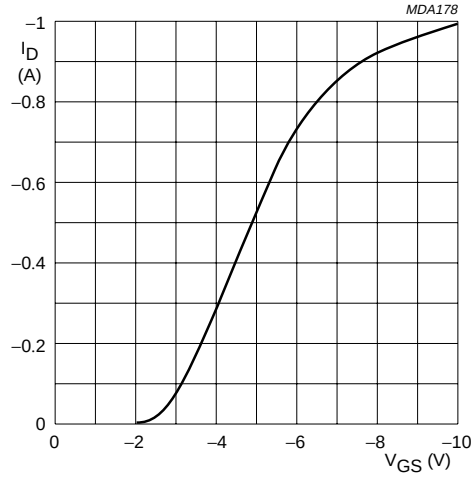
V_{GS} = 0; T_j = 25 °C; f = 1 MHz.
(1) C_{iss}.
(2) C_{oss}.
(3) C_{rss}.

Fig.5 Capacitance as a function of drain-source voltage; typical values.



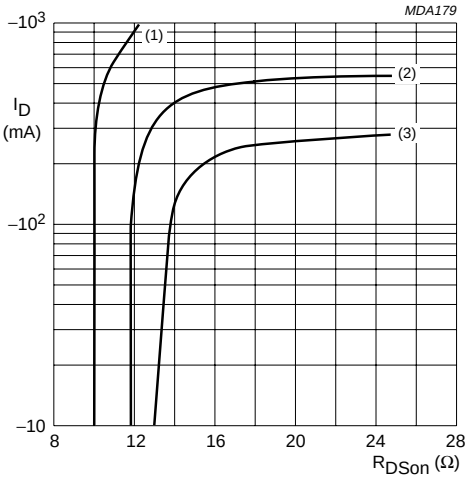
T_j = 25 °C.
(1) V_{GS} = −10 V.
(2) V_{GS} = −6 V.
(3) V_{GS} = −5 V.
(4) V_{GS} = −4 V.
(5) V_{GS} = −3 V.

Fig.6 Output characteristics; typical values.



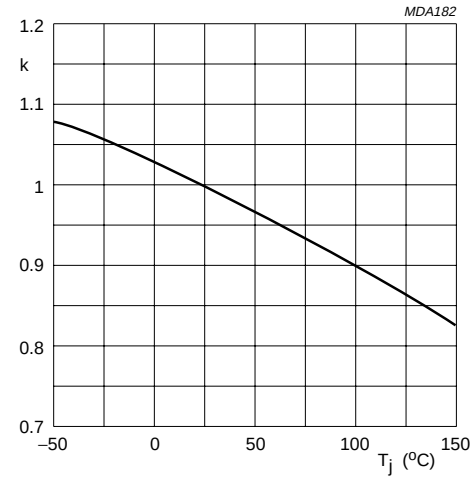
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristic; typical values.



T_j = 25 °C.
(1) V_{GS} = −10 V.
(2) V_{GS} = −5 V.
(3) V_{GS} = −4 V.

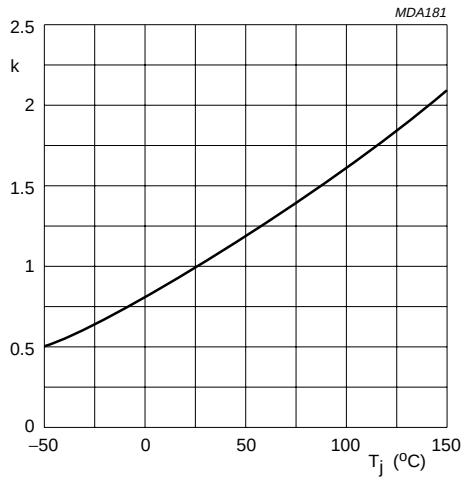
Fig.8 Drain current as a function of drain-source on-state resistance; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

V_{GSth} at I_D = −1 mA.

Fig.9 Temperature coefficient of gate-source threshold voltage; typical values.



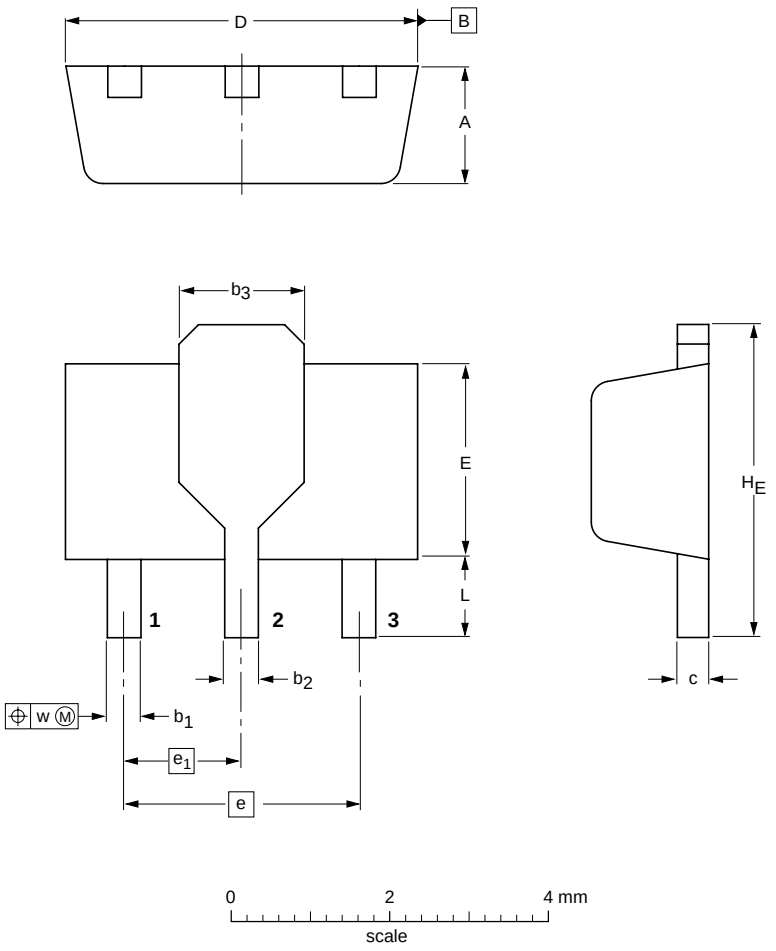
$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

I_D = –200 mA; V_{GS} = –10 V.

Fig.10 Temperature coefficient of drain-source on-state resistance; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads **SOT89**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89		TO-243	SC-62			~~97-02-28~~ 99-09-13

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