Unit: mm

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (U-MOSII)

SSM6J08FU

Power Management Switch DC-DC Converter

Small Package

Low on Resistance $\div R_{on}$ = 0.18 Ω (max) (@VGS = -4 V)

: $R_{on} = 0.26 \Omega \text{ (max) } (@V_{GS} = -2.5 \text{ V})$

Low Gate Threshold Voltage

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DS}	-20	V	
Gate-Source voltage		V _{GSS}	±12	V	
Drain current	DC	I _D	-1.3	A	
	Pulse	I _{DP} (Note 2)	-2.6		
Drain power dissipation		P _D (Note 1)	300	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

2.1 ± 0.1 1.25 ± 0.1 1, 2, 5, 6 : DRAIN : GATE : SOURCE US₆ **JEDEC** JEITA **TOSHIBA** 2-2J1D

Weight: 6.8 mg (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board

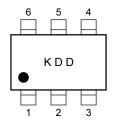
(25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.32 mm² \times 6) Fig: 1.

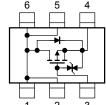
Note 2: The pulse width limited by max channel temperature.

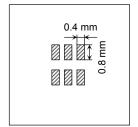
Marking

Equivalent Circuit

Fig 1: 25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.32 mm² \times 6







Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

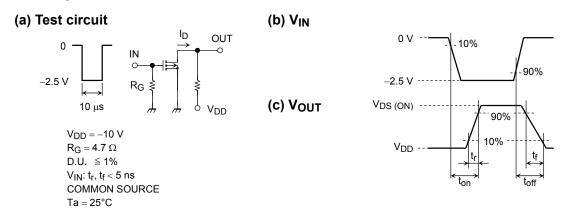
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Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I _{GSS}	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$	_	_	±1	μА
Drain-Source breakdown voltage	V (BR) DSS	$I_D = -1 \text{ mA}, V_{GS} = 0$	-20	_	_	V	
	V (BR) DSX	$I_D = -1 \text{ mA}, V_{GS} = 12 \text{ V}$	-8	_	_	V	
Drain Cut-off curr	ent	I _{DSS}	$V_{DS} = -20 \ V, \ V_{GS} = 0$	_	_	-1	μА
Gate threshold vo	oltage	V _{th}	$V_{DS} = -3 \text{ V}, I_D = -0.1 \text{ mA}$	-0.5	_	-1.1	V
Forward transfer	admittance	Y _{fs}	$V_{DS} = -3 \text{ V}, I_D = -0.65 \text{ A}$ (Note 3)	1.3	2.7	_	S
Drain-Source ON resistance			$I_D = -0.65 \text{ A}, V_{GS} = -4 \text{ V}$ (Note 3)) —	140	180	mΩ
		R _{DS (ON)}	$I_D = -0.65 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 3)) —	200	260	
			$I_D = -0.65 \text{ A}, V_{GS} = -2.0 \text{ V}$ (Note 3)) —	260	460	
Input capacitance	vacitance C_{iss} $V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		_	370	_	pF	
Reverse transfer capacitance		C _{rss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	73	_	pF
Output capacitance		C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	_	116	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = -10 \text{ V}, I_D = -0.65 \text{ A},$	_	33	_	ns
	Turn-off time	t _{off}	$V_{GS} = 0 \sim -2.5 \text{ V}, R_G = 4.7 \Omega$	_	47	_	ns

Note 3: Pulse test

Switching Time Test Circuit

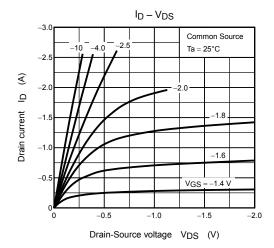


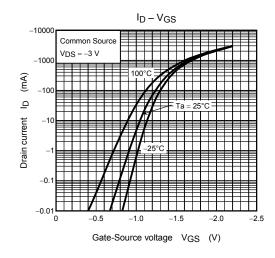
Precaution

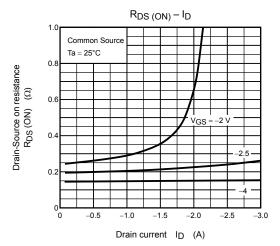
 V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = $-100~\mu A$ for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} .

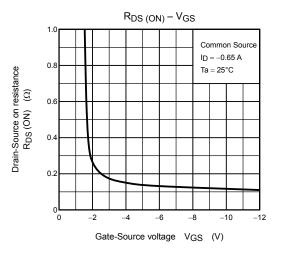
(relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$)

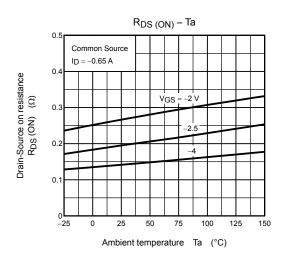
Please take this into consideration for using the device.

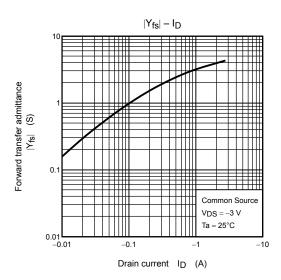




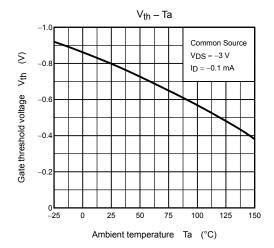


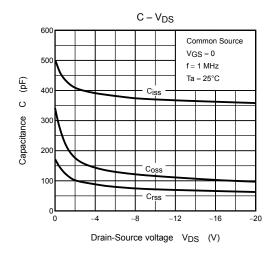


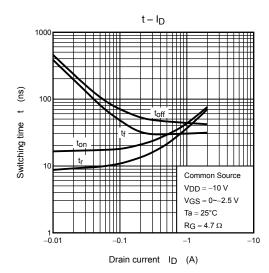


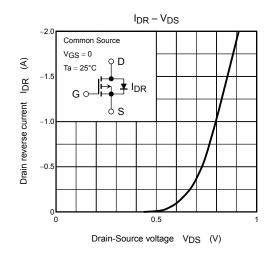


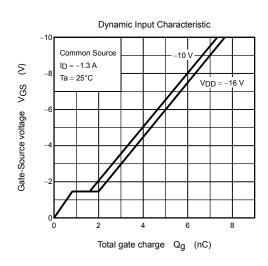
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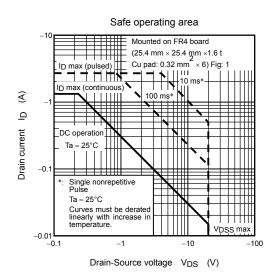




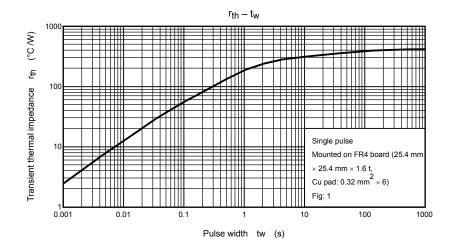


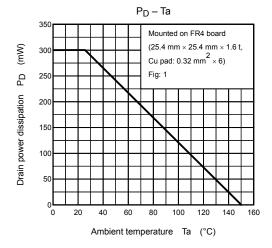






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