



## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package Option	$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$V_{GS(TH)}$ (max) (V)	$I_{D(ON)}$ (min) (mA)
	TO-92				
VN3515	VN3515L-G	350	15	1.8	150

-G indicates package is RoHS compliant ("Green")



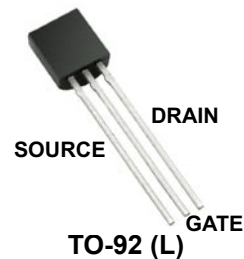
### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

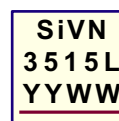
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Pin Configuration



### Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or TO-92 (L)

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (mA)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{ja}$ ( $^\circ\text{C}/\text{W}$ )	$I_{DR}$ <sup>†</sup> (mA)	$I_{DRM}$ (mA)
TO-92	150	600	1.0	125	170	150	600

### Notes:

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

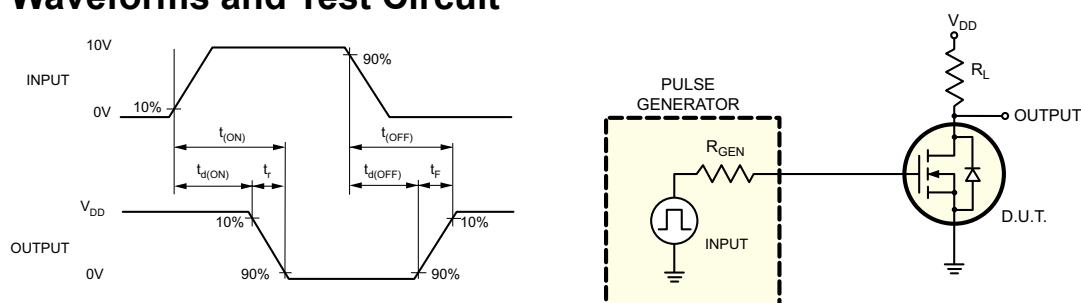
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	350	-	-	V	$V_{GS} = 0\text{V}$ , $I_D = 100\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	0.6	-	1.8	V	$V_{GS} = V_{DS}$ , $I_D = 1.0\text{mA}$
$I_{GSS}$	Gate body leakage	-	-	10	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
$I_{DSS}$	Zero gate voltage drain current	-	-	1	$\mu\text{A}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 0.8$ Max Rating
		-	-	100		$V_{DS} = 0.8$ Max Rating, $V_{GS} = 0\text{V}$ , $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	0.15	0.3	-	A	$V_{GS} = 4.5\text{V}$ , $V_{DS} = 10\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	9.5	15	$\Omega$	$V_{GS} = 4.5\text{V}$ , $I_D = 100\text{mA}$
		-	17	35		$V_{GS} = 4.5\text{V}$ , $I_D = 100\text{mA}$ , $T_A = 125^\circ\text{C}$
$G_{FS}$	Forward transductance	125	350	-	mmho	$V_{DS} = 15\text{V}$ , $I_D = 100\text{mA}$
$C_{ISS}$	Input capacitance	-	-	110	$\text{pF}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1.0\text{MHz}$
$C_{OSS}$	Common source output capacitance	-	-	30		
$C_{RSS}$	Reverse transfer capacitance	-	-	10		
$t_r$	Rise time	-	-	20	ns	$V_{DD} = 25\text{V}$ , $I_D = 100\text{mA}$ , $R_{GEN} = 25\Omega$
$t_{d(ON)}$	Turn-on delay time	-	-	20		
$t_f$	Fall time	-	-	65		
$t_{d(OFF)}$	Turn-off delay time	-	-	65		
$V_{SD}$	Diode forward voltage drop	-	-	1.2	V	$V_{GS} = 0\text{V}$ , $I_{SD} = 160\text{mA}$

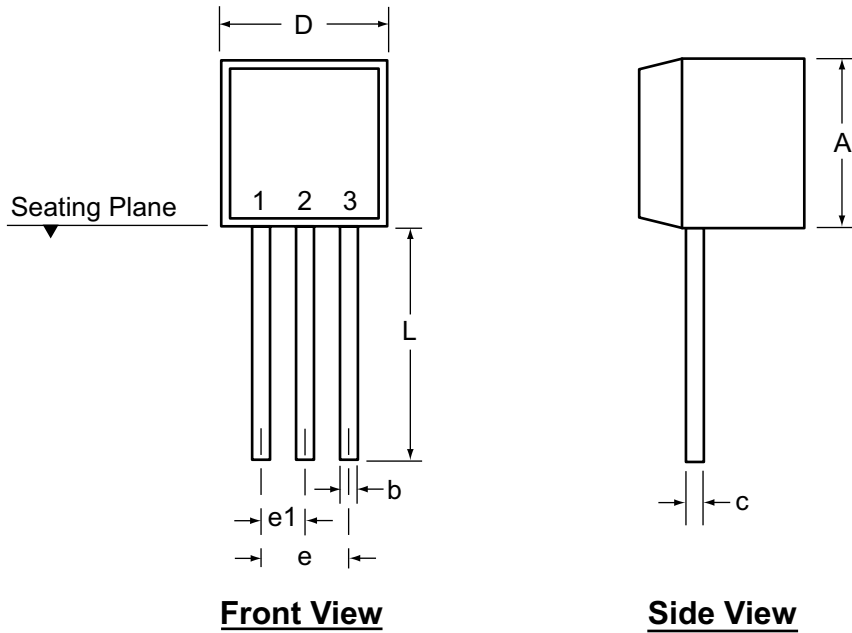
### Notes:

- All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit



### 3-Lead TO-92 Package Outline (L)



Symbol	A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the original JEDEC drawing. The value listed is for reference only.

† This dimension is a non-JEDEC dimension.

Drawings not to scale.

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(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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