



# PSMN015-60BS

N-channel 60 V 14.8 mΩ standard level MOSFET in D2PAK

Rev. 2 — 1 March 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

### 1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

### 1.4 Quick reference data

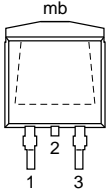
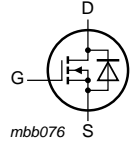
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	60	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>	-	-	50	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	86	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 100\text{ °C}$ ; see <a href="#">Figure 12</a>	-	-	23.7	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a>	-	12.6	14.8	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 30\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	4.7	-	nC
$Q_{G(tot)}$	total gate charge		-	20.9	-	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 50\text{ A}$ ; $V_{sup} \leq 60\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; unclamped	-	-	44	mJ



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		

**SOT404 (D2PAK)**

[1] It is not possible to make connection to pin 2

## 3. Ordering information

Table 3. Ordering information

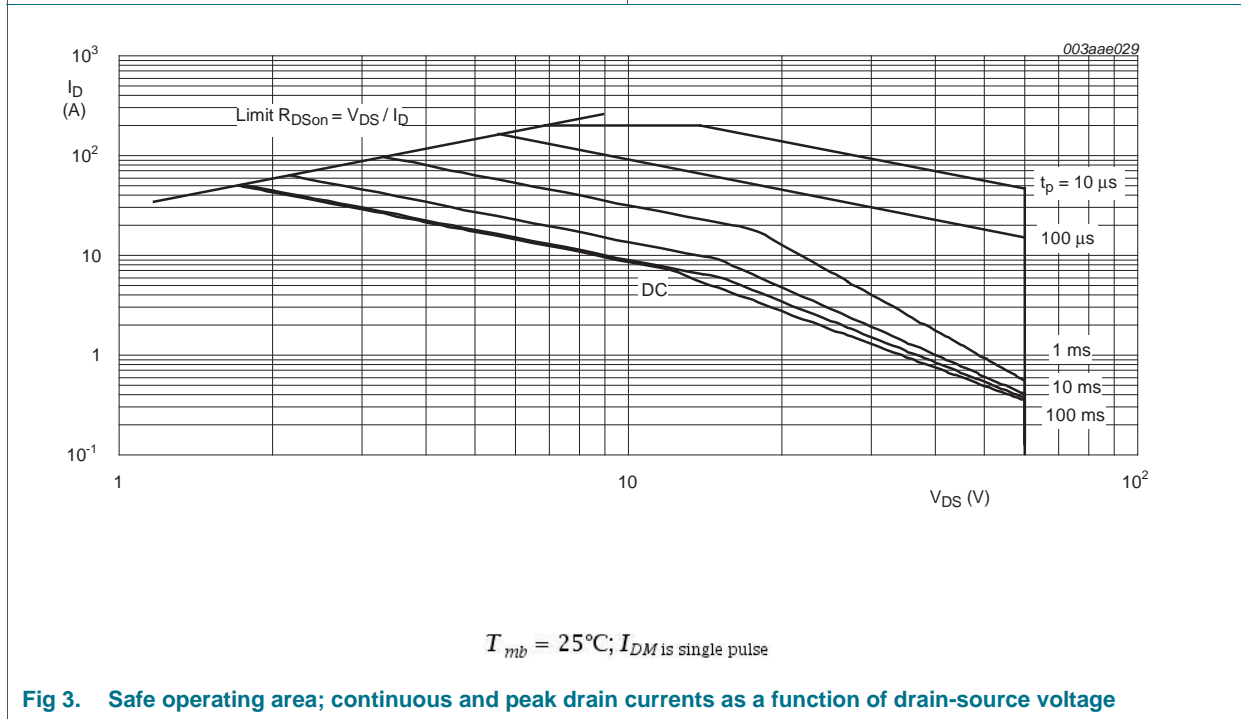
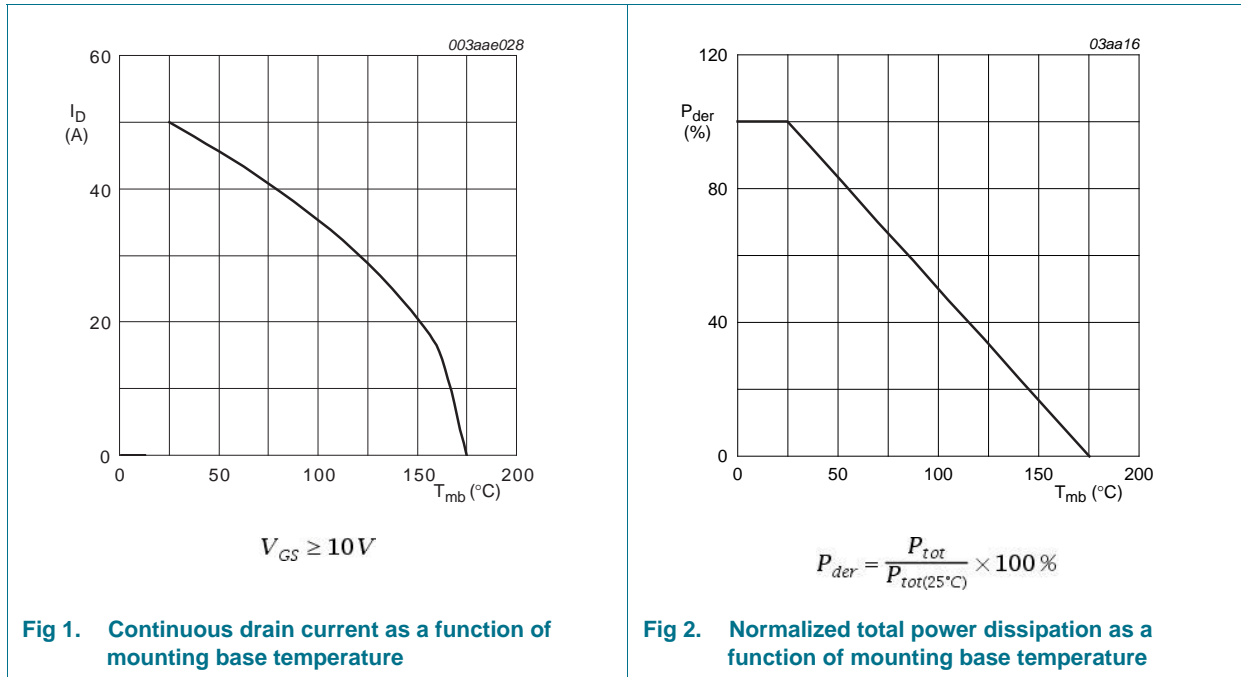
Type number	Package		Version
	Name	Description	
PSMN015-60BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

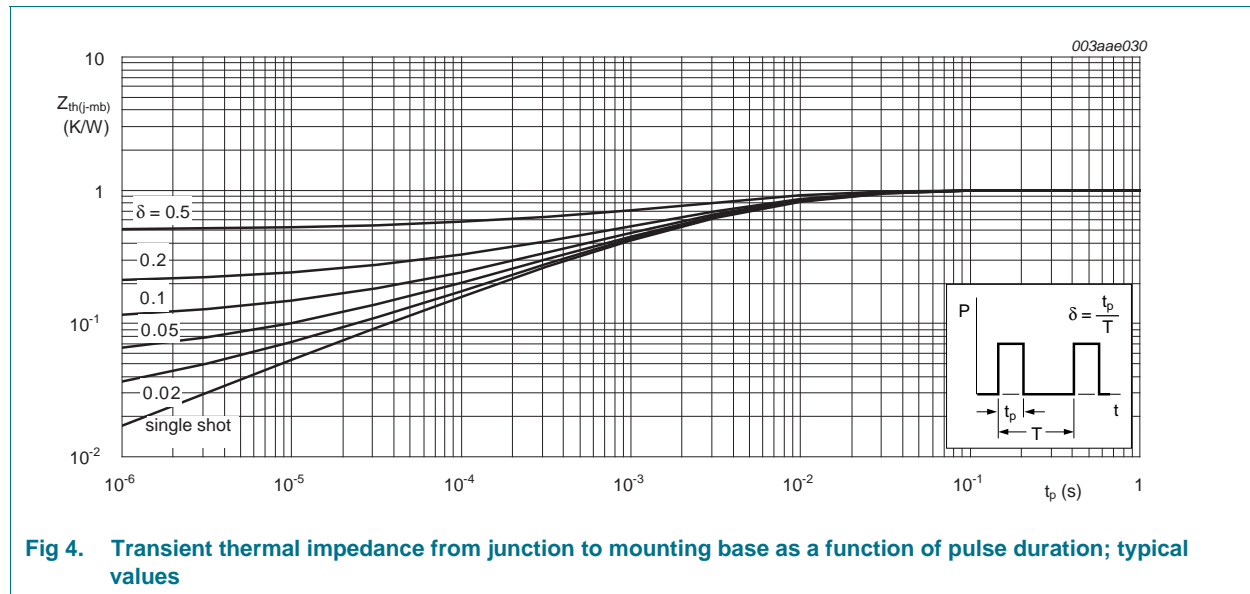
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	36	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	50	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	201	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	86	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
$T_{slid(M)}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	50	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	201	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 50\text{ A}; V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ }\Omega$ ; unclamped	-	44	mJ



### 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	1	1.74	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	60	-	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values**

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	2	3	4	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	-	4.8	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.03	2	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$	-	-	30	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	10	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	28.9	34	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 100 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	-	23.7	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	12.6	14.8	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.3	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	20.9	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	17	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	6.2	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a>	-	3.7	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.4	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	4.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 30 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	4.8	-	V
$C_{iss}$	input capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 16</a>	-	1220	-	pF
$C_{oss}$	output capacitance		-	169	-	pF
$C_{rss}$	reverse transfer capacitance		-	95	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; R_L = 1.2 \text{ } \Omega; V_{GS} = 10 V$ ; $R_{G(ext)} = 4.7 \text{ } \Omega$	-	12	-	ns
$t_r$	rise time		-	13	-	ns
$t_{d(off)}$	turn-off delay time		-	27	-	ns
$t_f$	fall time		-	7	-	ns

Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 30\text{ V}$	-	31	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}; V_{DS} = 30\text{ V}$	-	28.5	-	nC

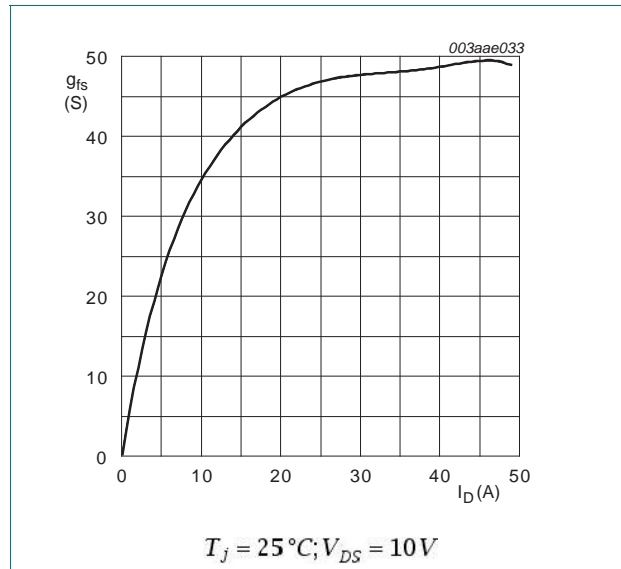


Fig 5. Forward transconductance as a function of drain current; typical values

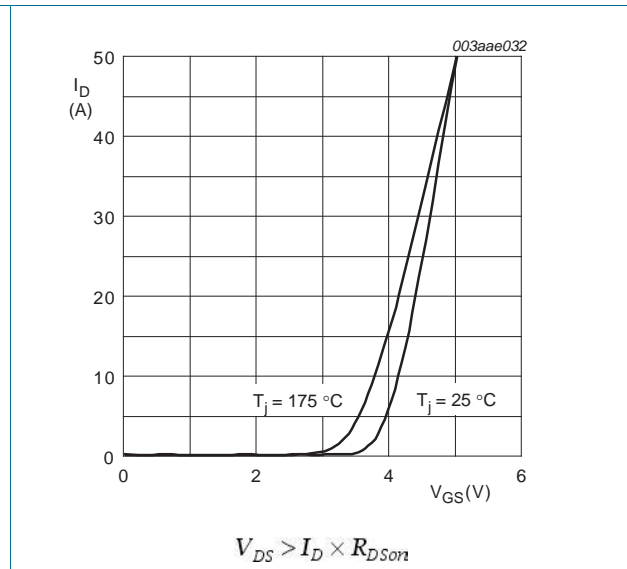


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

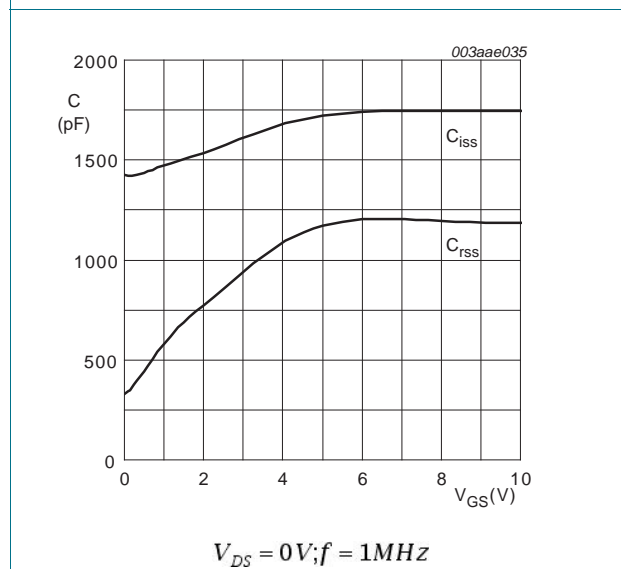


Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

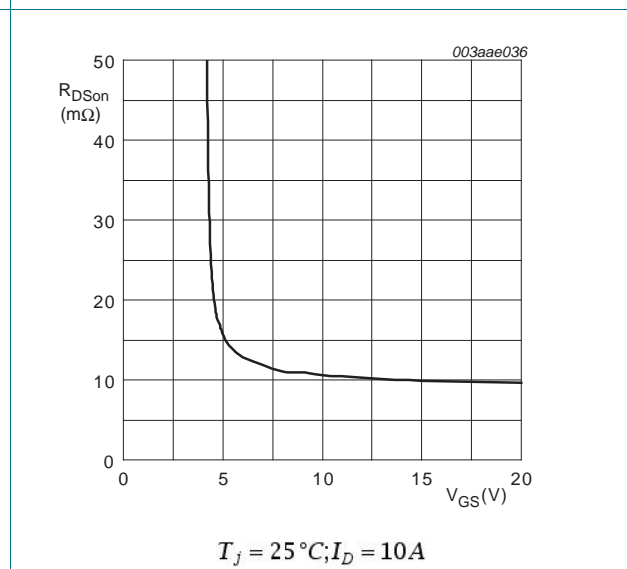


Fig 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

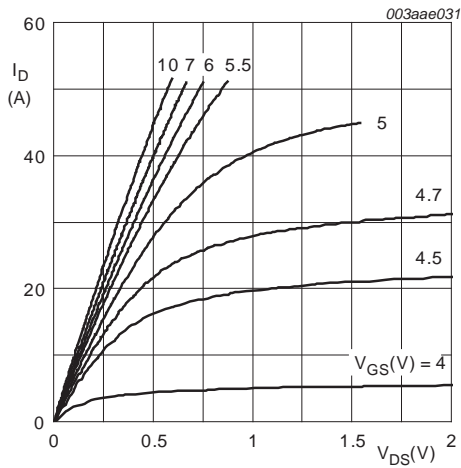


Fig 9. Output characteristics: drain current as a function of drain-source voltage; typical values

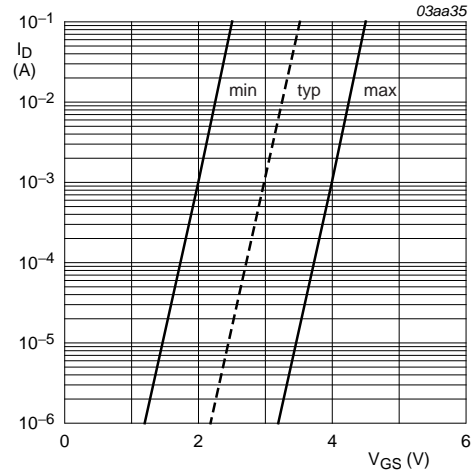


Fig 10. Sub-threshold drain current as a function of gate-source voltage

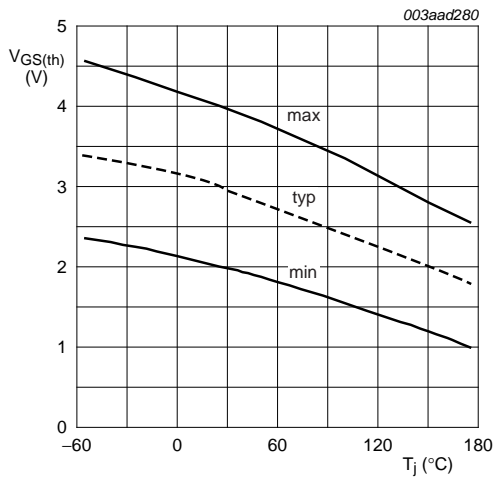
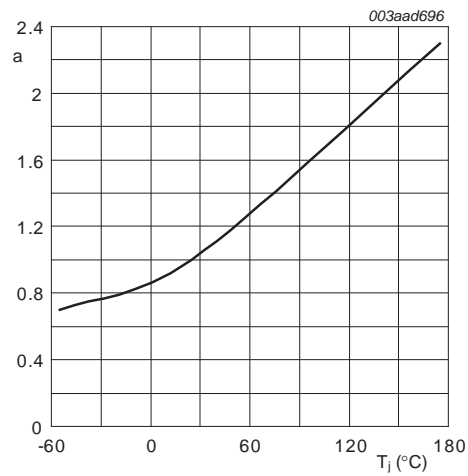
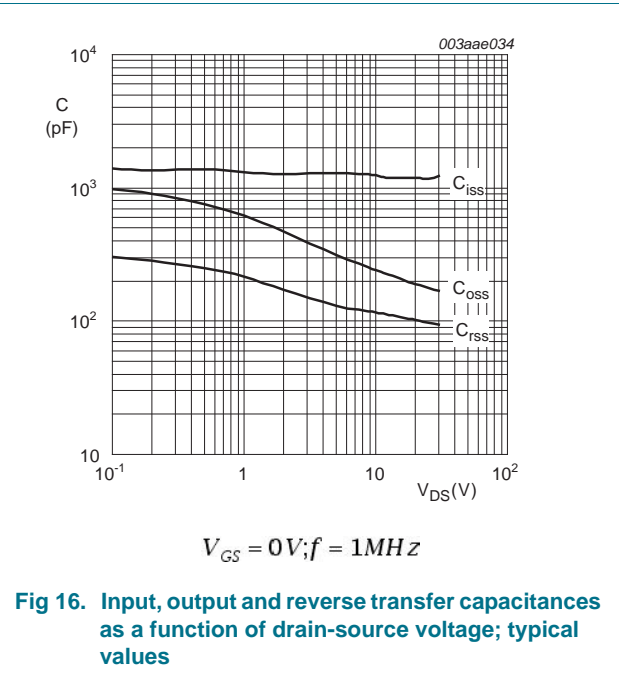
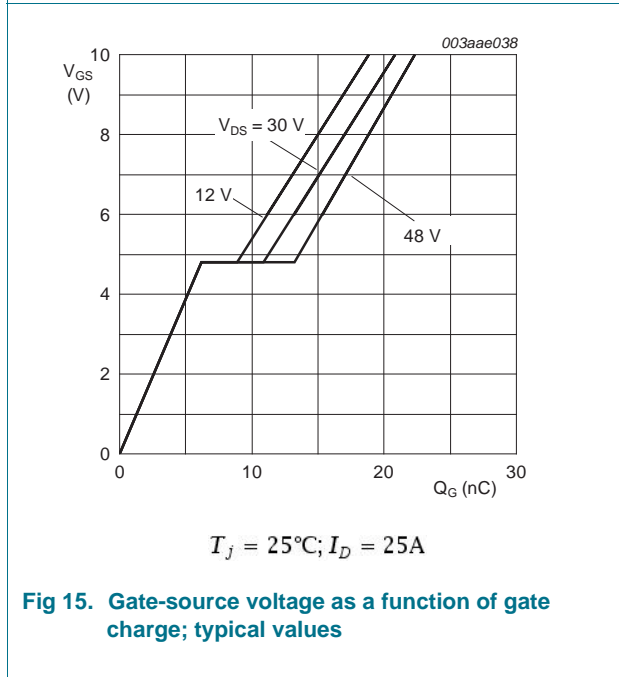
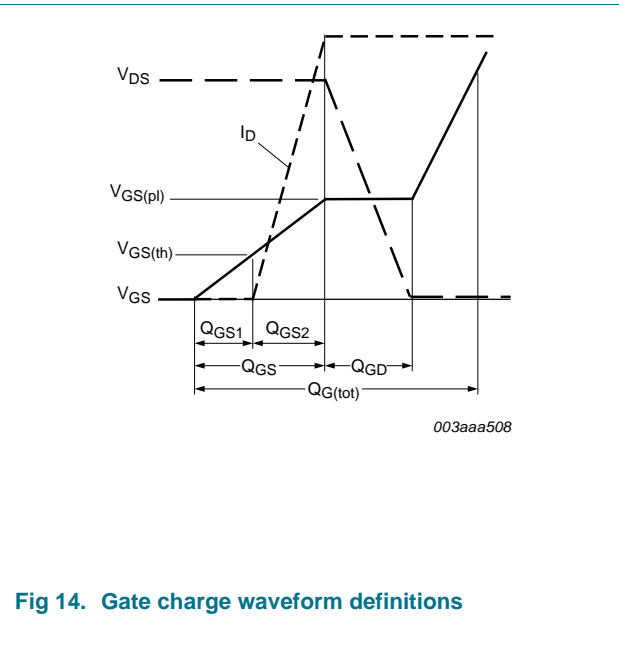
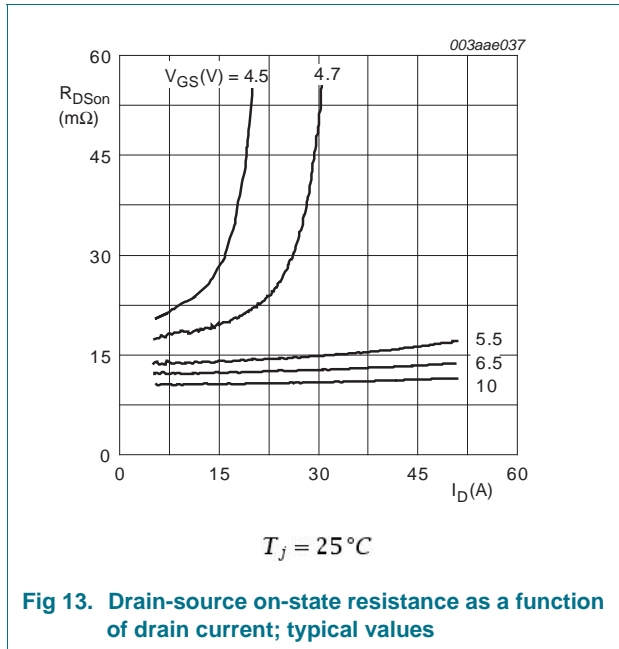


Fig 11. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DS(on)}}{R_{DS(on)25^\circ C}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature.





7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

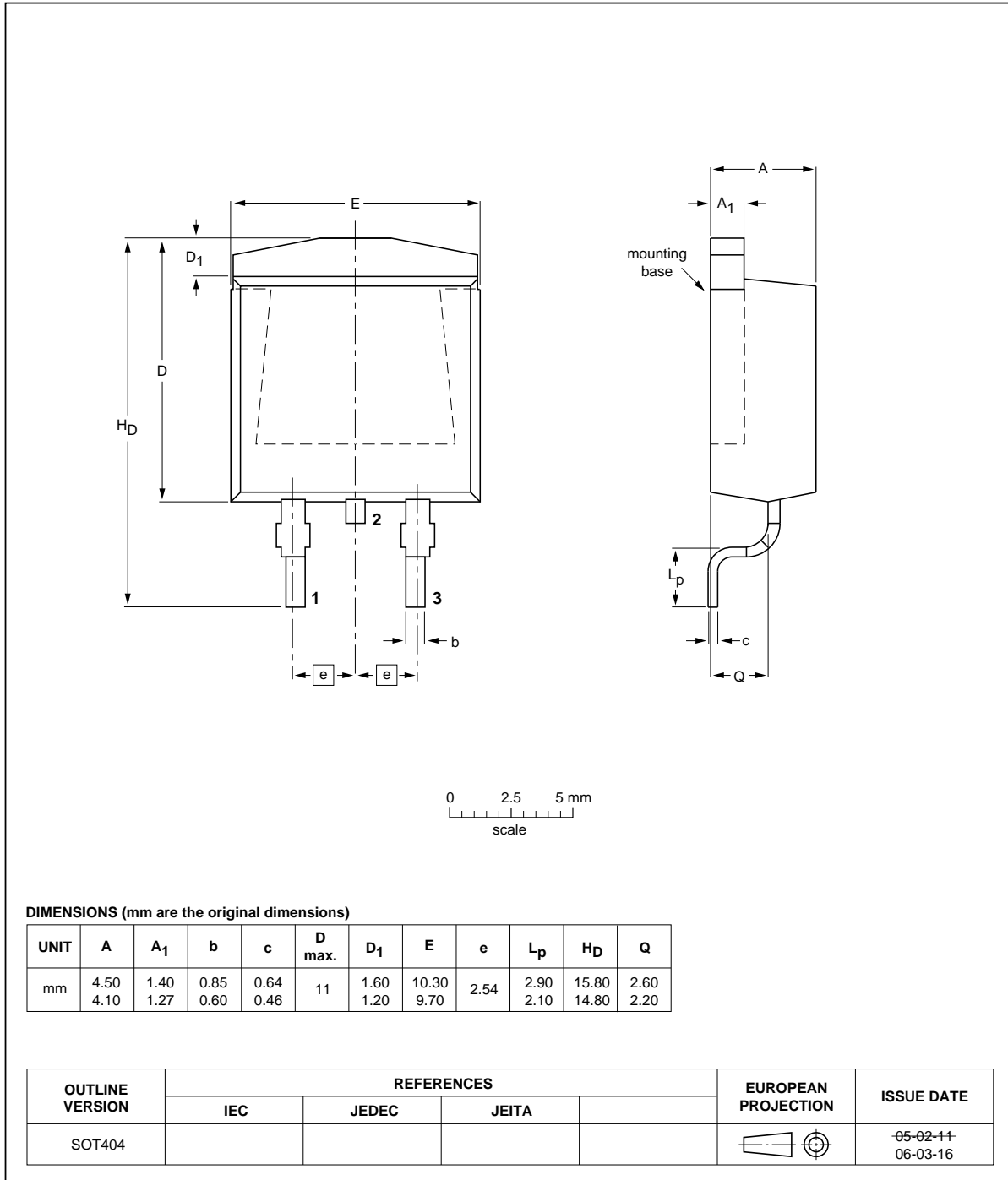


Fig 17. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN015-60BS v.2	20120301	Product data sheet	-	PSMN015-60BS v.1
Modifications:	<ul style="list-style-type: none"><li>• Status changed from objective to product.</li><li>• Various changes to content.</li></ul>			
PSMN015-60BS v.1	20111021	Objective data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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