



PSMN010-25YLC

N-channel 25 V 10.6 mΩ logic level MOSFET in LPAK using NextPower technology

Rev. 2 — 25 October 2011

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

1.4 Quick reference data

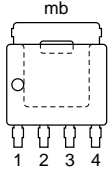
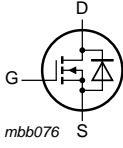
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	25	V
I_D	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 1	-	-	39	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ see Figure 2	-	-	30	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ see Figure 12	-	11.9	14	mΩ
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ see Figure 12	-	9	10.6	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}; I_D = 10\text{ A}; V_{DS} = 12\text{ V};$ see Figure 14 ; see Figure 15	-	1.5	-	nC
$Q_{G(tot)}$	total gate charge		-	5	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

**SOT669 (LFAK;
Power-SO8)**

3. Ordering information

Table 3. Ordering information

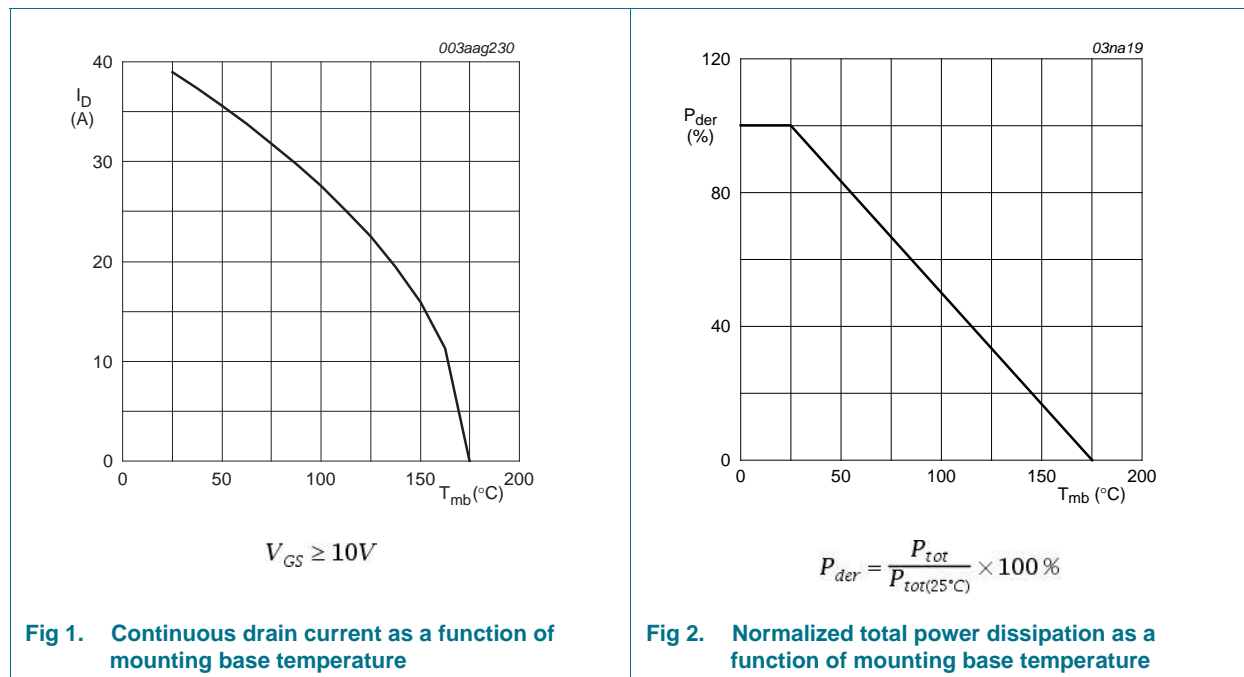
Type number	Package		Version
	Name	Description	
PSMN010-25YLC	LFAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	25	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	25	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	-	39	A
		V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	-	28	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; see Figure 4	-	158	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	30	W
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	110	-	V
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	27	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	158	A
Avalanche ruggedness					
E _{DS(AL)}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 39 A; V _{sup} ≤ 25 V; unclamped; R _{GS} = 50 Ω; see Figure 3	-	9	mJ



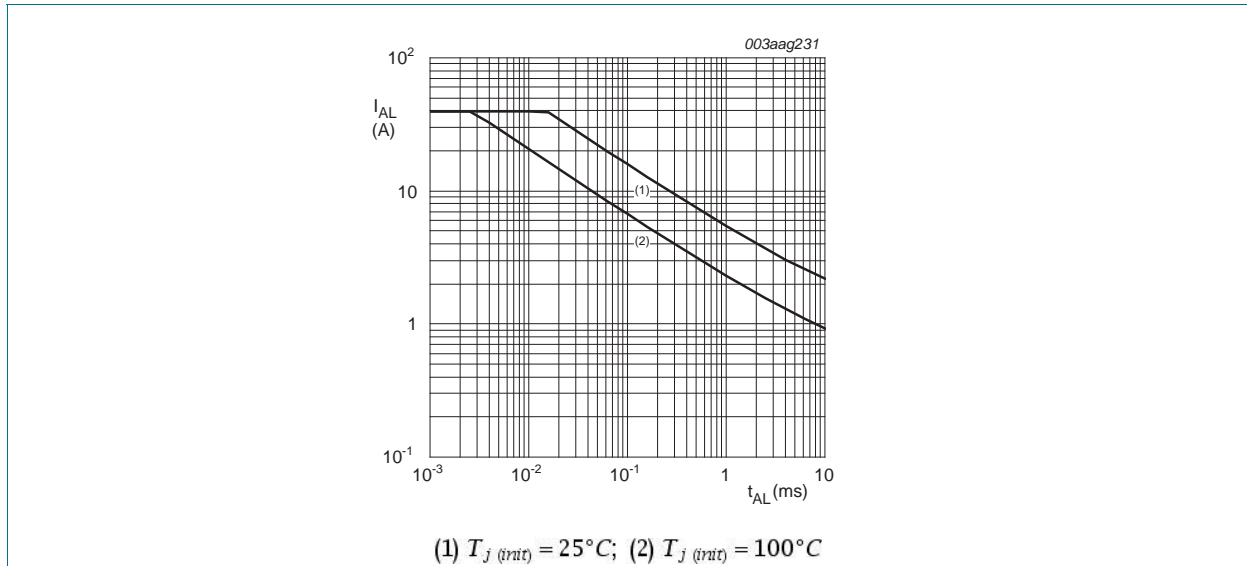


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

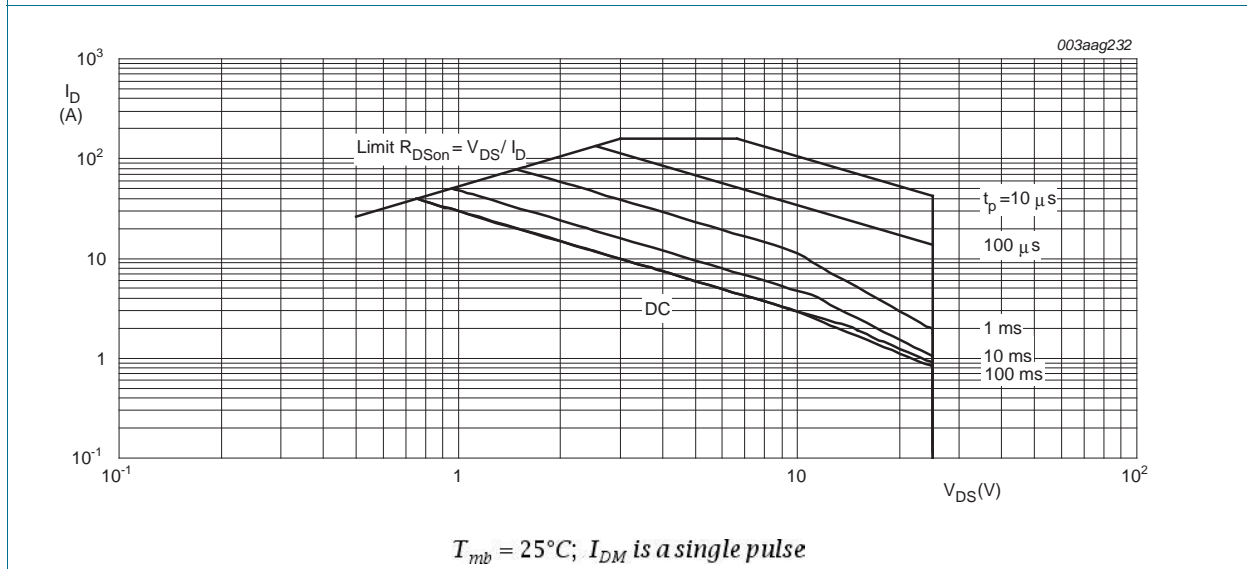


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	4.87	5.06	K/W

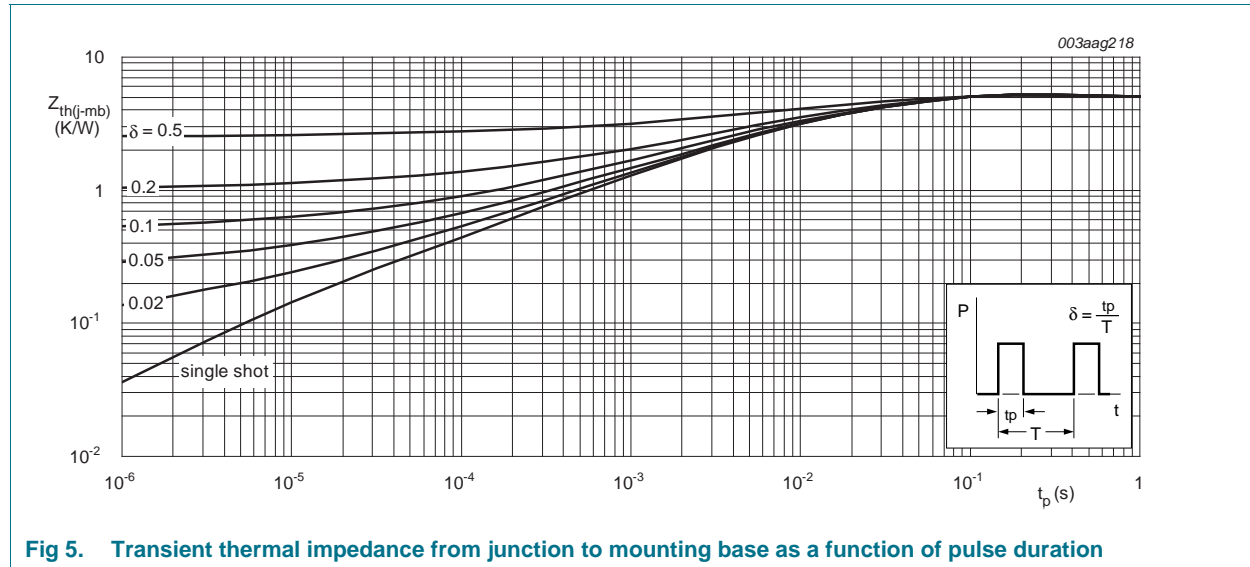


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

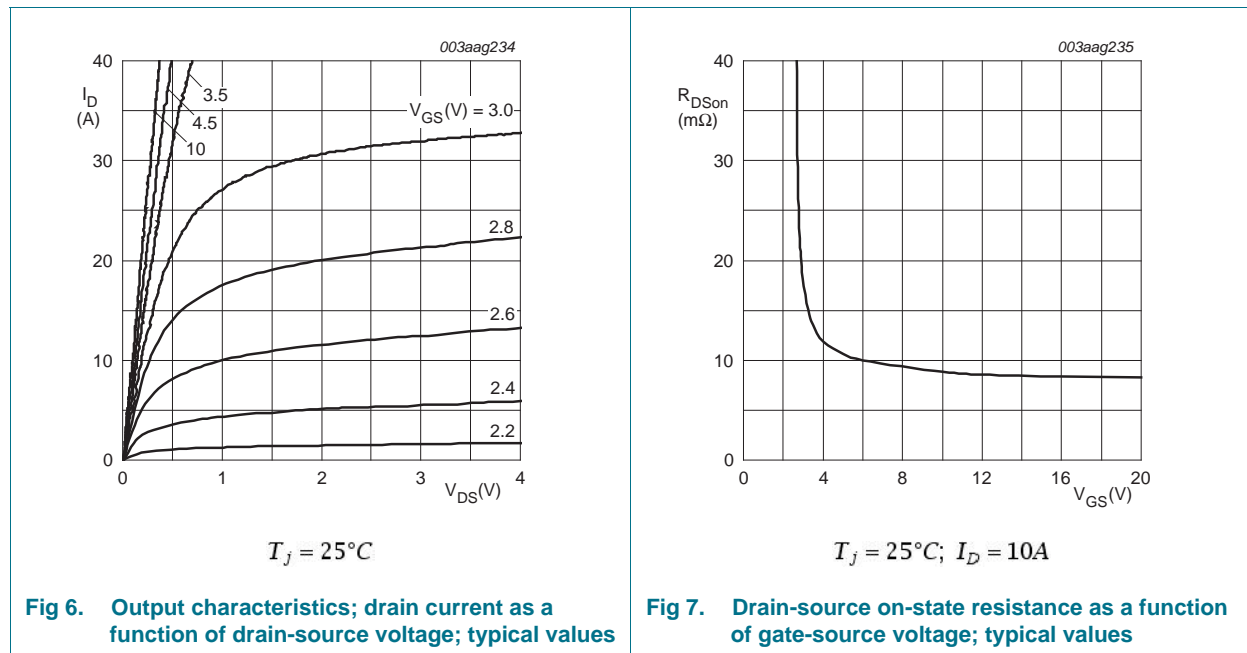
6. Characteristics

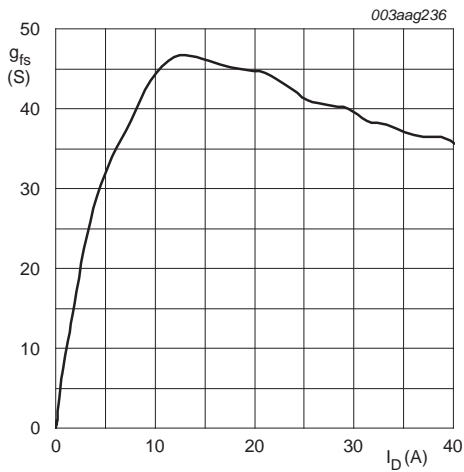
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 10 ; see Figure 11	1.05	1.6	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 12	-	11.9	14	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ C$; see Figure 12 ; see Figure 13	-	-	22.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C$; see Figure 12	-	9	10.6	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 150 \text{ }^\circ C$; see Figure 12 ; see Figure 13	-	-	16.9	mΩ
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	2	4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V}$; see Figure 14 ; see Figure 15	-	11	-	nC
		$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V}$; see Figure 14 ; see Figure 15	-	5	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	9.5	-	nC
Q_{GS}	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V}$; see Figure 14 ; see Figure 15	-	1.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.1	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	0.4	-	nC
Q_{GD}	gate-drain charge		-	1.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 10 \text{ A}; V_{DS} = 12 \text{ V}$; see Figure 14 ; see Figure 15	-	2.54	-	V
C_{iss}	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$;	-	678	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$; see Figure 16	-	166	-	pF
C_{rss}	reverse transfer capacitance		-	55	-	pF

Table 6. Characteristics ...continued

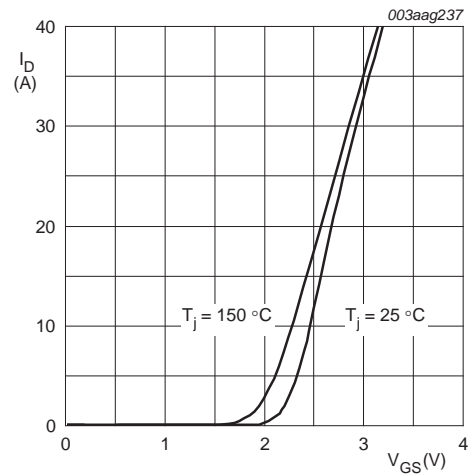
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.6\ \Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 4.7\ \Omega$	-	10.7	-	ns
t_r	rise time		-	9.8	-	ns
$t_{d(off)}$	turn-off delay time		-	11.5	-	ns
t_f	fall time		-	4.2	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz}$	-	3.9	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 17	-	0.85	1.1	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 12\text{ V}$	-	15.1	-	ns
Q_r	recovered charge		-	4.8	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}; I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s};$ $V_{DS} = 12\text{ V};$ see Figure 18	-	8.8	-	ns
t_b	reverse recovery fall time		-	6.3	-	ns





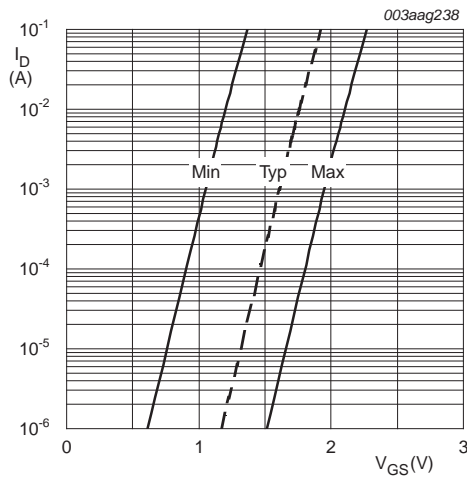
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values



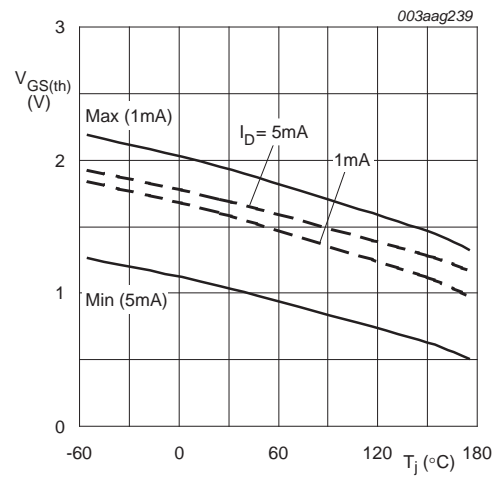
$V_{DS} = 10\text{V}$

Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



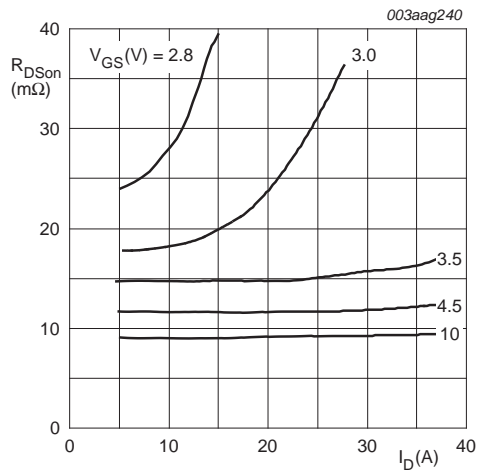
$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



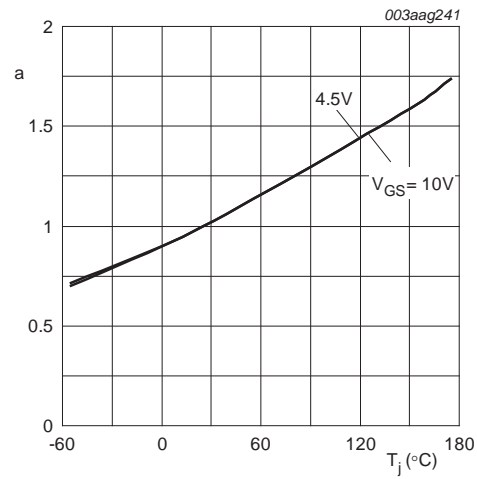
$V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



$T_j = 25^\circ C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

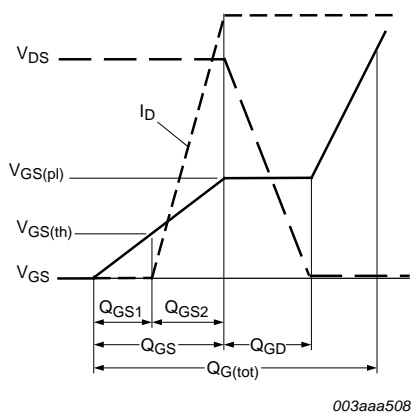
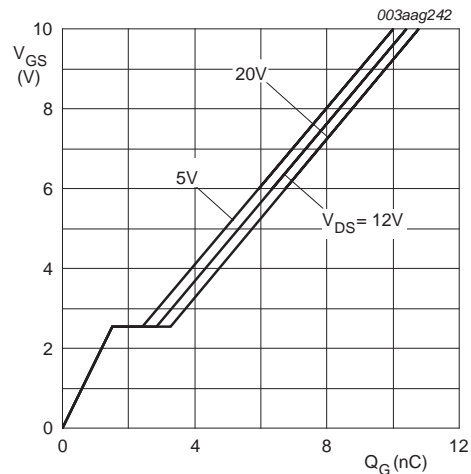
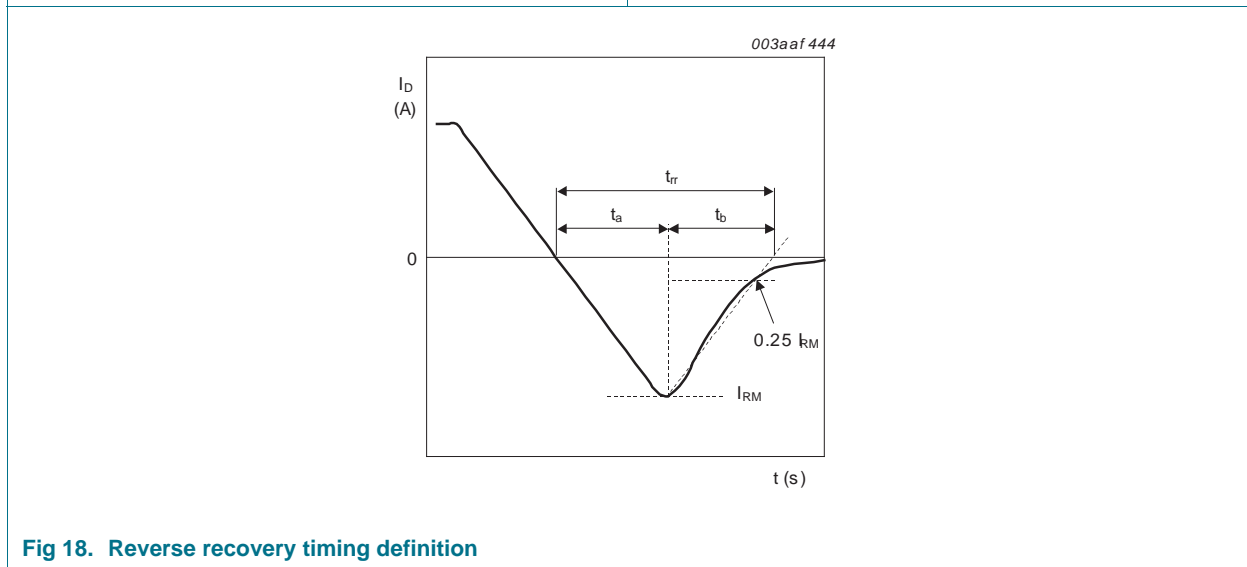
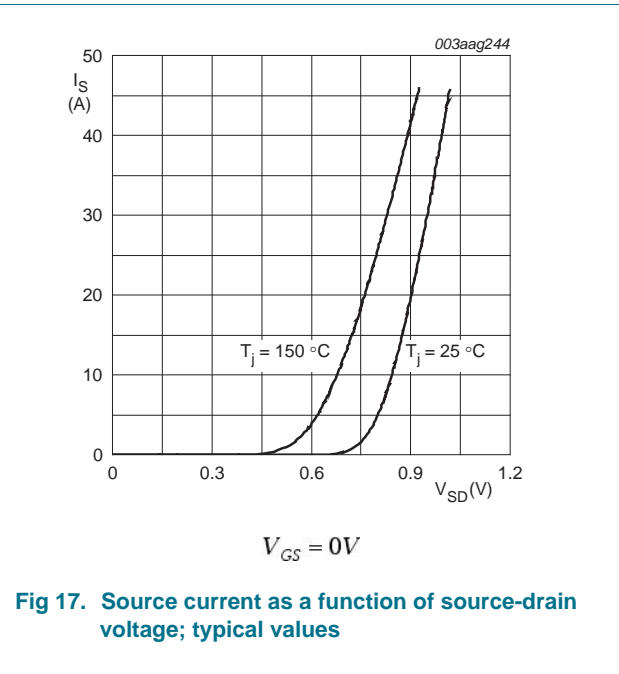
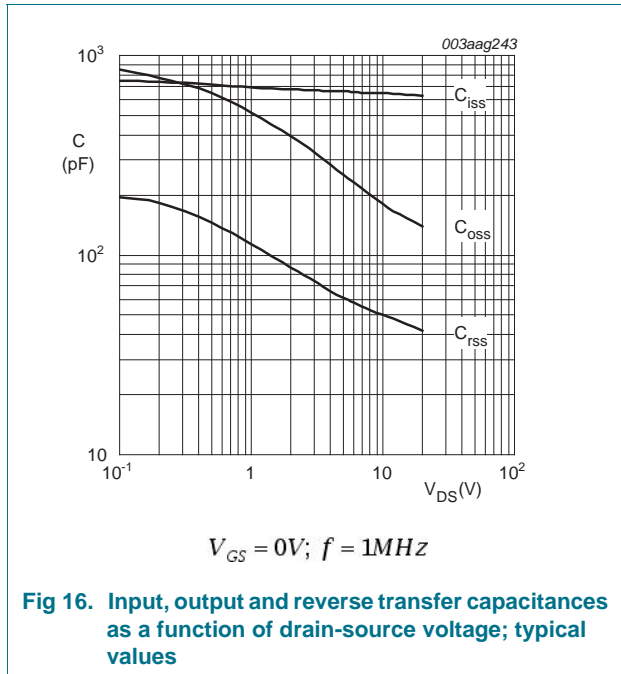


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ C; I_D = 10A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



7. Package outline

Plastic single-ended surface-mounted package (LFPAK; Power-SO8); 4 leads

SOT669

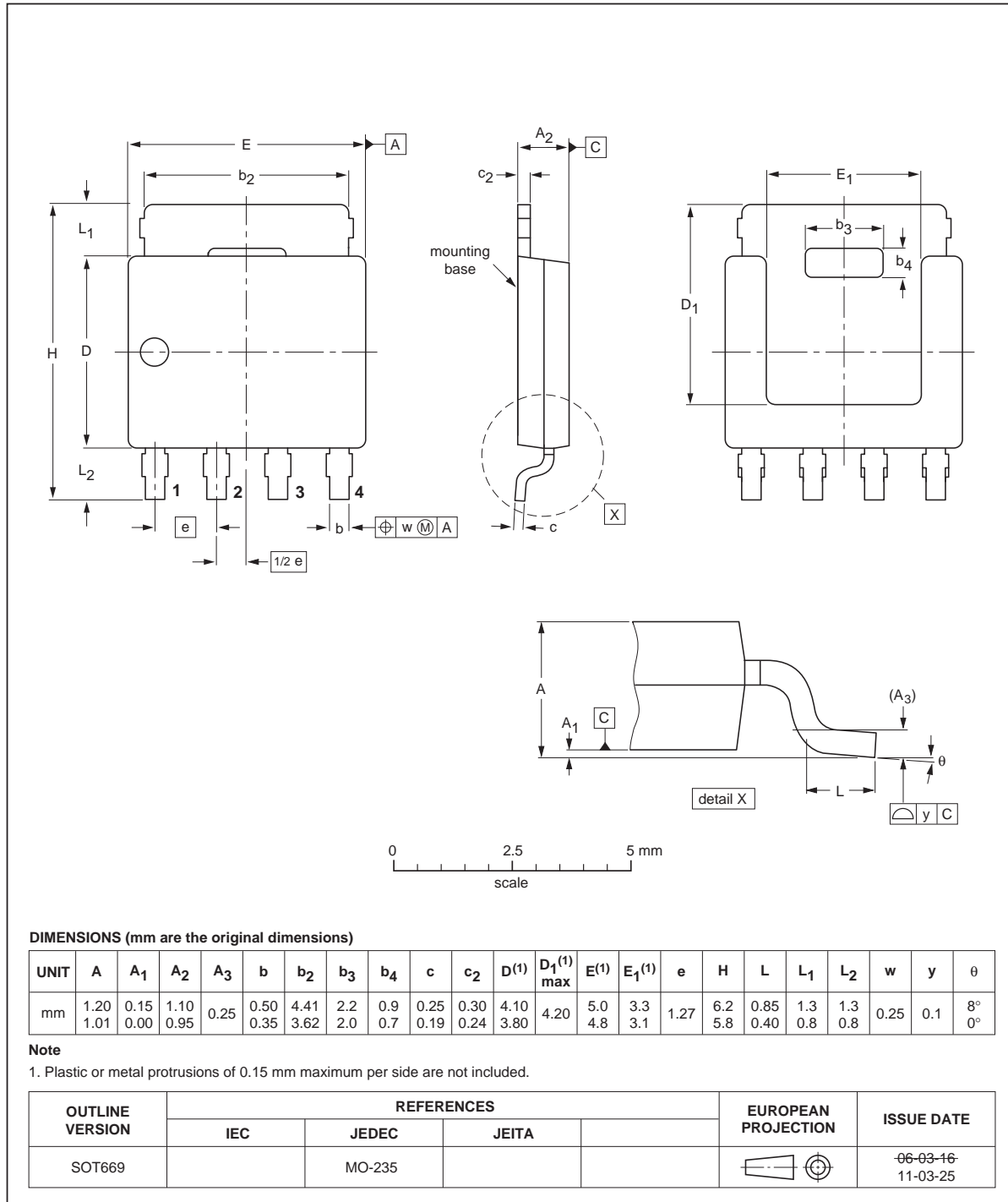


Fig 19. Package outline SOT669 (LFPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN010-25YLC v.2	20111025	Product data sheet	-	PSMN010-25YLC v.1
Modifications:	• Data sheet status changed from preliminary to product.			
PSMN010-25YLC v.1	20110923	Preliminary data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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