

DMP1245UFCL

12V P-CHANNEL ENHANCEMENT MODE MOSFET

Summary

| V _{(BR)DSS} | R _{DS(on)} max | I _D max |
|----------------------|--------------------------------|--------------------|
| -12V | 29mΩ @V _{GS} = -4.5V | -6.6 A |
| | 45mΩ @V _{GS} = -2.5V | -5.3 A |
| | 60mΩ @V _{GS} = -1.8V | -4.6 A |
| | 100mΩ @V _{GS} = -1.5V | -3.5 A |

Application

This device provides a high performance, low R_{DS(ON)} P channel MOSFETs in the thermally and space efficient X1-DFN1616-6 package. The low R_{DS(ON)} of this MOSFET ensures conduction losses are kept making it ideal for use as a:

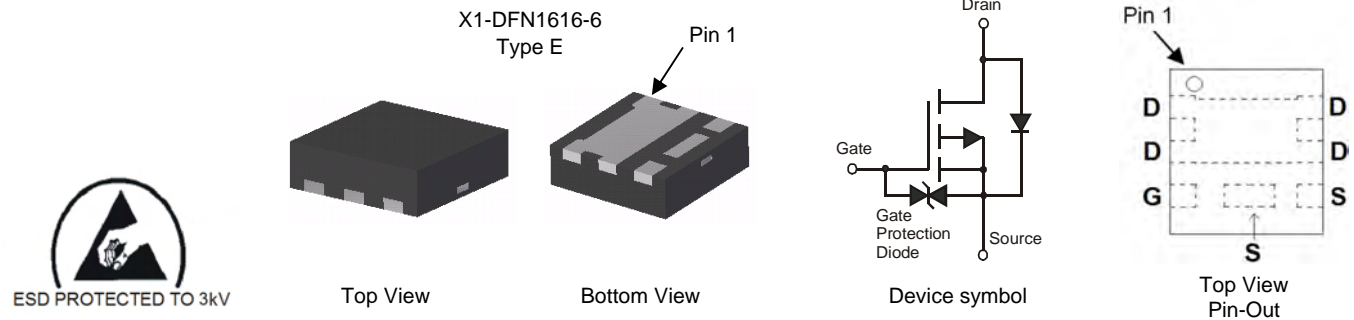
- Battery disconnect switch
- Load switch for power management functions

Features and Benefits

- Typical off board profile of 0.5mm - ideally suited for thin applications
- Low R_{DS(ON)} – minimizes conduction losses
- PCB footprint of 2.56mm²
- **3kV ESD Protected Gate** – protected against human borne ESD
- "Lead-Free", RoHS Compliant (Note 1)
- "Green" Device (Note 2)

Mechanical Data

- Case: X1-DFN1616-6 Type E
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Lead Free Plating (NiPdAu Finish over Copper leadframe).
- Terminals: Solderable per MIL-STD-202, Method 208
- Weight: 0.04 grams (approximate)

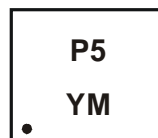


Ordering Information (Note 3)

| Product | Marking | Reel size (inches) | Tape width (mm) | Quantity per reel |
|---------------|---------|--------------------|-----------------|-------------------|
| DMP1245UFCL-7 | P5 | 7 | 8 | 3,000 |

- Notes:
1. No purposefully added lead.
 2. Diodes Inc's "Green" Policy can be found on our website at <http://www.diodes.com>
 3. For packaging details, go to our website at <http://www.diodes.com>

Marking Information



P5 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: X = 2010)
 M = Month (ex: 9 = September)

Date Code Key

| Year | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 |
|------|------|------|------|------|------|------|------|
| Code | Y | Z | A | B | C | D | E |

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | O | N | D |

Maximum Ratings @T_A = 25°C unless otherwise specified

| Characteristic | Symbol | Value | Units |
|-----------------------------------|------------------|--|-------|
| Drain-Source Voltage | V _{DSS} | -12 | V |
| Gate-Source Voltage | V _{GSS} | ±8 | V |
| Continuous Drain Current (Note 5) | I _D | -6.6 -5.25 | A |
| | | @ T _A = 25°C @ T _A = 70°C | |
| Pulsed Drain Current | I _{DM} | -16.67 | A |
| | | T _P = 10µs | |

Thermal Characteristics @T_A = 25°C unless otherwise specified

| Characteristic | Symbol | Value | Units |
|---|-----------------------------------|-------------|-------|
| Total Power Dissipation | P _D | 613 | mW |
| | | 1.7 | W |
| Thermal Resistance, Junction to Ambient | R _{θJA} | 204 | °C/W |
| | | 74 | |
| Operating and Storage Temperature Range | T _J , T _{STG} | -55 to +150 | °C |

- Notes:
4. For a device surface mounted on minimum recommended pad layout, in still air conditions; the device is measured when operating in a steady state condition.
 5. For a device surface mounted on 25mm by 25mm by 1.6mm FR4 PCB with high coverage of single sided 2oz copper, in still air conditions; the device is measured when operating in a steady state condition.

Thermal Characteristics

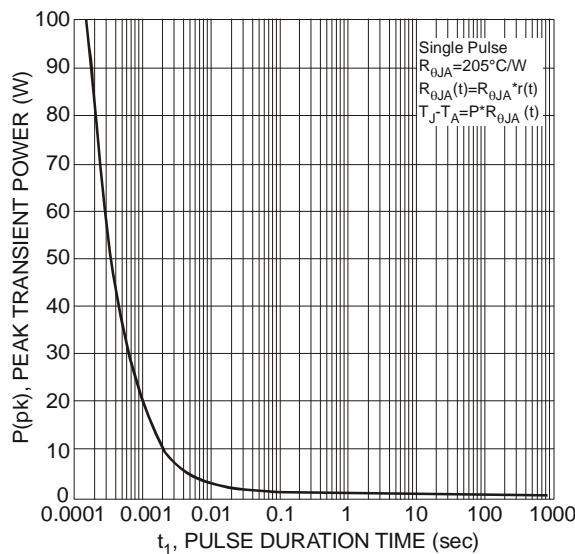


Fig. 1 Single Pulse Maximum Power Dissipation

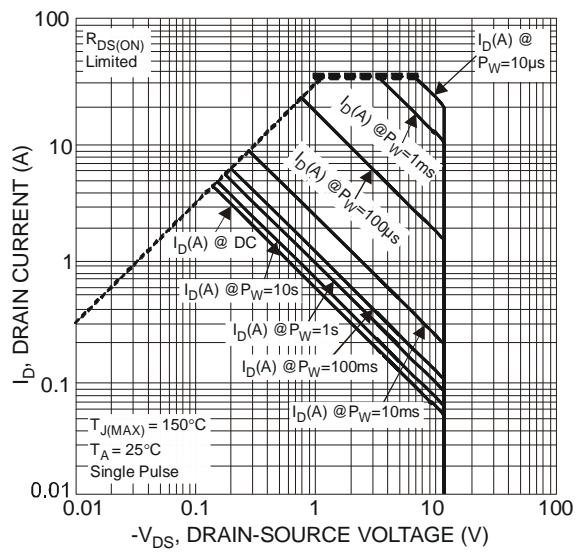
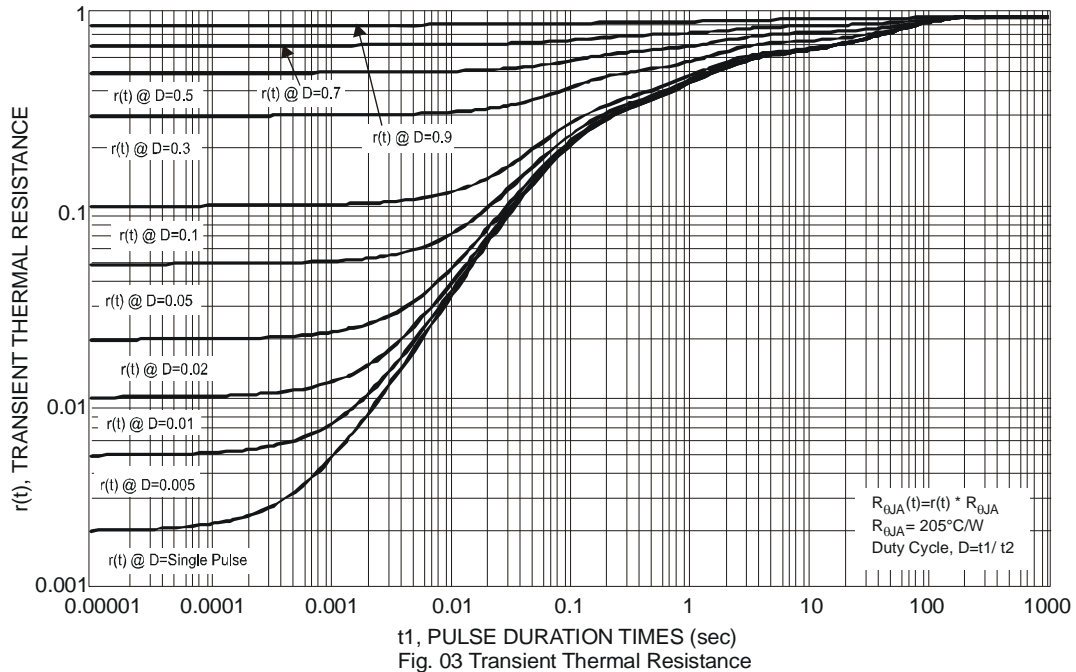


Fig. 2 SOA, Safe Operation Area



Electrical Characteristics @T_A = 25°C unless otherwise specified

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|----------------------|------|--------|-------|------|--|
| OFF CHARACTERISTICS (Note 6) | | | | | | |
| Drain-Source Breakdown Voltage | BV _{DSS} | -12 | — | — | V | V _{GS} = 0V, I _D = -250μA |
| Zero Gate Voltage Drain Current T _J = 25°C | I _{DSS} | — | — | -1 | μA | V _{DS} = -12.0V, V _{GS} = 0V |
| Gate-Source Leakage | I _{GSS} | — | — | ±10 | μA | V _{GS} = ±8.0V, V _{DS} = 0V |
| ON CHARACTERISTICS (Note 6) | | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | -0.3 | -0.6 | -0.95 | V | V _{DS} = V _{GS} , I _D = -250μA |
| Static Drain-Source On-Resistance | R _{DS (ON)} | — | 25 | 29 | mΩ | V _{GS} = -4.5V, I _D = -4A |
| | | — | 31 | 45 | | V _{GS} = -2.5V, I _D = -3.5A |
| | | — | 40 | 60 | | V _{GS} = -1.8V, I _D = -1A |
| | | — | 60 | 100 | | V _{GS} = -1.5V, I _D = -0.5A |
| Forward Transfer Admittance | Y _{fs} | 0.4 | 3 | - | S | V _{DS} = -5V, I _D = -2A |
| Diode Forward Voltage | V _{SD} | - | - | -1.0 | V | V _{GS} = 0V, I _D = -2A |
| DYNAMIC CHARACTERISTICS (Note 7) | | | | | | |
| Input Capacitance | C _{iSS} | - | 1357.4 | - | pF | V _{DS} = -10V, V _{GS} = 0V f = 1.0MHz |
| Output Capacitance | C _{oSS} | - | 499 | - | pF | |
| Reverse Transfer Capacitance | C _{rSS} | - | 273.6 | - | pF | |
| Gate Resistance | R _g | - | 14.26 | - | Ω | V _{DS} = 0V, V _{GS} = 0V, f = 1MHz |
| Total Gate Charge | Q _g | - | 16.1 | - | nC | V _{GS} = -4.5V I _D = -1A, V _{DS} = -10V |
| Gate-Source Charge | Q _{gs} | - | 26.1 | - | nC | |
| Gate-Drain Charge | Q _{gd} | - | 1.71 | - | nC | |
| Turn-On Delay Time | t _{D(on)} | - | 20.48 | - | ns | V _{GS} = -2.5V, V _{DS} = -10V I _D = -180mA, R _G = 2.0Ω, |
| Turn-On Rise Time | t _r | - | 15.2 | - | ns | |
| Turn-Off Delay Time | t _{D(off)} | - | 33.11 | - | ns | |
| Turn-Off Fall Time | t _f | - | 219.4 | - | ns | |
| Turn-Off Fall Time | t _f | - | 217.64 | - | ns | |

Notes: 6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

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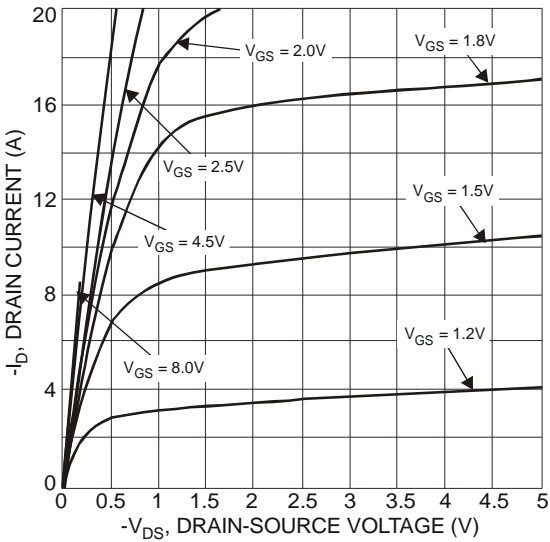


Fig. 4 Typical Output Characteristics

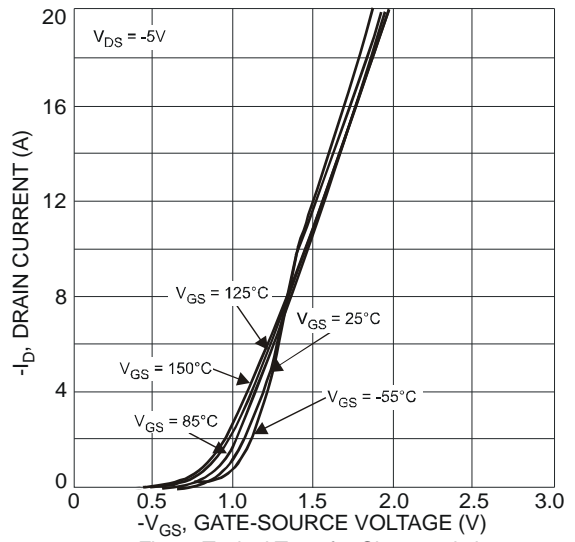


Fig. 5 Typical Transfer Characteristic

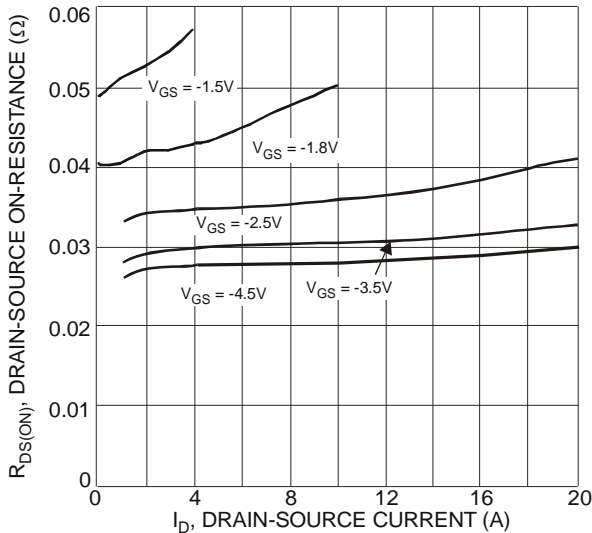


Fig. 6 Typical On-Resistance vs. Drain Current and Gate Voltage

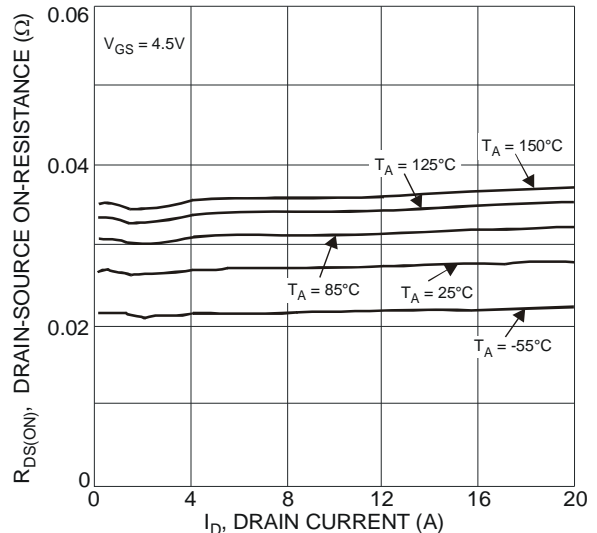


Fig. 7 Typical On-Resistance vs. Drain Current and Temperature

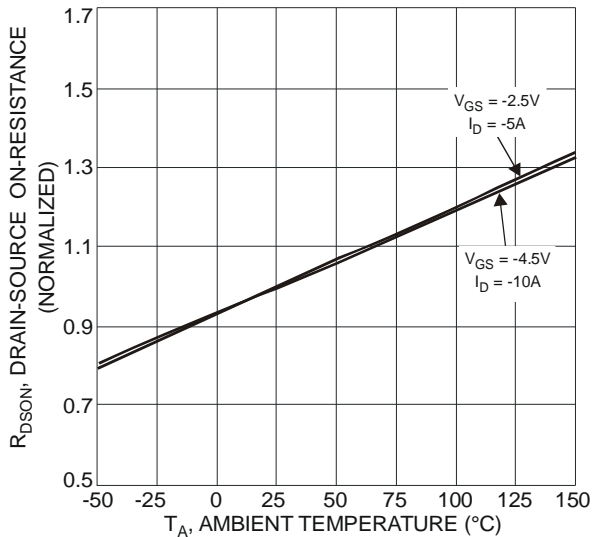


Fig. 8 On-Resistance Variation with Temperature

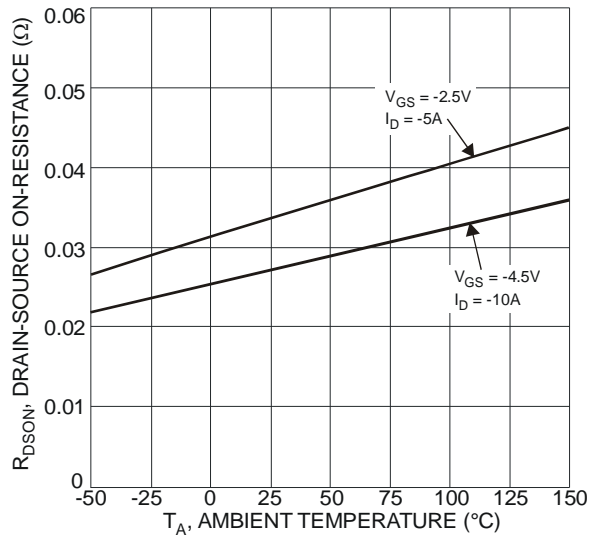


Fig. 9 On-Resistance Variation with Temperature

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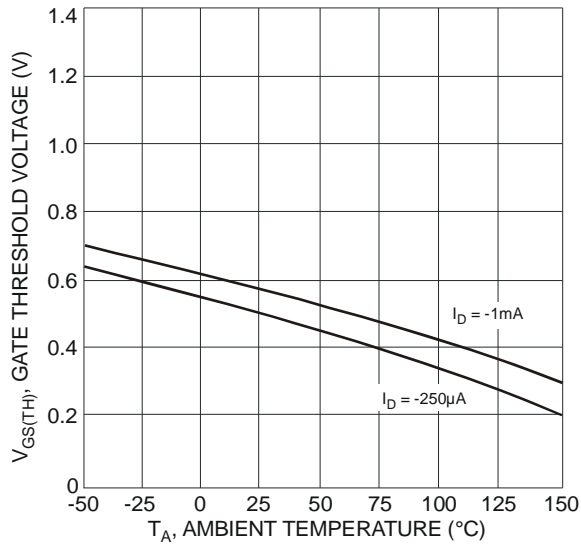


Fig. 10 Gate Threshold Variation vs. Ambient Temperature

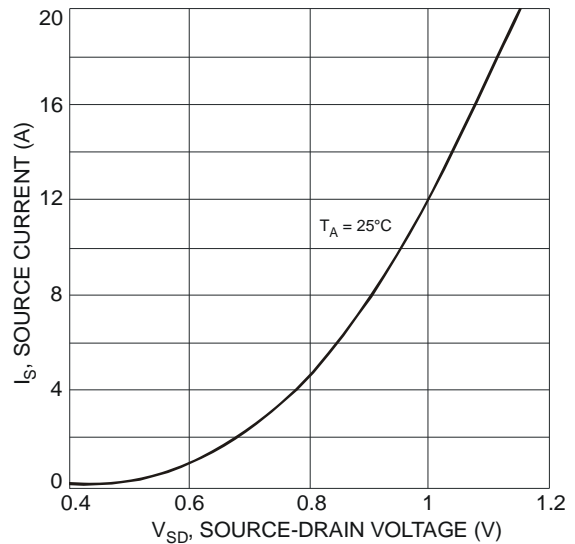


Fig. 11 Diode Forward Voltage vs. Current

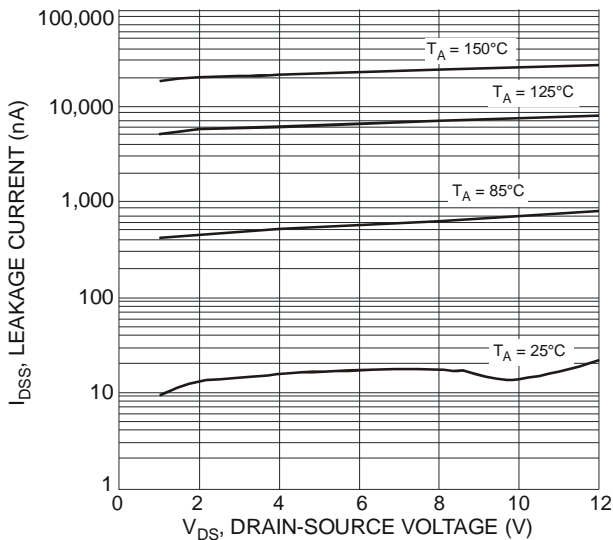


Fig. 12 Typical Drain-Source Leakage Current vs. Voltage

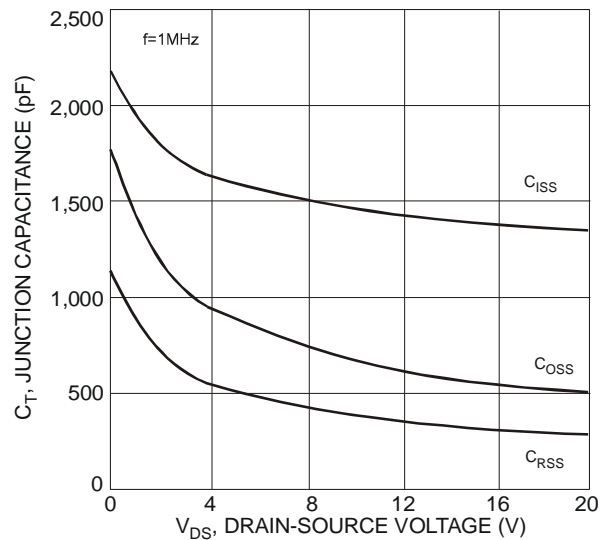


Fig. 13 Typical Junction Capacitance

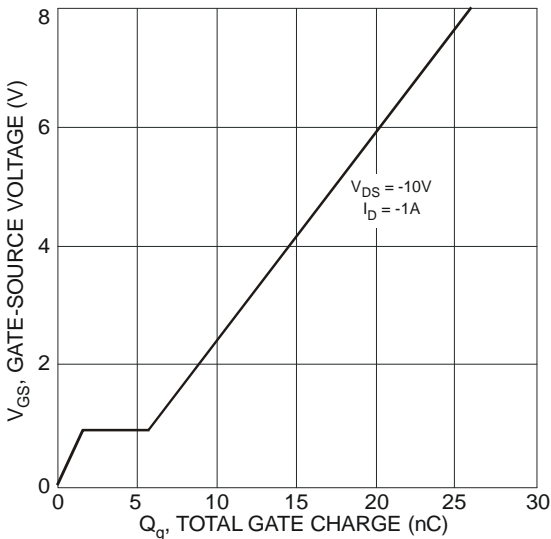
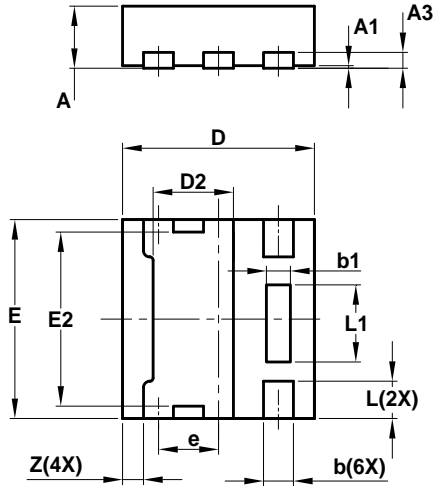


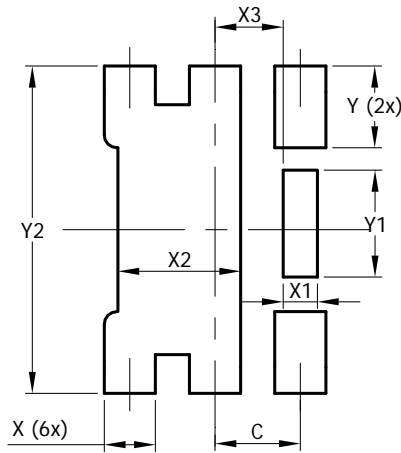
Fig. 14 Gate-Charge Characteristics

Package Outline Dimensions



| X1-DFN1616-6 Type E | | | |
|------------------------|------|------|-------|
| Dim | Min | Max | Typ |
| A | 0.47 | 0.53 | 0.50 |
| A1 | 0 | 0.05 | 0.02 |
| A3 | — | — | 0.13 |
| b | 0.20 | 0.30 | 0.25 |
| b1 | 0.10 | 0.30 | 0.20 |
| D | 1.55 | 1.65 | 1.60 |
| D2 | 0.57 | 0.77 | 0.67 |
| E | 1.55 | 1.65 | 1.60 |
| E2 | 1.30 | 1.50 | 1.40 |
| e | — | — | 0.50 |
| L | 0.25 | 0.35 | 0.30 |
| L1 | 0.52 | 0.72 | 0.62 |
| Z | — | — | 0.175 |
| All Dimensions in mm | | | |

Suggested Pad Layout



| Dimensions | Value (in mm) |
|------------|---------------|
| C | 0.500 |
| X | 0.300 |
| X1 | 0.200 |
| X2 | 0.720 |
| X3 | 0.400 |
| Y | 0.475 |
| Y1 | 0.620 |
| Y2 | 1.900 |

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