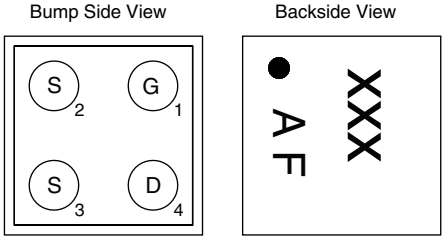
P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I_D (A)[a, e]	Q_g (Typ.)
- 20	0.076 at V_{GS} = - 4.5 V	- 2.9	7.5 nC
	0.100 at V_{GS} = - 2.5 V	- 2.5	
	0.145 at V_{GS} = - 1.8 V	- 2.1	
	0.320 at V_{GS} = - 1.5 V	- 0.5	

MICRO FOOT



Device Marking: A F
xxx = Date/Lot Traceability Code

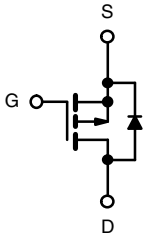
FEATURES

- TrenchFET® Power MOSFET
- Small 0.8 mm x 0.8 mm outline area
- Low 0.4 mm max. profile
- Material categorization:
  For definitions of compliance please see
  www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Load switches and chargers switches
- Battery management
- DC/DC converters
- For smart phones and tablet PCs



P-Channel MOSFET

Ordering Information: Si8817DB-T2-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	- 2.9[a]	A
	T_A = 70 °C		- 2.3[a]	
	T_A = 25 °C		- 2.1[b]	
	T_A = 70 °C		- 1.7[b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	- 15	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 0.7[a]	
	T_A = 25 °C		- 0.4[b]	
Maximum Power Dissipation	T_A = 25 °C	P_D	0.9[a]	W
	T_A = 70 °C		0.6[a]	
	T_A = 25 °C		0.5[b]	
	T_A = 70 °C		0.3[b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Package Reflow Conditions[c]	VPR		260	
	IR/Convection		260	

Notes:
a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on T_A = 25 °C.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a, b]	t = 5 s	R_{thJA}	105	135	°C/W
Maximum Junction-to-Ambient[c, d]	t = 5 s		200	260	

Notes:
a. Surface mounted on 1" x 1" FR4 board with full copper.
b. Maximum under steady state conditions is 185 °C/W.
c. Surface mounted on 1" x 1" FR4 board with minimum copper.
d. Maximum under steady state conditions is 330 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 12		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.4		- 1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 70 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 1 A		0.061	0.076	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.080	0.100	
		V_{GS} = - 1.8 V, I_D = - 0.5 A		0.110	0.145	
		V_{GS} = - 1.5 V, I_D = - 0.5 A		0.165	0.320	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 1 A		5		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		615		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}			75		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 8 V, I_D = - 1 A		12.5	19	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 1 A		7.5	12	
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			1.9		
Gate Resistance	R_g	V_{GS} = - 0.1 V, f = 1 MHz		14		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		20	40	ns
Rise Time	t_r			20	40	
Turn-Off Delay Time	$t_{d(off)}$			52	100	
Fall Time	t_f			22	45	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 10 Ω $I_D \cong$ - 1 A, V_{GEN} = - 8 V, R_g = 1 Ω		6	15	
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			60	120	
Fall Time	t_f			23	45	

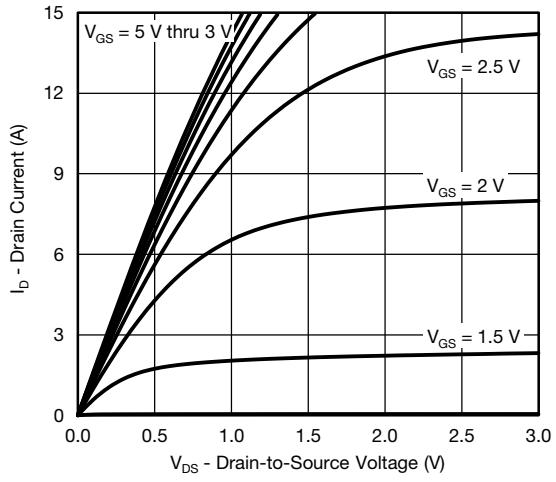
For technical questions, contact: pmostechsupport@vishay.com
Document Number: 62759
S12-1858-Rev. A, 06-Aug-12

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_A = 25 °C			- 0.7	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	I_S = - 1 A, V_{GS} = 0 V		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 1 A, dI/dt = 100 A/µs, T_J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	30	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			17		

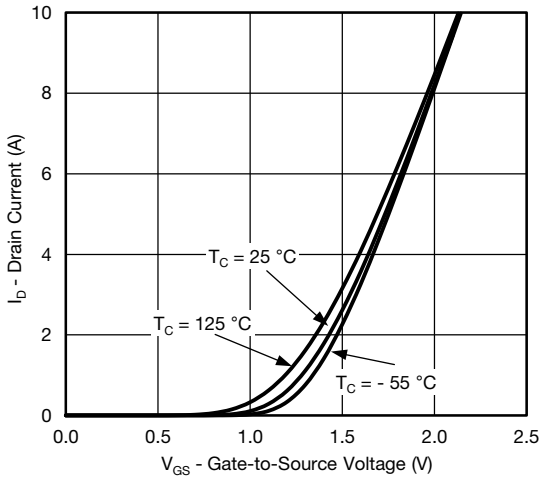
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

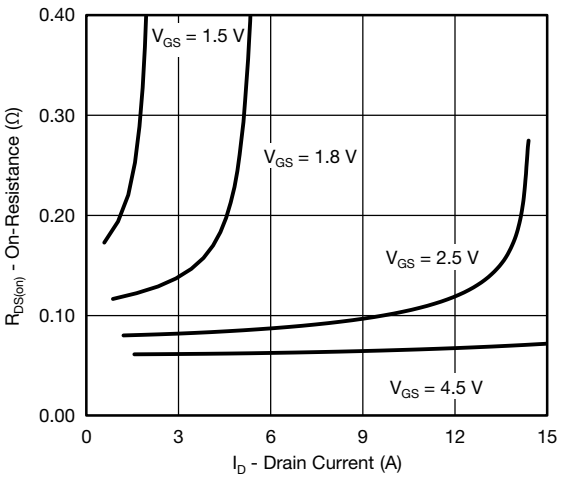
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



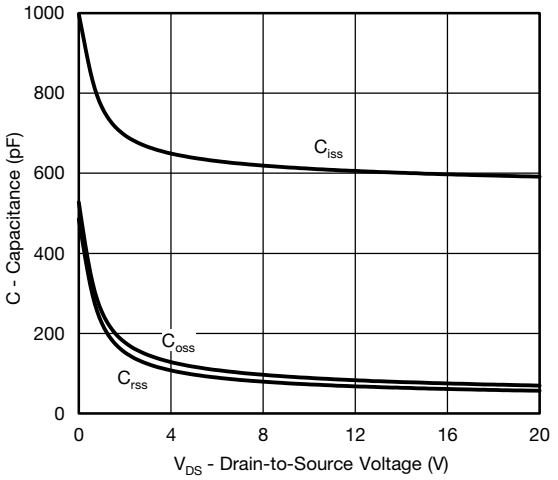
Output Characteristics



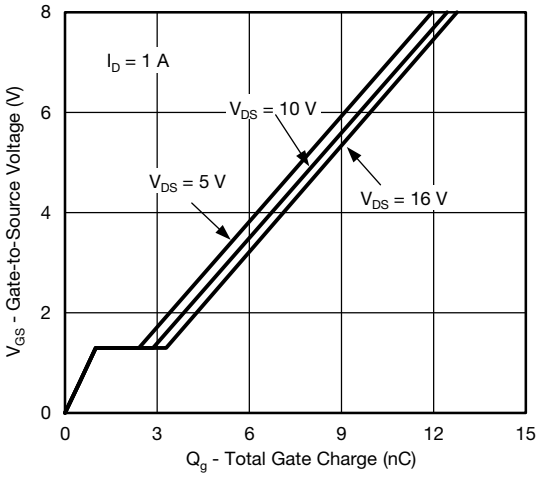
Transfer Characteristics



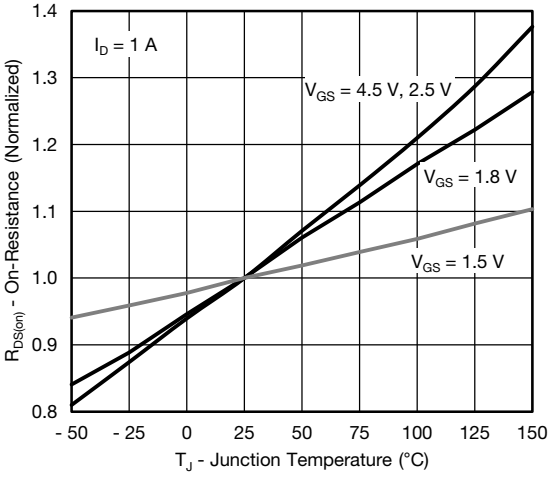
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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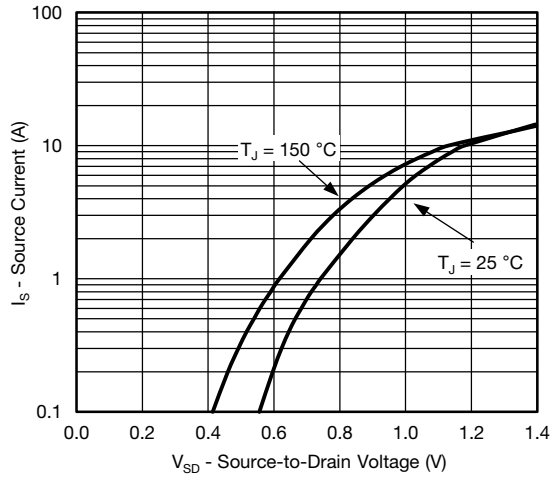
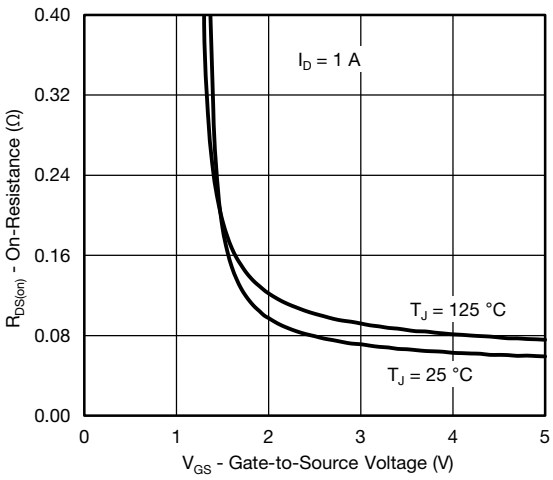
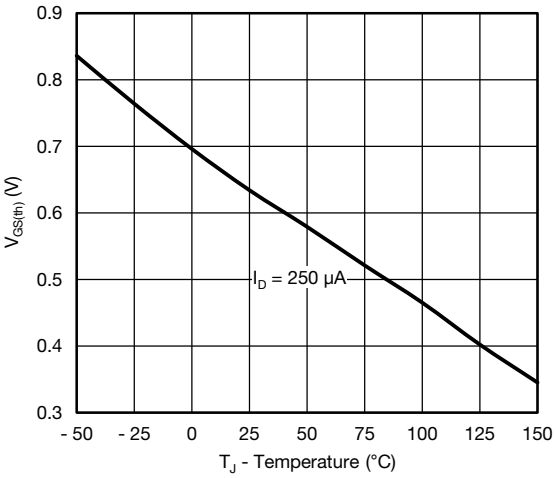
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



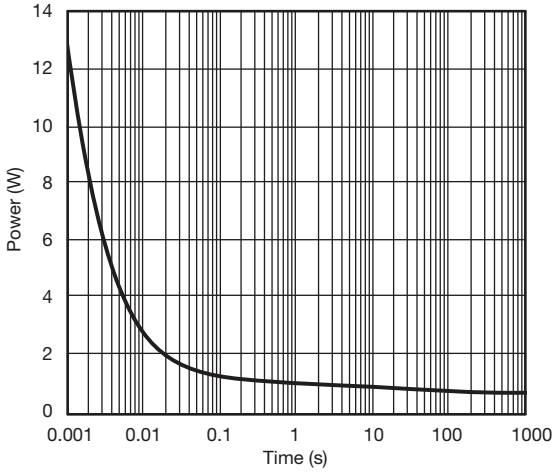
Source-Drain Diode Forward Voltage



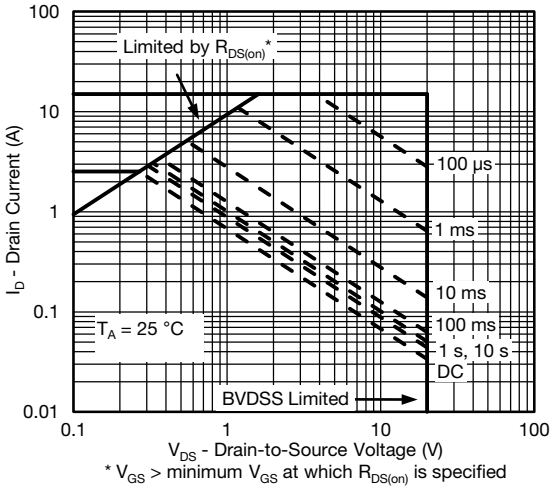
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

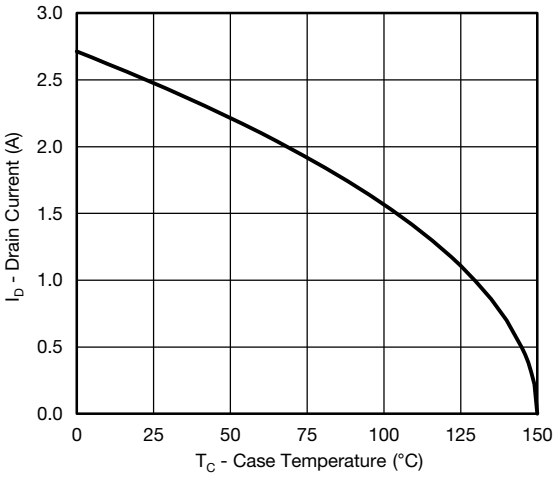


Single Pulse Power, Junction-to-Ambient

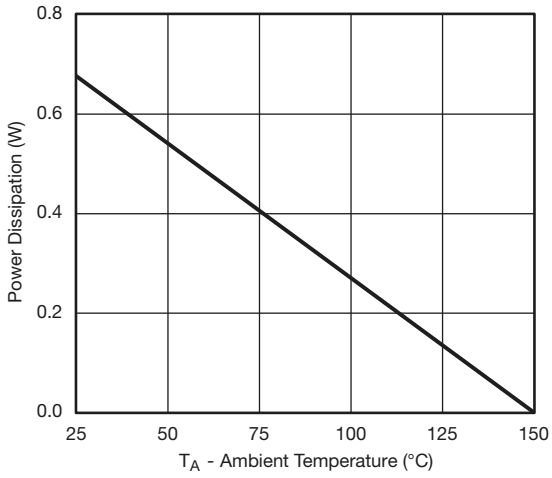


Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Derating

Note:
When mounted on 1" x 1" FR4 with full copper.

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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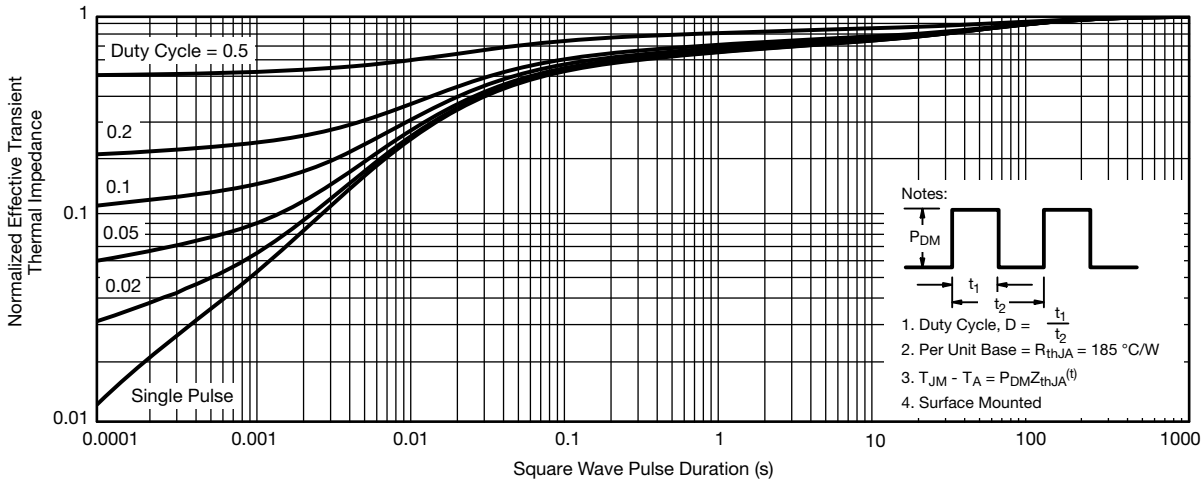
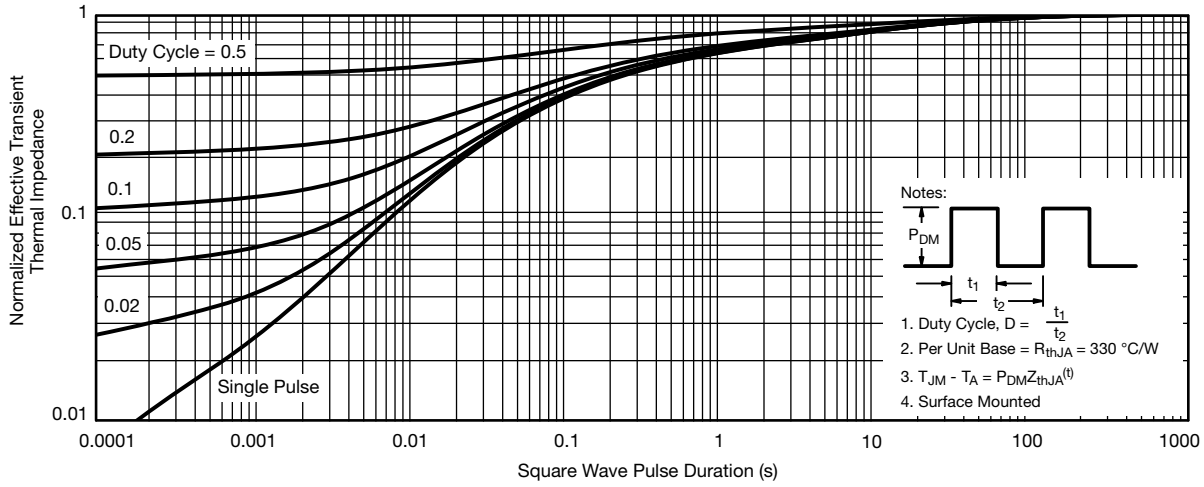


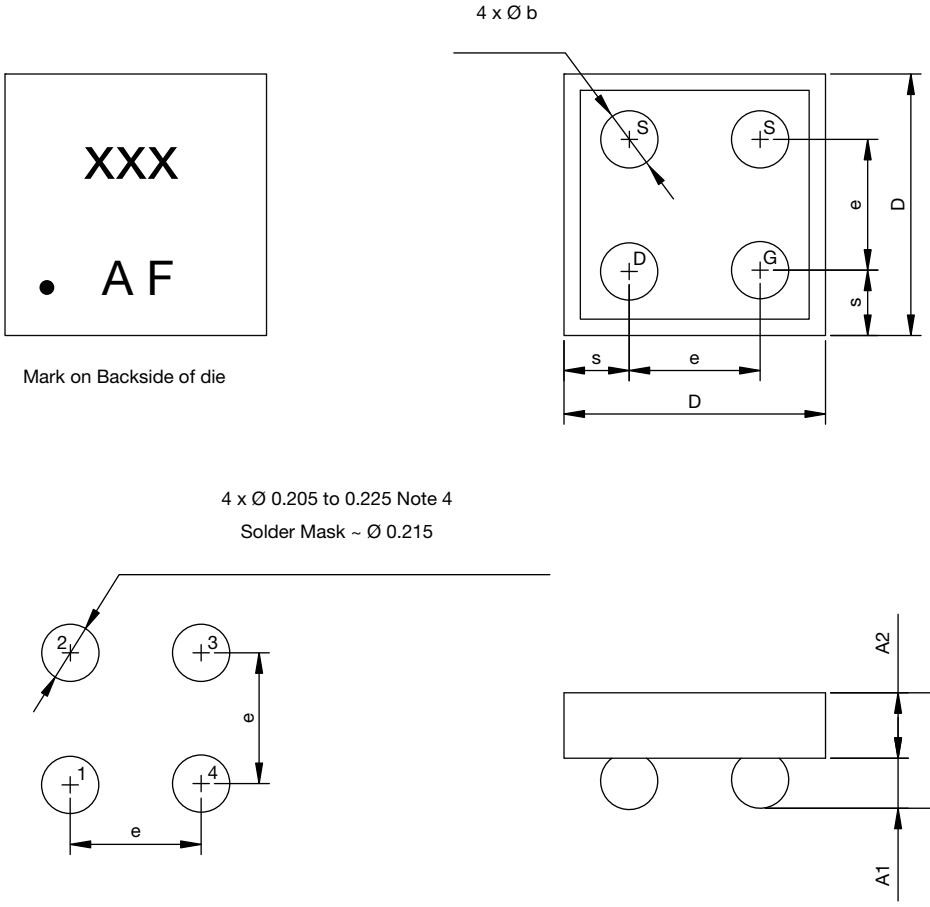
Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with maximum Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with minimum Copper)

PACKAGE OUTLINE

MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



Notes (Unless otherwise specified):
1. All dimensions are in millimeters.
2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.
3. Backside surface is coated with a Ti/Ni/Ag layer.
4. Non-solder mask defined copper landing pad.
5. • is location of pin 1.

Dim.	Millimeters[a]			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.314	0.357	0.400	0.0124	0.0141	0.0157
A_1	0.127	0.157	0.187	0.0050	0.0062	0.0074
A_2	0.187	0.200	0.213	0.0074	0.0079	0.0084
b	0.165	0.175	0.185	0.0064	0.0068	0.0072
e		0.400			0.0157	
s	0.180	0.200	0.220	0.0070	0.0078	0.0086
D	0.760	0.800	0.840	0.0299	0.0314	0.0330

Notes:
a. Use millimeters as the primary measurement.

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