

STW60NM50N

N-channel 500 V, 0.035 Ω 68 A, MDmesh™ II Power MOSFET in TO-247 package

Datasheet — preliminary data

Features

Туре	V _{DSS} (@Tjmax)	R _{DS(on)} max	I _D
STW60NM50N	550 V	<0.043 Ω	68 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh[™] technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

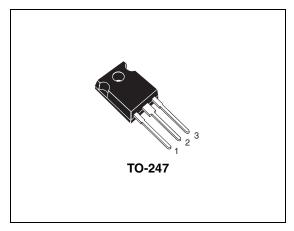


Figure 1. Internal schematic diagram

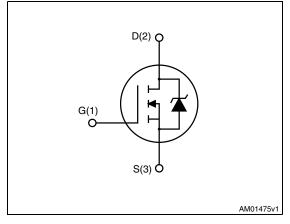


Table 1. Device summary

Order code	Marking	Package	Packaging
STW60NM50N	60NM50N	TO-247	Tube

Doc ID 023157 Rev 1

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This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Electrical ratings

	Table 2.	Absolute	maximum	ratings
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Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	±25	V
۱ _D	Drain current (continuous) at $T_C = 25 \ ^{\circ}C$	68	А
۱ _D	Drain current (continuous) at T _C = 100 °C	43	А
I _{DM} ⁽¹⁾	Drain current (pulsed)	272	А
P _{TOT}	Total dissipation at $T_C = 25 \ ^{\circ}C$	446	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15	V/ns
T _{stg}	Storage temperature	-55 to 150	°C
Тj	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 68$ A, di/dt ≤ 400 A/µs, V_{DD} =80% V_{(BR)DSS}

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	0.28	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	50	°C/W

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	14	A
E _{AS}	Single pulse avalanche energy (starting Tj=25 °C, I _D =I _{AS} , V _{DD} =50 V)	551	mJ



2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0$, $I_D = 1$ mA	500			v
I _{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 500 V$ $V_{GS} = 0, V_{DS} = 500 V, T_j = 125 °C$			1 100	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20 V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2	3	4	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 34 A		0.035	0.043	Ω

Table 5. On/off states

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 100 \text{ V}, \text{ f} = 1 \text{ MHz},$ $V_{GS} = 0$	-	5790 365 14	-	pF pF pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	$V_{GS} = 0V$, $V_{DS} = 0V$ to 480V	-	1008	-	pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}, \text{ I}_{D} = 68 \text{ A},$ $V_{GS} = 10 \text{ V}$ (see Figure 3)	-	178 28 95	-	nC nC nC
R _g	Gate input resistance	f=1 MHz gate DC bias=0 Test signal level = 20 mV open drain	-	2	-	Ω

1. $C_{oss eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7.	Switching times
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Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300 \text{ V}, I_D = 32.5 \text{ A}$ $R_G = 4.7 \Omega V_{GS} = 10 \text{ V}$ (see Figure 2)	-	206 36 40 27.5	-	ns ns ns ns



Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current Source-drain current (pulsed)		-		68 272	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 68 A, V _{GS} = 0			1.6	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 68 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$ $V_{DD} = 100 \text{ V}$ (see Figure 4)		476 10.5 44		ns nC A
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 68 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s}$ $V_{DD} = 100 \text{ V, } \text{T}_{j} = 150 \text{ °C}$ (see Figure 4)		586 15 51		ns nC A

Table 8.Source drain diode

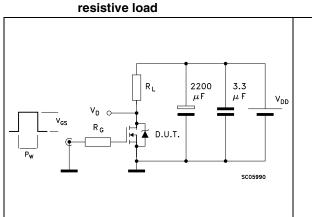
1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = $300 \ \mu$ s, duty cycle 1.5%



Figure 2.

3 Test circuits



Switching times test circuit for



Figure 3. Gate charge test circuit

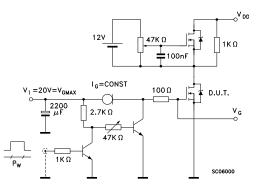
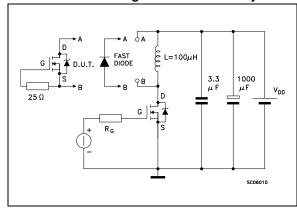
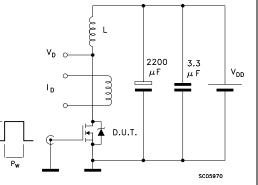


Figure 4. Test circuit for inductive load Figure 5. Unclamped Inductive load test switching and diode recovery times circuit







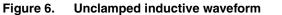
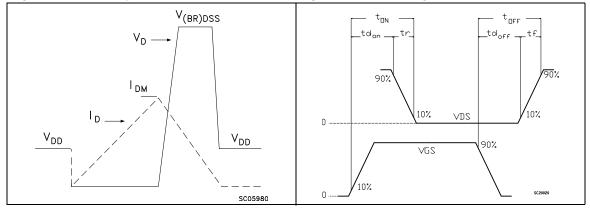


Figure 7. Switching time waveform





4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.

Dim	mm.		
Dim.	Min.	Тур.	Max.
А	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
С	0.40		0.80
D	19.85		20.15
Е	15.45		15.75
е	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Table 9. TO-247 mechanical data



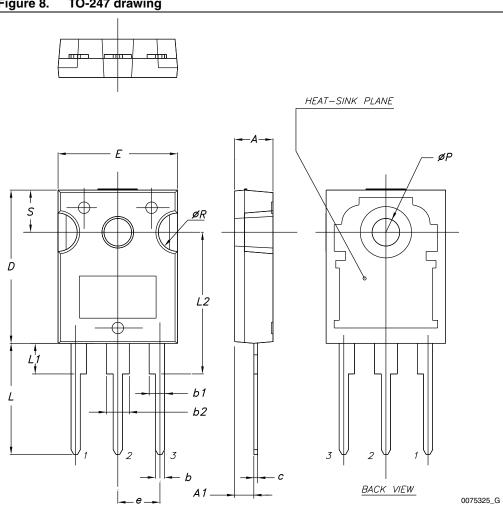


Figure 8. TO-247 drawing

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5 Revision history

Table 10. Document revision history

Date	Revision	Changes
26-Apr-2012	1	First release.



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