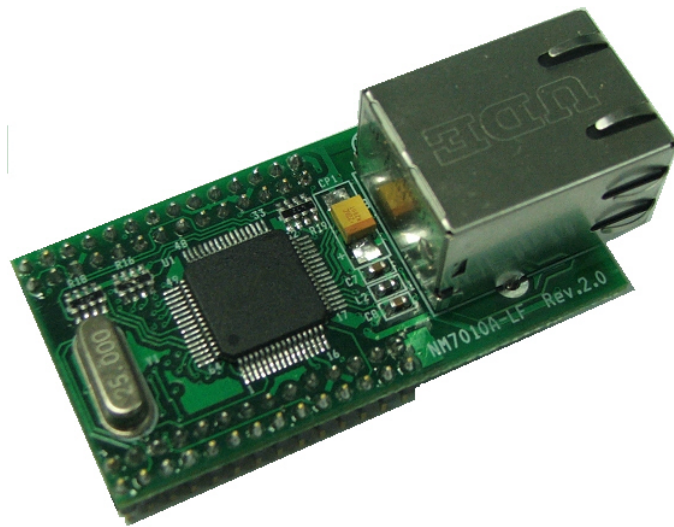


NM7010A-LF

(Ver. 2.6)



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Document History Information

Revision	Date	Description
V2.5	July 3, 2006	Revision Docs & NM7010A-LF Module - Datasheet, Part List, Schematics - NM7010A-LF 1.1 → NM7010A-LF 2.0 (Replace PHY & Mag-Jack Parts)
V2.6	July 24, 2007	Revision Docs & NM7010A-LF Module - Datasheet, PartList, Schematics - NM7010A-LF Rev.2.0 replace PHY and related parts



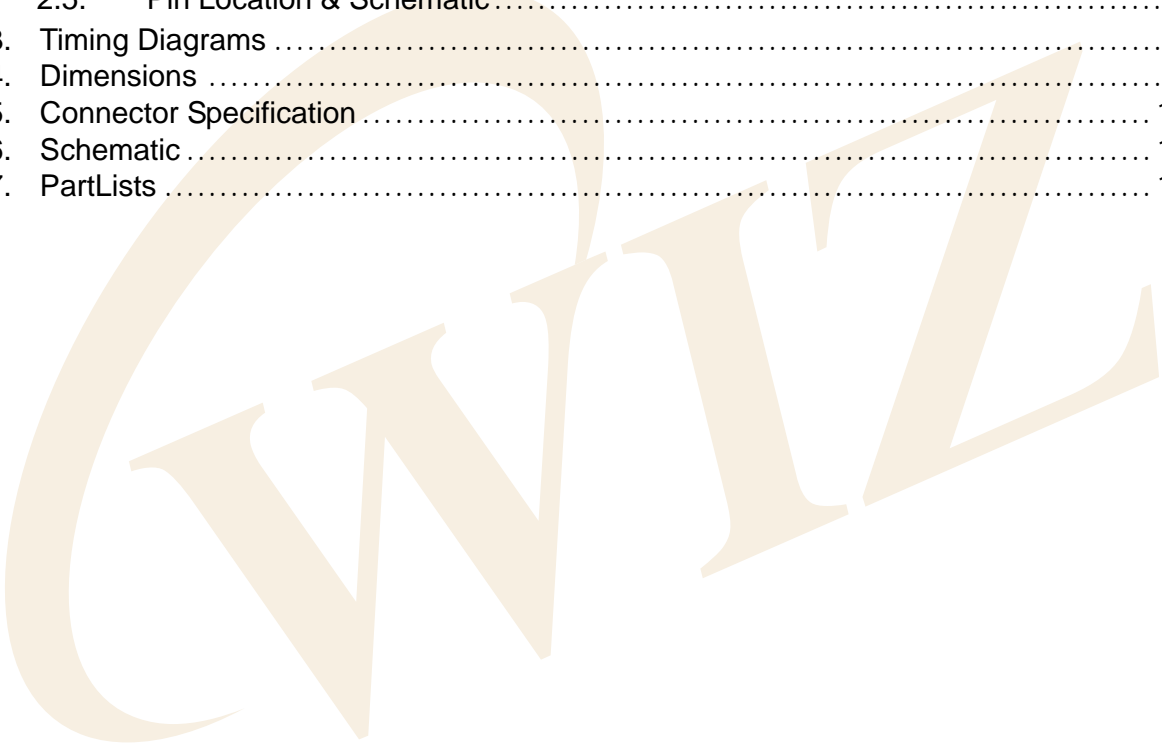
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If you have something to ask about WIZnet Products, Write down your question on Q&A Board of 'Support' menu in WIZnet website (www.wiznet.co.kr). WIZnet Engineer will give an answer as soon as possible.

The screenshot shows the WIZnet website interface. At the top, there is a navigation bar with links for Home, Sitemap, Contact us, and 한국어. Below this is a secondary menu with links for Products, Technology, Technical Q & A, Library, Where to buy, Value Chain, and About us. The main content area features a large banner for the W5100 chip, described as a '3 in 1' solution for embedded Internet, combining TCP/IP Core, MAG, and PHY. To the right, there is a 'New Products' section for the WIZ Series with W5100, specifically the Serial-to-Ethernet WIZ100SR. Below the banner, there are sections for 'Application Reference' and 'Solution Provider', each with a list of items and dates. A 'WIZnet News' section is also present. A large blue callout 'Click !!' with an arrow points to the 'Technical Support' link in the bottom right corner of the main content area. The footer contains the WIZnet logo, copyright information, and logos for NEC, AMTEL, and MICROCHIP.

Table of Contents

1. Introduction	4
1.1. Features	4
1.2. Block Diagram	4
2. Pin Assignments & descriptions	5
2.1. Power & Ground	5
2.2. MCU Interfaces	5
2.3. Network status & LEDs	6
2.4. Miscellaneous Signals	7
2.5. Pin Location & Schematic	8
3. Timing Diagrams	8
4. Dimensions	9
5. Connector Specification	10
6. Schematic	11
7. PartLists	13



1. Introduction

NM7010A-LF is the network module that includes W3100A-LF (TCP/IP hardwired chip), Ethernet PHY (**IP101A**), MAG-JACK (RJ45 with X'FMR) with other glue logics. It can be used as a component and no effort is required to interface W3100A-LF and PHY chip. The NM7010A-LF is an ideal option for users who want to develop their Internet enabling systems rapidly.

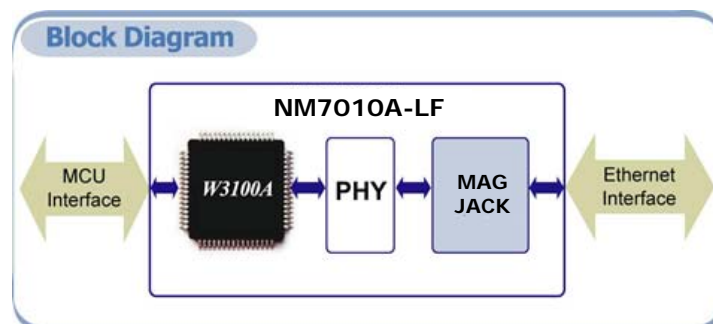
NM7010A-LF consists of W3100A-LF, Ethernet PHY and MAG-JACK.

- TCP/IP, MAC protocol layer: W3100A-LF
- Physical layer: Ethernet PHY(IP101A-LF LQFP48)
- Connector: MAG-JACK

1.1. Features

- Supports 10/100 Base TX half/full duplex operation
- Supports auto-negotiation, **Auto MDI/MDIX**
- IEEE 802.3/802.3u Complaints
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports Intel/Motorola MCU bus Interface and I²C Interface
- Supports Direct/Indirect mode bus access
- Supports clocked mode, non-clocked mode, external clocked mode
- Supports Socket API for easy application programming
- Interfaces with Two 2.0mm pitch 2 * 14 header pin

1.2. Block Diagram



/INT	O	JP1 : 2	Interrupt : Active low After reception or transmission it indicates that the W3100A-LF requires MCU attention. By writing values to the Interrupt Status Register of W3100A-LF the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W3100A-LF(Interrupt Mask Register). For more details refer to the W3100A-LF Datasheet
I_SCL	I	JP2 : 25	SCL : Used as clock by I ² C interface mode. Internally pull-down
I_SDA	I/O	JP2 : 26	SDA : Used as data by I ² C interface mode. Internally pull-down

2.3. Network status & LEDs

You can observe the network status using MAC-JACK LEDs. LED interface can be extended to the LED of the main board.

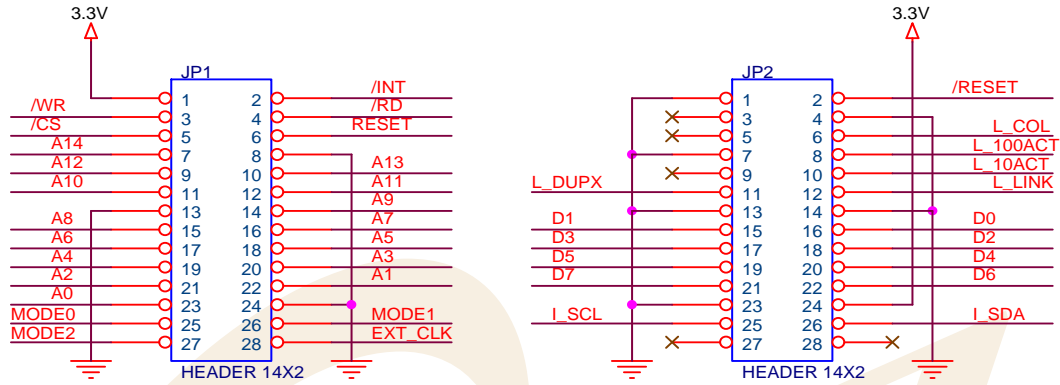
Symbol	Type	Pin No.	Description
L_COL	O	JP2 : 6	Collision LED : Active low when collisions occur.
L_100ACT	O	JP2 : 8	Link 100/ACT LED : Active low when linked by 100 Base TX, and blinking when transmitting or receiving data.
L_10ACT	O	JP2 : 10	Link 10/ACT LED : Active low when linked by 10 Base T, and blinking when transmitting or receiving data.
L_DUPX	O	JP2 : 11	Full Duplex LED : Active low when in full duplex operation. Active high when in half duplex operation.
L_LINK	O	JP2 : 12	Link LED : Active low when linked

2.4. Miscellaneous Signals

Symbol	Type	Pin No.	Description															
RESET	I	JP1 : 6	<p>Reset : Active high</p> <p>Initializes or Reinitializes the W3100A-LF. Asserting this pin will force a reset process to occur, which will result in all internal registers reinitializing to their default and all strapping options are reinitialized.</p> <p>For complete reset function, this pin must be asserted low for at least 10us. Refer to W3100A-LF datasheet for further detail regarding reset.</p>															
/RESET	I	JP2 : 2	<p>Reset : Active low</p> <p>Reset RTL8201BL chip. For complete reset function this pin must be asserted low for at least 10ms.</p>															
MODE1~0	I	JP1 : 26 , JP1 : 25	<p>Mode Select : These pins select MCU interface and operating mode. Since each pin is pull-down internally, clocked mode (the default mode) is selected when these pins are not connected.</p> <table border="1" data-bbox="901 1024 1339 1255"> <thead> <tr> <th>M1</th> <th>M0</th> <th>Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Clocked</td> </tr> <tr> <td>0</td> <td>1</td> <td>External clocked</td> </tr> <tr> <td>1</td> <td>0</td> <td>Non-clocked</td> </tr> <tr> <td>1</td> <td>1</td> <td>I²C interface</td> </tr> </tbody> </table> <p>Refer to W3100A-LF datasheet for further detail regarding mode select</p>	M1	M0	Mode	0	0	Clocked	0	1	External clocked	1	0	Non-clocked	1	1	I ² C interface
M1	M0	Mode																
0	0	Clocked																
0	1	External clocked																
1	0	Non-clocked																
1	1	I ² C interface																
EXT_CLK	I	JP1 : 28	<p>External clock : supplementary clock used for external clocked mode.</p> <p>In external clocked mode, W3100A-LF uses this clock to interface with MCU.</p> <p>Refer to W3100A-LF datasheet for further detail regarding external clock.</p>															
NC	-	JP1 : 27, JP2 : 3 JP2 : 5, JP2 : 9 JP2 : 27, JP2 : 28	Not Connect															

2.5. Pin Location & Schematic

Refer to "Chapter 4. Dimension".



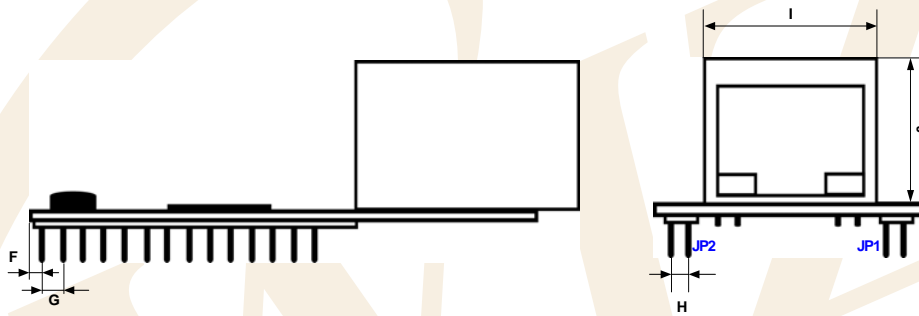
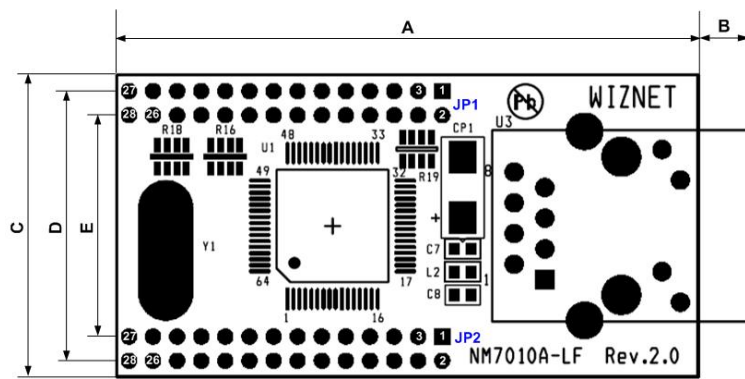
3. Timing Diagrams

NM7010A-LF provides following interfaces of W3100A-LF

- Direct/Indirect mode bus access
- I²C Interface
- Clocked mode, Non-Clocked mode, External clocked mode

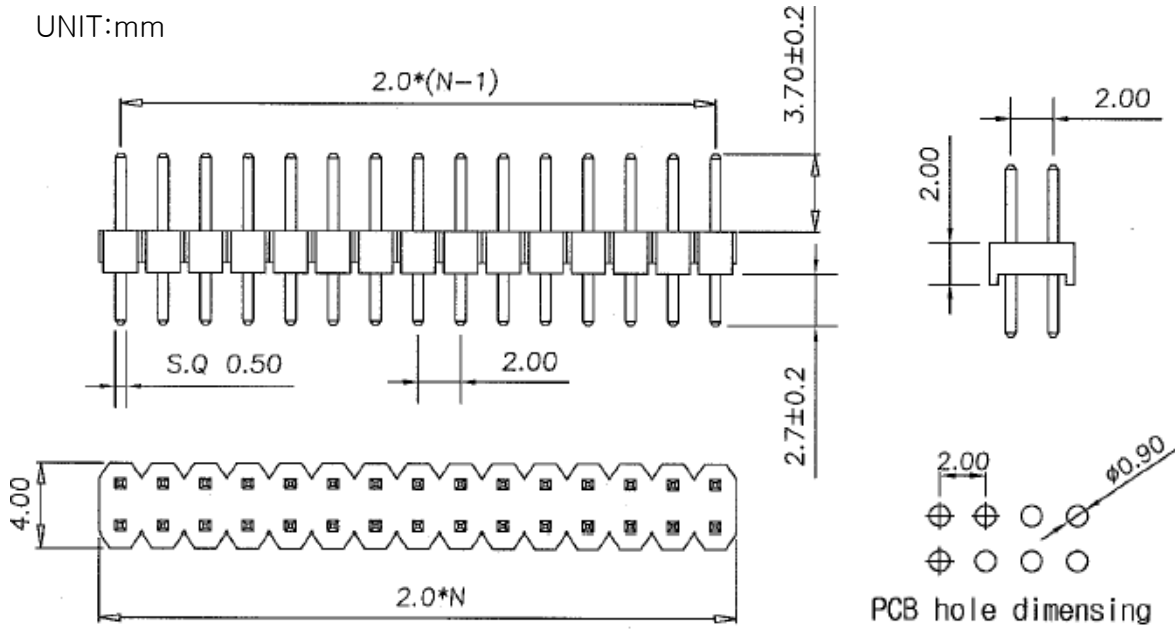
Refer to W3100A-LF datasheet for timing of NM7010A-LF

4. Dimensions

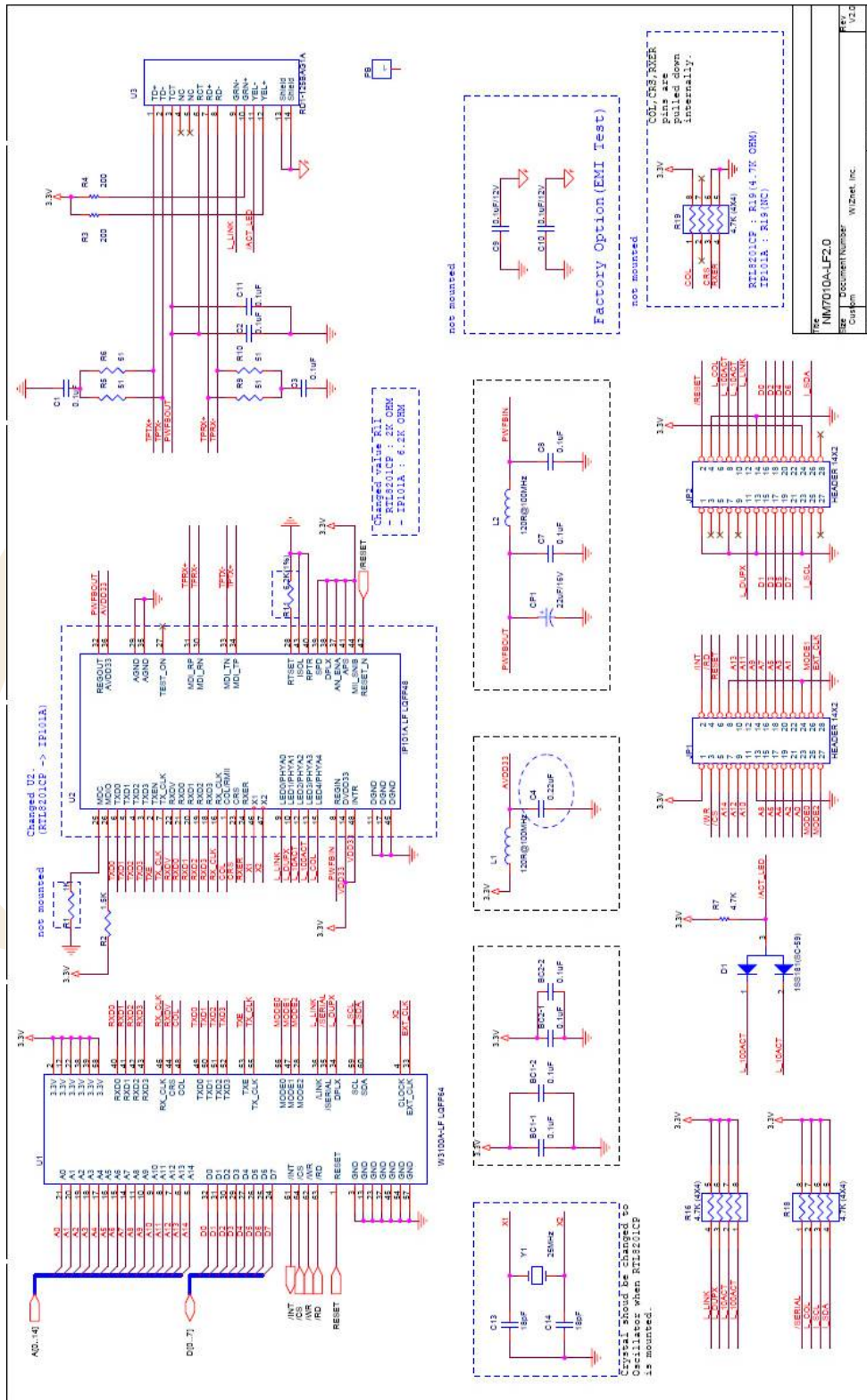


Symbols	Dimensions (mm)
A	48.0
B	4.0
C	25.0
D	22.4
E	18.4
F	1.0
G	2.0
H	2.0
I	16.0
J	13.4

5. Connector Specification



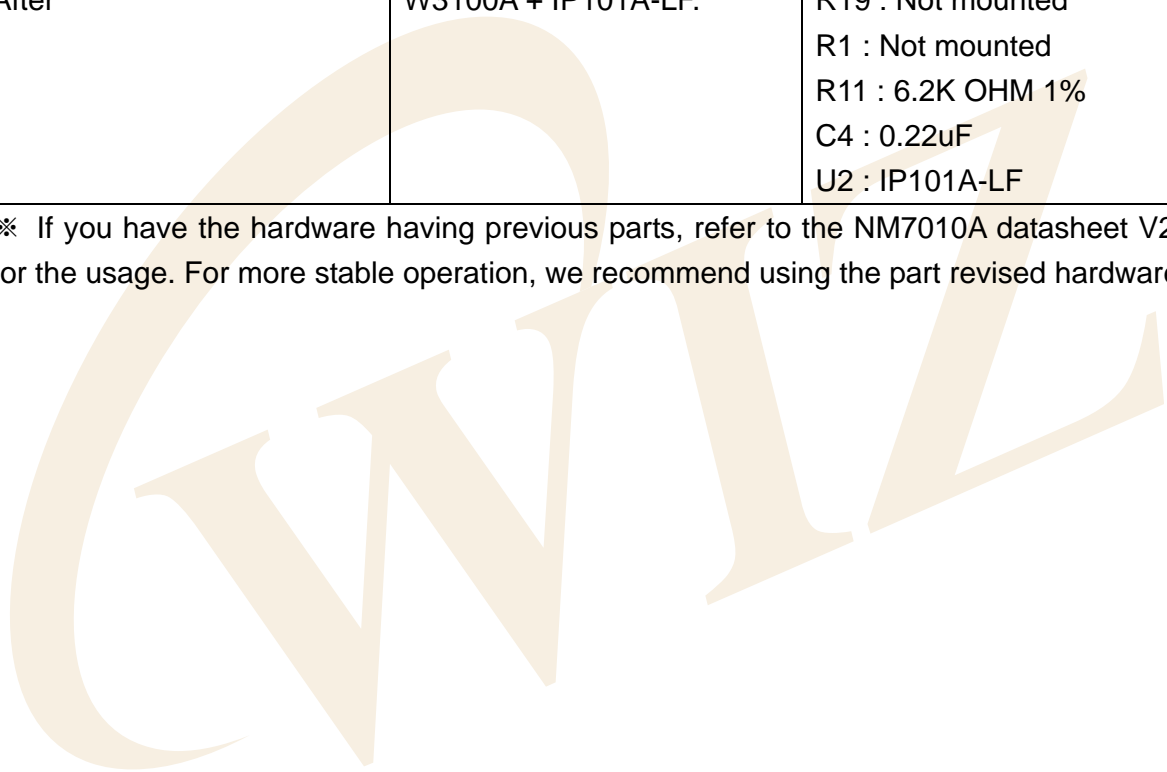
6. Schematic



[Schematic History (NM7010A-LF REV.2.0)]

	Description	Parts
Before	W3100A + RTL8201CP	R19 : 4.7K OHM ARRAY R1 : 1K OHM R11 : 2K OHM 1% C4 : 0.1uF U2 : RTL8201CP
After	W3100A + IP101A-LF.	R19 : Not mounted R1 : Not mounted R11 : 6.2K OHM 1% C4 : 0.22uF U2 : IP101A-LF

※ If you have the hardware having previous parts, refer to the NM7010A datasheet V2.5 for the usage. For more stable operation, we recommend using the part revised hardware.



7. PartLists

Item	Q.ty	Reference	Part	Tech. Characteristics	Package
1	10	C1,C2,C3,C7,C8, C11,BC1-1,BC1-2, BC2-1,BC2-2	0.1uF	50V-20% Ceramic	CASE 0603
2	1	C4	0.22uF	50V-20% Ceramic	CASE 0603
3	1	CP1	22uF	16Vmin 10%	EIA/IECQ 3528
4	2	C13,C14	18pF	50V-20% Ceramic	CASE 0603
5	0	C9,C10	0.1uF	NOT MOUNTED	
6	1	D1	1SS181 Switching Diode		SC-59
7	2	JP1,JP2	2X14 28PIN 2mm DIP STRAIGHT Header	2 X 14 2mm pitch	
8	2	L1,L2	120R Chip Ferrite Bead	120R@100MHz 300mA	CASE 0603
9	0	R1	1K	NOT MOUNTED	
10	1	R2	1.5K	1/10W-5% SMD	CASE 0603
11	2	R3,R4	200	1/10W-5% SMD	CASE 0603
12	4	R5,R6,R9,R10	51 1%	1/10W-1% SMD	CASE 0603
13	1	R7	4.7K	1/10W-5% SMD	CASE 0603
14	1	R11	6.2K 1%	1/10W-1% SMD	CASE 0603
15	2	R16,R18	4.7K Chip Array(0603 X 4)	50V-5% SMD Chip-Array	CASE 1206
16	0	R19	4.7K Chip Array(0603 X 4)	NOT MOUNTED	
17	1	U1	W3100A-LF		LQFP64
18	1	U2	IP101A-LF		LQFP48
19	1	U3	RD1-125BAG1A	Transformer + RJ45	
20	1	Y1	25MHz Crystal	Holder Type, CL=18pF	ATS-25U
21	1		NM7010A-LF REV2.0 FR4 1.6T 4LAYER	PRINTED CIRCUIT BOARD	