



Low-Power, SC70/SOT μ P Reset Circuits with Capacitor-Adjustable Reset Timeout Delay

General Description

The MAX6340/MAX6421–MAX6426 low-power micro-processor supervisor circuits monitor system voltages from 1.6V to 5V. These devices perform a single function: they assert a reset signal whenever the V_{CC} supply voltage falls below its reset threshold. The reset output remains asserted for the reset timeout period after V_{CC} rises above the reset threshold. The reset timeout is externally set by a capacitor to provide more flexibility.

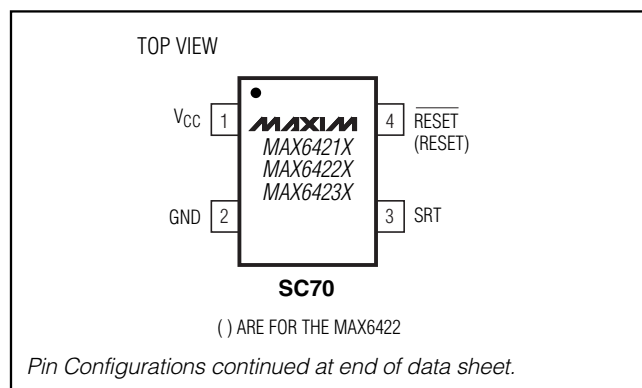
The MAX6421/MAX6424 have an active-low, push-pull reset output. The MAX6422 has an active-high, push-pull reset output and the MAX6340/MAX6423/MAX6425/MAX6426 have an active-low, open-drain reset output. The MAX6421/MAX6422/MAX6423 are offered in 4-pin SC70 or SOT143 packages. The MAX6340/MAX6424/MAX6425/MAX6426 are available in 5-pin SOT23-5 packages.

Applications

Portable Equipment
Battery-Powered Computers/Controllers
Automotive
Medical Equipment
Intelligent Instruments
Embedded Controllers
Critical μ P Monitoring
Set-Top Boxes
Computers

Typical Operating Circuit appears at end of data sheet.

Pin Configurations



Features

- ◆ Monitor System Voltages from 1.6V to 5V
- ◆ Capacitor-Adjustable Reset Timeout Period
- ◆ Low Quiescent Current (1.6 μ A typ)
- ◆ Three RESET Output Options
 - Push-Pull $\overline{\text{RESET}}$
 - Push-Pull RESET
 - Open-Drain RESET
- ◆ Guaranteed Reset Valid to $V_{CC} = 1V$
- ◆ Immune to Short V_{CC} Transients
- ◆ Small 4-Pin SC70, 4-Pin SOT143, and 5-Pin SOT23 Packages
- ◆ MAX6340 Pin Compatible with LP3470
- ◆ MAX6424/MAX6425 Pin Compatible with NCP300–NCP303, MC33464/MC33465, S807/S808/S809, and RN5VD
- ◆ MAX6426 Pin Compatible with PST92XX

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|----------------|-----------------|-------------|
| MAX6340UK_ _-T | -40°C to +125°C | 5 SOT23-5 |
| MAX6421XS_ _-T | -40°C to +125°C | 4 SC70-4 |
| MAX6421US_ _-T | -40°C to +125°C | 4 SOT143-4 |
| MAX6422XS_ _-T | -40°C to +125°C | 4 SC70-4 |
| MAX6422US_ _-T | -40°C to +125°C | 4 SOT143-4 |
| MAX6423XS_ _-T | -40°C to +125°C | 4 SC70-4 |
| MAX6423US_ _-T | -40°C to +125°C | 4 SOT143-4 |
| MAX6424UK_ _-T | -40°C to +125°C | 5 SOT23-5 |
| MAX6425UK_ _-T | -40°C to +125°C | 5 SOT23-5 |
| MAX6426UK_ _-T | -40°C to +125°C | 5 SOT23-5 |

Note: The MAX6340/MAX6421–MAX6426 are available with factory-trimmed reset thresholds from 1.575V to 5.0V in approximately 0.1V increments. Insert the desired nominal reset threshold suffix (from Table 1) into the blanks. There are 50 standard versions with a required order increment of 2500 pieces. Sample stock is generally held on standard versions only (see Standard Versions Table). Required order increment is 10,000 pieces for nonstandard versions. Contact factory for availability. All devices are available in tape-and-reel only.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

Selector Guide appears at end of data sheet.



Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX6340/MAX6421–MAX6426

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ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND

| | |
|--|------------------------------|
| V_{CC} | -0.3V to +6.0V |
| SRT, $\overline{\text{RESET}}$, RESET (push-pull) | -0.3V to ($V_{CC} + 0.3$)V |
| RESET (open drain) | -0.3V to +6.0V |
| Input Current (all pins) | ± 20 mA |
| Output Current (RESET, RESET) | ± 20 mA |

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

| | |
|---|---|
| 4-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) | 245mW |
| 4-Pin SOT143 (derate 4mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) | 320mW |
| 5-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) | 571mW |
| Operating Temperature Range | -40°C to $+125^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature | $+150^\circ\text{C}$ |
| Lead Temperature (soldering, 10s) | $+300^\circ\text{C}$ |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{CC} = 1\text{V}$ to 5.5V , $T_A = T_{\text{MIN}}$ to T_{MAX} , unless otherwise specified. Typical values are at $V_{CC} = 5\text{V}$ and $T_A = +25^\circ\text{C}$.) (Note 1)

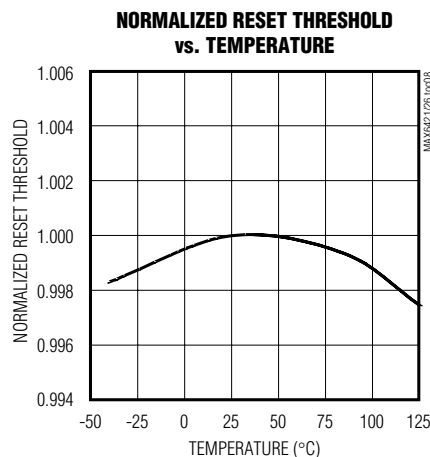
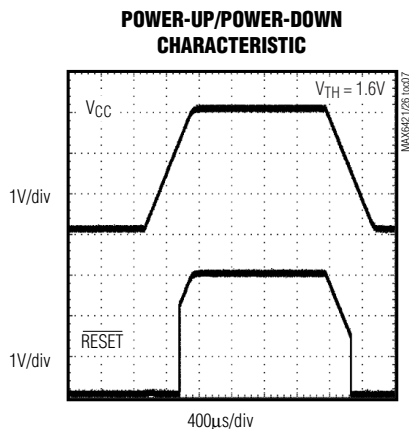
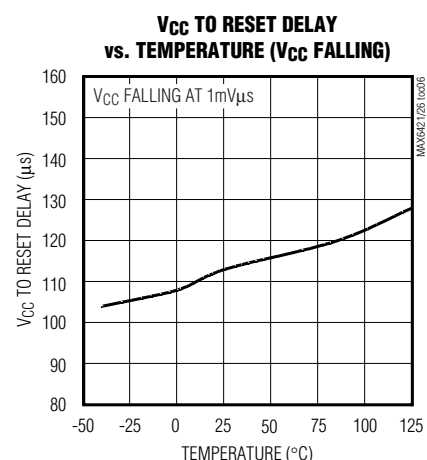
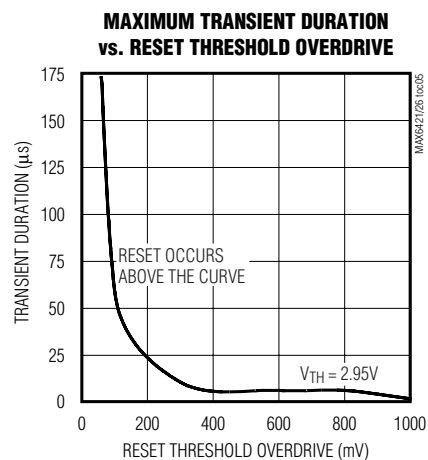
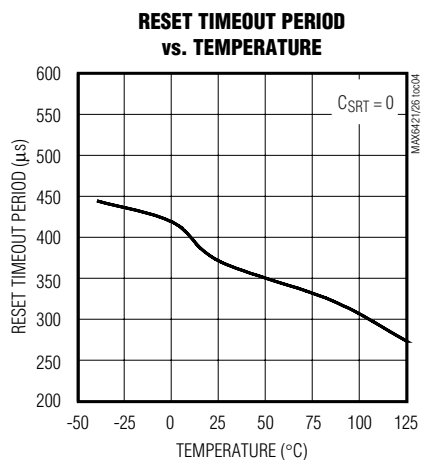
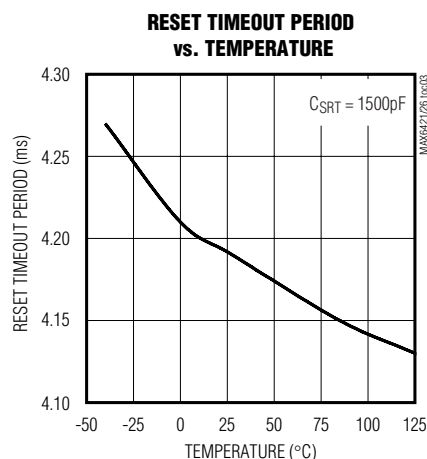
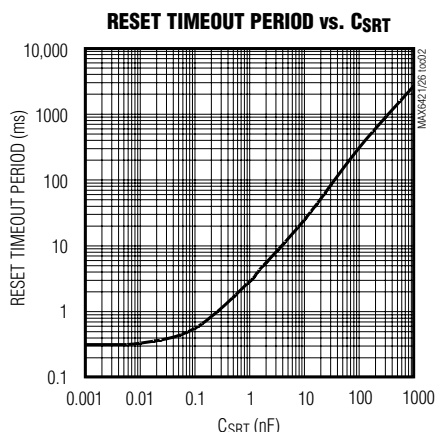
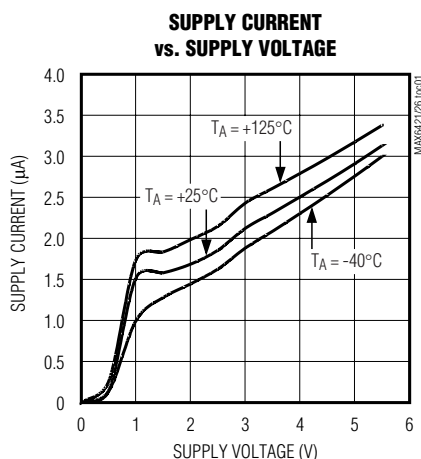
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------|---|---------------------|-------------------|------|---------------|
| Supply Voltage Range | V_{CC} | | 1.0 | | 5.5 | V |
| Supply Current | I_{CC} | $V_{CC} \leq 5.0\text{V}$ | | 2.5 | 4.2 | μA |
| | | $V_{CC} \leq 3.3\text{V}$ | | 1.9 | 3.4 | |
| | | $V_{CC} \leq 2.0\text{V}$ | | 1.6 | 2.5 | |
| V_{CC} Reset Threshold Accuracy | V_{TH} | $T_A = +25^\circ\text{C}$ | $V_{TH} - 1.5\%$ | $V_{TH} + 1.5\%$ | | V |
| | | $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ | $V_{TH} - 2.5\%$ | $V_{TH} + 2.5\%$ | | |
| Hysteresis | V_{HYST} | | | $4 \times V_{TH}$ | | mV |
| V_{CC} to Reset Delay | t_{RD} | V_{CC} falling at $1\text{mV}/\mu\text{s}$ | | 80 | | μs |
| Reset Timeout Period | t_{RP} | $CSRT = 1500\text{pF}$ | 3.00 | 4.375 | 5.75 | ms |
| | | $CSRT = 0$ | | 0.275 | | |
| V_{SRT} Ramp Current | I_{RAMP} | $V_{SRT} = 0$ to 0.65V ; $V_{CC} = 1.6\text{V}$ to 5V | | 240 | | nA |
| V_{SRT} Ramp Threshold | $V_{TH-RAMP}$ | $V_{CC} = 1.6\text{V}$ to 5V (V_{RAMP} rising) | | 0.65 | | V |
| RAMP Threshold Hysteresis | | V_{RAMP} falling threshold | | 33 | | mV |
| $\overline{\text{RESET}}$ Output Voltage Low | V_{OL} | $V_{CC} \geq 1.0\text{V}$, $I_{SINK} = 50\mu\text{A}$ | | | 0.3 | V |
| | | $V_{CC} \geq 2.7\text{V}$, $I_{SINK} = 1.2\text{mA}$ | | | 0.3 | |
| | | $V_{CC} \geq 4.5\text{V}$, $I_{SINK} = 3.2\text{mA}$ | | | 0.4 | |
| $\overline{\text{RESET}}$ Output Voltage High, Push-Pull | V_{OH} | $V_{CC} \geq 1.8\text{V}$, $I_{SOURCE} = 200\mu\text{A}$ | $0.8 \times V_{CC}$ | | | V |
| | | $V_{CC} \geq 2.25\text{V}$, $I_{SOURCE} = 500\mu\text{A}$ | $0.8 \times V_{CC}$ | | | |
| | | $V_{CC} \geq 4.5\text{V}$, $I_{SOURCE} = 800\mu\text{A}$ | $0.8 \times V_{CC}$ | | | |
| $\overline{\text{RESET}}$ Output Leakage Current, Open-Drain | I_{LKG} | $V_{CC} > V_{TH}$, reset not asserted | | | 1.0 | μA |
| RESET Output Voltage High | V_{OH} | $V_{CC} \geq 1.0\text{V}$, $I_{SOURCE} = 1\mu\text{A}$ | $0.8 \times V_{CC}$ | | | V |
| | | $V_{CC} \geq 1.8\text{V}$, $I_{SOURCE} = 150\mu\text{A}$ | $0.8 \times V_{CC}$ | | | |
| | | $V_{CC} \geq 2.7\text{V}$, $I_{SOURCE} = 500\mu\text{A}$ | $0.8 \times V_{CC}$ | | | |
| | | $V_{CC} \geq 4.5\text{V}$, $I_{SOURCE} = 800\mu\text{A}$ | $0.8 \times V_{CC}$ | | | |
| RESET Output Voltage Low | V_{OL} | $V_{CC} \geq 1.8\text{V}$, $I_{SINK} = 500\mu\text{A}$ | | | 0.3 | V |
| | | $V_{CC} \geq 2.7\text{V}$, $I_{SINK} = 1.2\text{mA}$ | | | 0.3 | |
| | | $V_{CC} \geq 4.5\text{V}$, $I_{SINK} = 3.2\text{mA}$ | | | 0.4 | |

Note 1: Devices production tested at $+25^\circ\text{C}$. Overtemperature limits are guaranteed by design.

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Typical Operating Characteristics

($V_{CC} = 5V$, $C_{SRT} = 1500pF$, $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description

| PIN | | | | | NAME | FUNCTION |
|---------|-------------------------------|--------------------|---------|-------|---------------------------|---|
| MAX6340 | MAX6421 MAX6422 MAX6423 | MAX6424 MAX6425 | MAX6426 | | | |
| SOT23 | SOT143 | SC70 | SOT23 | SOT23 | | |
| 1 | 3 | 3 | 5 | 1 | SRT | Set Reset Timeout Input. Connect a capacitor between SRT and ground to set the timeout period. Determine the period as follows: $t_{RP} = 2.73 \times 10^6 \times C_{SRT} + 275\mu s$ with t_{RP} in seconds and C_{SRT} in farads. |
| 2 | 1 | 2 | 3 | 2, 3 | GND | Ground |
| 3 | — | — | 4 | — | N.C. | Not Internally Connected. Can be connected to GND. |
| 4 | 2 | 1 | 2 | 5 | V _{CC} | Supply Voltage and Reset Threshold Monitor Input |
| 5 | 4 | 4 | 1 | 4 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ changes from high to low whenever V _{CC} drops below the selected reset threshold voltage. $\overline{\text{RESET}}$ remains low for the reset timeout period after V _{CC} exceeds the reset threshold. |
| — | | | — | — | RESET | RESET changes from low to high whenever V _{CC} drops below the selected reset threshold voltage. RESET remains high for the reset timeout period after V _{CC} exceeds the reset threshold. |

Detailed Description

Reset Output

The reset output is typically connected to the reset input of a μ P. A μ P's reset input starts or restarts the μ P in a known state. The MAX6340/MAX6421-MAX6426 μ P supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see *Typical Operating Characteristics*).

$\overline{\text{RESET}}$ changes from high to low whenever V_{CC} drops below the threshold voltage. Once V_{CC} exceeds the threshold voltage, $\overline{\text{RESET}}$ remains low for the capacitor-adjustable reset timeout period.

The MAX6422 active-high RESET output is the inverse logic of the active-low $\overline{\text{RESET}}$ output. All device outputs are guaranteed valid for V_{CC} > 1V.

The MAX6340/MAX6423/MAX6425/MAX6426 are open-drain $\overline{\text{RESET}}$ outputs. Connect an external pullup resistor to any supply from 0 to 5.5V. Select a resistor value large enough to register a logic low when $\overline{\text{RESET}}$ is asserted and small enough to register a logic high while supplying all input current and leakage paths connected to the $\overline{\text{RESET}}$ line. A 10k Ω to 100k Ω pullup is sufficient in most applications.

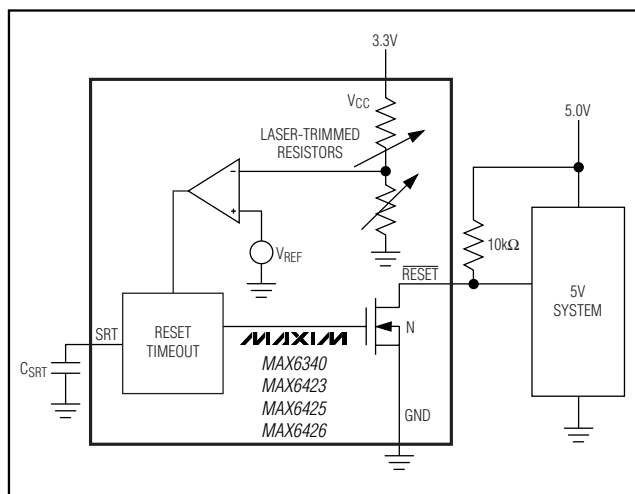


Figure 1. MAX6340/MAX6423/MAX6425/MAX6426 Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Selecting a Reset Capacitor

The reset timeout period is adjustable to accommodate a variety of μ P applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and ground. Calculate the reset timeout capacitor as follows:

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$$C_{SRT} = (t_{RP} - 275\mu s) / (2.73 \times 10^6)$$

where t_{RP} is in seconds and C_{SRT} is in farads.

The reset delay time is set by a current/capacitor-controlled ramp compared to an internal 0.65V reference. An internal 240nA ramp current source charges the external capacitor. The charge to the capacitor is cleared when a reset condition is detected. Once the reset condition is removed, the voltage on the capacitor ramps according to the formula: $dV/dt = I/C$. The C_{SRT} capacitor must ramp to 0.65V to deassert the reset. C_{SRT} must be a low-leakage (<10nA) type capacitor; ceramic is recommended.

Operating as a Voltage Detector

The MAX6340/MAX6421-MAX6426 can be operated in a voltage detector mode by floating the SRT pin. The reset delay times for V_{CC} rising above or falling below the threshold are not significantly different. The reset output is deasserted smoothly without false pulses.

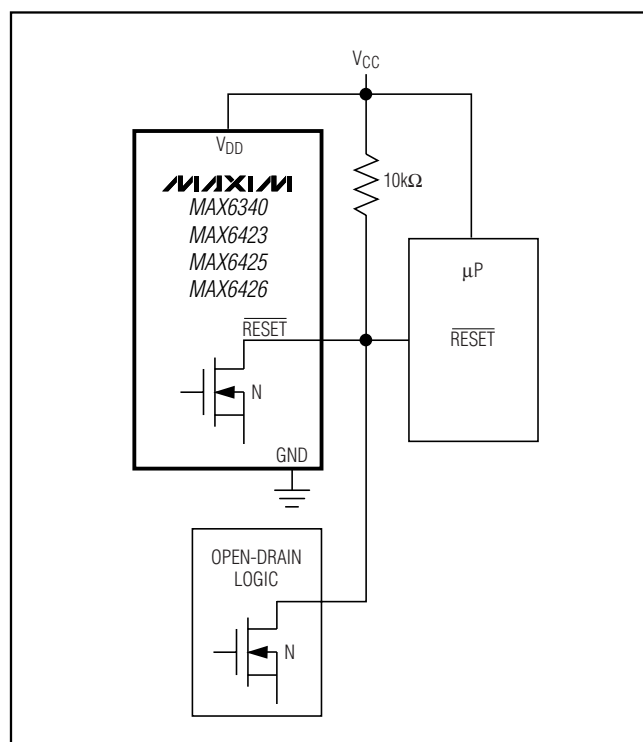


Figure 2. Wired-OR Reset Circuit

Applications Information

Interfacing to Other Voltages for Logic Compatibility

The open-drain outputs of the MAX6340/MAX6423/MAX6425/MAX6426 can be used to interface to μ Ps with other logic levels. As shown in Figure 1, the open-drain output can be connected to voltages from 0 to 5.5V. This allows for easy logic compatibility to various μ Ps.

Wired-OR Reset

To allow auxiliary circuitry to hold the system in reset, an external open-drain logic signal can be connected to the open-drain $\overline{\text{RESET}}$ of the MAX6340/MAX6423/MAX6425/MAX6426, as shown in Figure 2. This configuration can reset the μ P, but does not provide the reset timeout when the external logic signal is released.

Negative-Going V_{CC} Transients

In addition to issuing a reset to the μ P during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going transients (glitches). The graph Maximum Transient Duration vs. Reset Threshold Overdrive in the *Typical Operating Characteristics* shows this relationship.

The area below the curve of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a negative-going pulse applied to V_{CC} , starting above the actual reset threshold (V_{TH}) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient decreases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50 μ s or less does not cause a reset pulse to be issued.

Ensuring a Valid $\overline{\text{RESET}}$ or $\overline{\text{RESET}}$ Down to $V_{CC} = 0$

When V_{CC} falls below 1V, $\overline{\text{RESET}}$ / $\overline{\text{RESET}}$ current-sinking (sourcing) capabilities decline drastically. In the case of the MAX6421/MAX6424, high-impedance CMOS-logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problems in most applications, since most μ Ps and other circuitry do not operate with V_{CC} below 1V.

In those applications where $\overline{\text{RESET}}$ must be valid down to zero, adding a pulldown resistor between $\overline{\text{RESET}}$ and ground sinks any stray leakage currents, holding $\overline{\text{RESET}}$ low (Figure 3). The value of the pulldown resistor is not critical; 100k Ω is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground. For applications using the MAX6422, a 100k Ω pullup resis-

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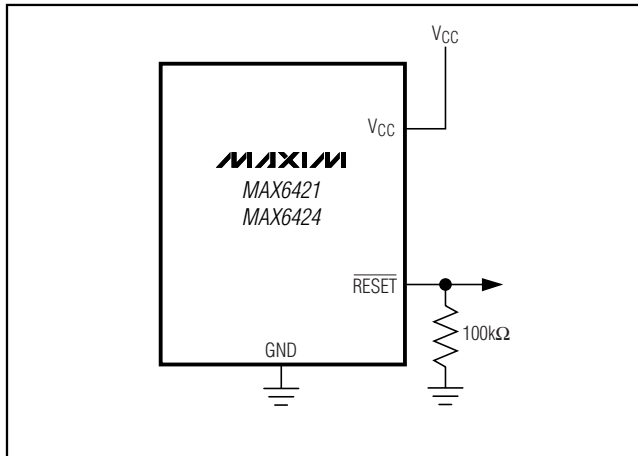


Figure 3. Ensuring $\overline{\text{RESET}}$ Valid to $V_{CC} = 0$

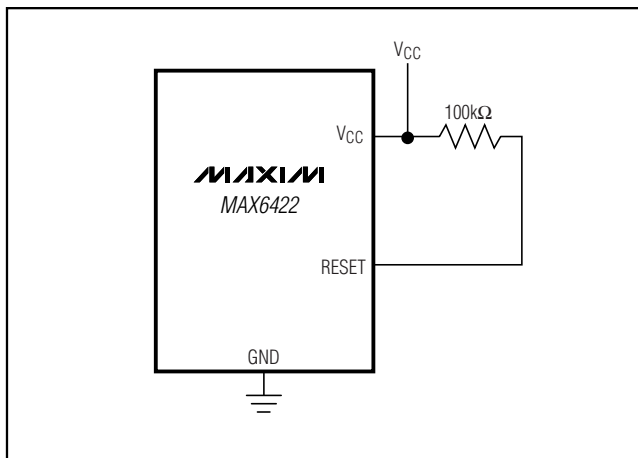


Figure 4. Ensuring $\overline{\text{RESET}}$ Valid to $V_{CC} = 0$

tor between RESET and V_{CC} holds RESET high when V_{CC} falls below 1V (Figure 4). Open-drain RESET versions are not recommended for applications requiring valid logic for V_{CC} down to zero.

Layout Consideration

SRT is a precise current source. When developing the layout for the application, be careful to minimize board capacitance and leakage currents around this pin. Traces connected to SRT should be kept as short as possible. Traces carrying high-speed digital signals and traces with large voltage potentials should be routed as far from SRT as possible. Leakage current and stray capacitance (e.g., a scope probe) at this pin could cause errors in the reset timeout period. When evaluating these parts, use clean prototype boards to ensure accurate reset periods.

Table 1. Reset Threshold Voltage Suffix

| SUFFIX | MIN | TYP | MAX |
|--------|-------|-------|-------|
| 16 | 1.536 | 1.575 | 1.614 |
| 17 | 1.623 | 1.665 | 1.707 |
| 18 | 1.755 | 1.800 | 1.845 |
| 19 | 1.853 | 1.900 | 1.948 |
| 20 | 1.950 | 2.000 | 2.050 |
| 21 | 2.048 | 2.100 | 2.153 |
| 22 | 2.133 | 2.188 | 2.243 |
| 23 | 2.313 | 2.313 | 2.371 |
| 24 | 2.340 | 2.400 | 2.460 |
| 25 | 2.438 | 2.500 | 2.563 |
| 26 | 2.559 | 2.625 | 2.691 |
| 27 | 2.633 | 2.700 | 2.768 |
| 28 | 2.730 | 2.800 | 2.870 |
| 29 | 2.852 | 2.925 | 2.998 |
| 30 | 2.925 | 3.000 | 3.075 |
| 31 | 2.998 | 3.075 | 3.152 |
| 32 | 3.120 | 3.200 | 3.280 |
| 33 | 3.218 | 3.300 | 3.383 |
| 34 | 3.315 | 3.400 | 3.485 |
| 35 | 3.413 | 3.500 | 3.558 |
| 36 | 3.510 | 3.600 | 3.690 |
| 37 | 3.608 | 3.700 | 3.793 |
| 38 | 3.705 | 3.800 | 3.895 |
| 39 | 3.803 | 3.900 | 3.998 |
| 40 | 3.900 | 4.000 | 4.100 |
| 41 | 3.998 | 4.100 | 4.203 |
| 42 | 4.095 | 4.200 | 4.305 |
| 43 | 4.193 | 4.300 | 4.408 |
| 44 | 4.266 | 4.375 | 4.484 |
| 45 | 4.388 | 4.500 | 4.613 |
| 46 | 4.509 | 4.625 | 4.741 |
| 47 | 4.583 | 4.700 | 4.818 |
| 48 | 4.680 | 4.800 | 4.920 |
| 49 | 4.778 | 4.900 | 5.023 |
| 50 | 4.875 | 5.000 | 5.125 |

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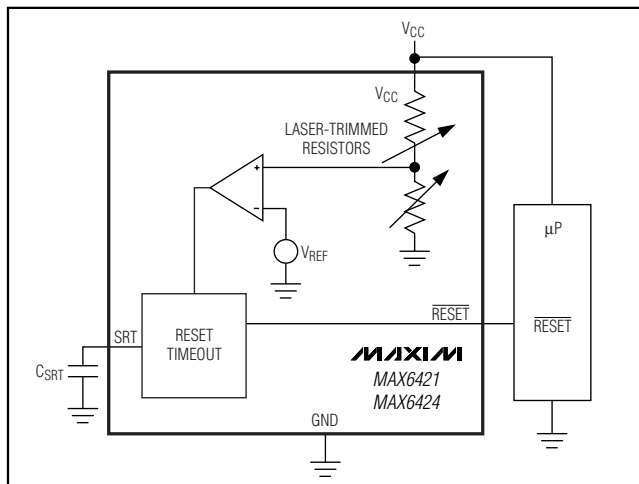
Standard Versions Table

| PART* | OUTPUT STAGE | TOP MARK |
|-----------------------|--------------------------------------|----------|
| MAX6340 UK16-T | Open-Drain $\overline{\text{RESET}}$ | AEBE |
| MAX6340UK22-T | Open-Drain $\overline{\text{RESET}}$ | AEBG |
| MAX6340UK26-T | Open-Drain $\overline{\text{RESET}}$ | AEBI |
| MAX6340UK29-T | Open-Drain $\overline{\text{RESET}}$ | AEBJ |
| MAX6340UK46-T | Open-Drain $\overline{\text{RESET}}$ | AEBM |
| MAX6421 US16-T | Push-Pull $\overline{\text{RESET}}$ | KADA |
| MAX6421XS16-T | Push-Pull $\overline{\text{RESET}}$ | ACU |
| MAX6421US22-T | Push-Pull $\overline{\text{RESET}}$ | KADE |
| MAX6421XS22-T | Push-Pull $\overline{\text{RESET}}$ | ACY |
| MAX6421US26-T | Push-Pull $\overline{\text{RESET}}$ | KADG |
| MAX6421XS26-T | Push-Pull $\overline{\text{RESET}}$ | ADA |
| MAX6421US29-T | Push-Pull $\overline{\text{RESET}}$ | KADH |
| MAX6421XS29-T | Push-Pull $\overline{\text{RESET}}$ | ADB |
| MAX6421US46-T | Push-Pull $\overline{\text{RESET}}$ | KADK |
| MAX6421XS46-T | Push-Pull $\overline{\text{RESET}}$ | ADE |
| MAX6422 US16-T | Push-Pull RESET | KADB |
| MAX6422XS16-T | Push-Pull RESET | ACV |
| MAX6422US22-T | Push-Pull RESET | KADM |
| MAX6422XS22-T | Push-Pull RESET | ADG |
| MAX6422US26-T | Push-Pull RESET | KADO |
| MAX6422XS26-T | Push-Pull RESET | ADI |
| MAX6422US29-T | Push-Pull RESET | KADP |
| MAX6422XS29-T | Push-Pull RESET | ADJ |
| MAX6422US46-T | Push-Pull RESET | KADS |
| MAX6422XS46-T | Push-Pull RESET | ADM |

| PART* | OUTPUT STAGE | TOP MARK |
|-----------------------|--------------------------------------|----------|
| MAX6423 US16-T | Open-Drain $\overline{\text{RESET}}$ | KADC |
| MAX6423XS16-T | Open-Drain $\overline{\text{RESET}}$ | ACW |
| MAX6423US22-T | Open-Drain $\overline{\text{RESET}}$ | KADU |
| MAX6423XS22-T | Open-Drain $\overline{\text{RESET}}$ | ADO |
| MAX6423US26-T | Open-Drain $\overline{\text{RESET}}$ | KADW |
| MAX6423XS26-T | Open-Drain $\overline{\text{RESET}}$ | ADQ |
| MAX6423US29-T | Open-Drain $\overline{\text{RESET}}$ | KADX |
| MAX6423XS29-T | Open-Drain $\overline{\text{RESET}}$ | ADR |
| MAX6423US46-T | Open-Drain $\overline{\text{RESET}}$ | KAEA |
| MAX6423XS46-T | Open-Drain $\overline{\text{RESET}}$ | ADU |
| MAX6424 UK16-T | Push-Pull $\overline{\text{RESET}}$ | ADUF |
| MAX6424UK22-T | Push-Pull $\overline{\text{RESET}}$ | ADUK |
| MAX6424UK26-T | Push-Pull $\overline{\text{RESET}}$ | ADUM |
| MAX6424UK29-T | Push-Pull $\overline{\text{RESET}}$ | ADUN |
| MAX6424UK46-T | Push-Pull $\overline{\text{RESET}}$ | ADUQ |
| MAX6425 UK16-T | Open-Drain $\overline{\text{RESET}}$ | ADUG |
| MAX6425UK22-T | Open-Drain $\overline{\text{RESET}}$ | ADUS |
| MAX6425UK26-T | Open-Drain $\overline{\text{RESET}}$ | ADUU |
| MAX6425UK29-T | Open-Drain $\overline{\text{RESET}}$ | ADUV |
| MAX6425UK46-T | Open-Drain $\overline{\text{RESET}}$ | ADUY |
| MAX6426 UK16-T | Open-Drain $\overline{\text{RESET}}$ | ADUH |
| MAX6426UK22-T | Open-Drain $\overline{\text{RESET}}$ | ADVA |
| MAX6426UK26-T | Open-Drain $\overline{\text{RESET}}$ | ADVC |
| MAX6426UK29-T | Open-Drain $\overline{\text{RESET}}$ | ADVD |
| MAX6426UK46-T | Open-Drain $\overline{\text{RESET}}$ | ADVG |

MAX6340/MAX6421-MAX6426

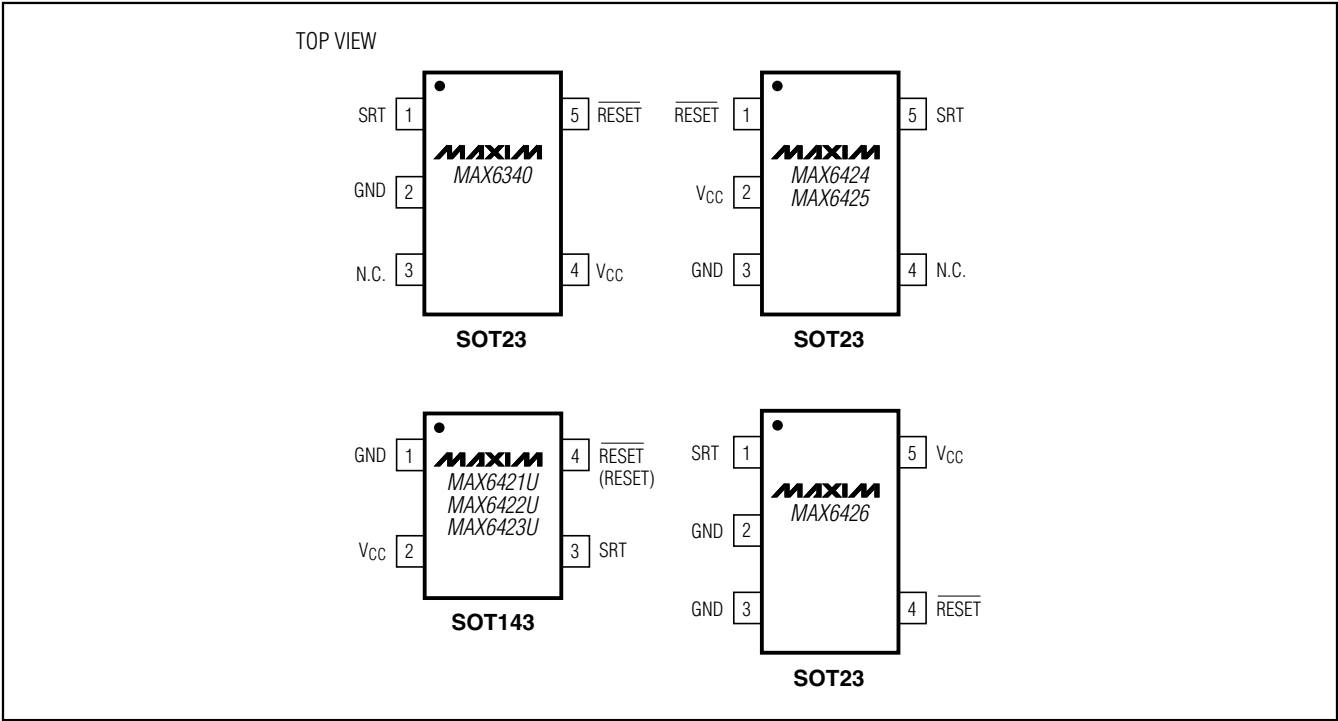
Typical Operating Circuit



*Sample stock is generally held on all standard versions. Contact factory for availability of nonstandard versions.

Low-Power, SC70/SOT μ P Reset Circuits with Capacitor-Adjustable Reset Timeout Delay

Pin Configurations (continued)



Selector Guide

| PART | PUSH-PULL $\overline{\text{RESET}}$ | PUSH-PULL RESET | OPEN-DRAIN $\overline{\text{RESET}}$ | PIN-PACKAGE |
|---------|-------------------------------------|-----------------|--------------------------------------|---------------|
| MAX6340 | — | — | ✓ | 5 SOT23 |
| MAX6421 | ✓ | — | — | 4 SOT143/SC70 |
| MAX6422 | — | ✓ | — | 4 SOT143/SC70 |
| MAX6423 | — | — | ✓ | 4 SOT143/SC70 |
| MAX6424 | ✓ | — | — | 5 SOT23 |
| MAX6425 | — | — | ✓ | 5 SOT23 |

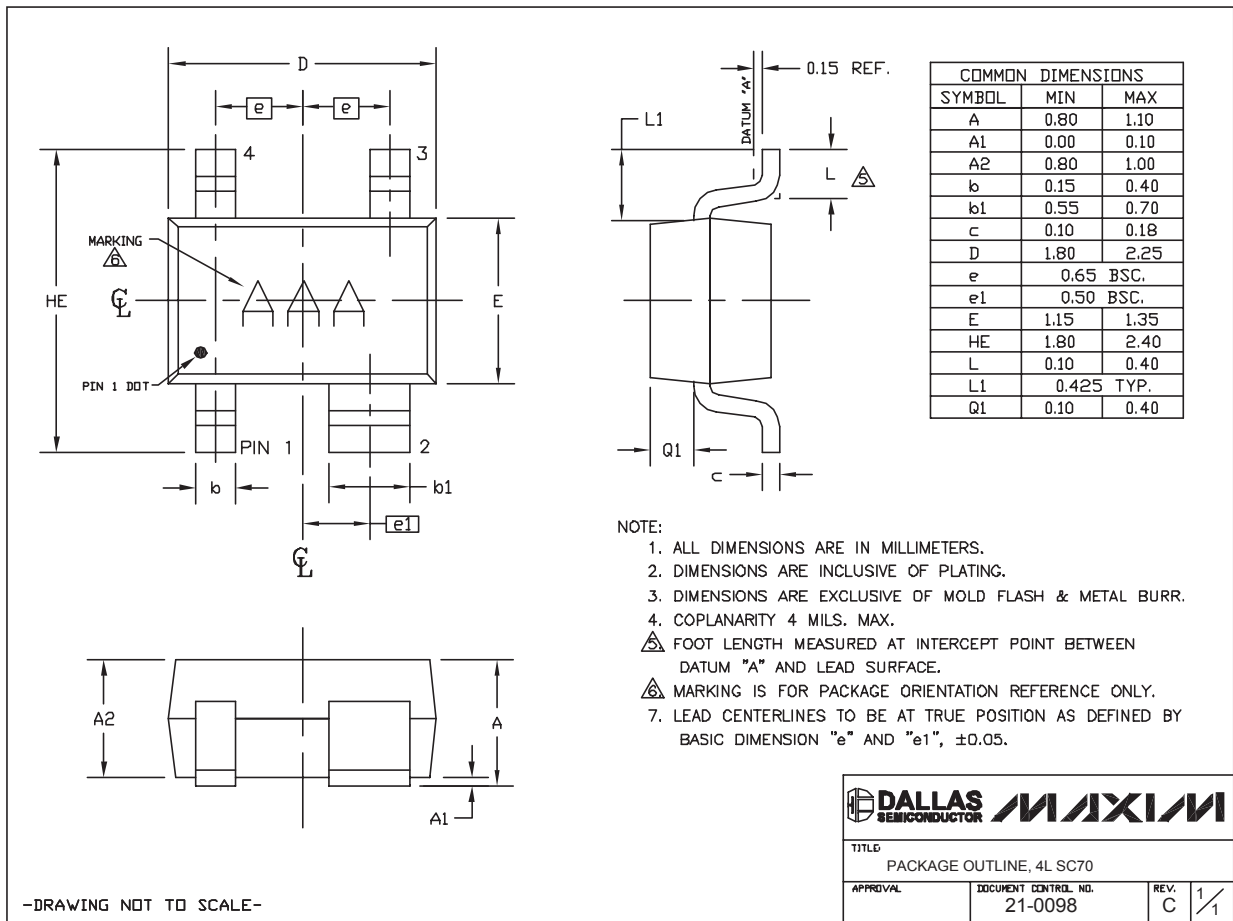
Chip Information

TRANSISTOR COUNT: 295
PROCESS: BiCMOS

Low-Power, SC70/SOT μ P Reset Circuits with Capacitor-Adjustable Reset Timeout Delay

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

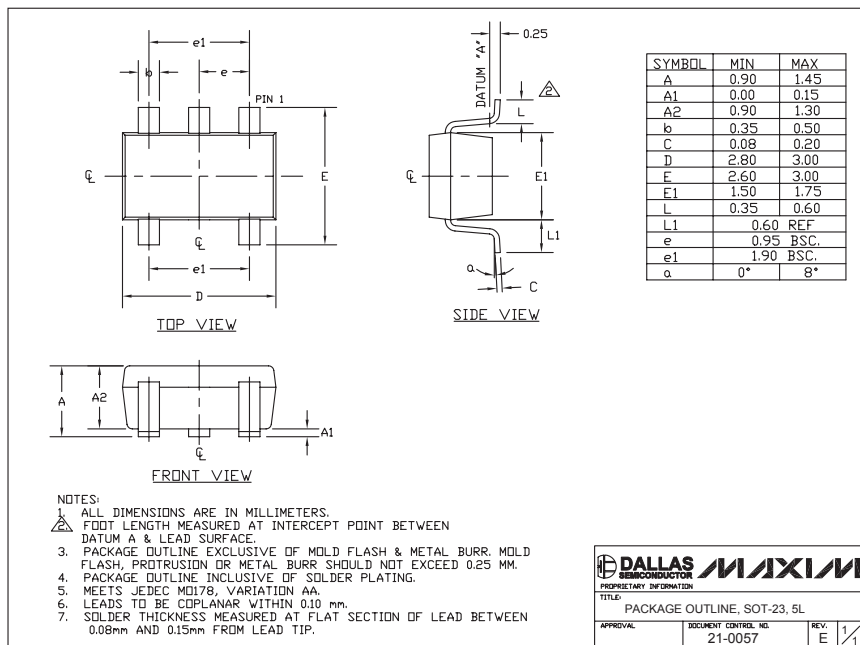
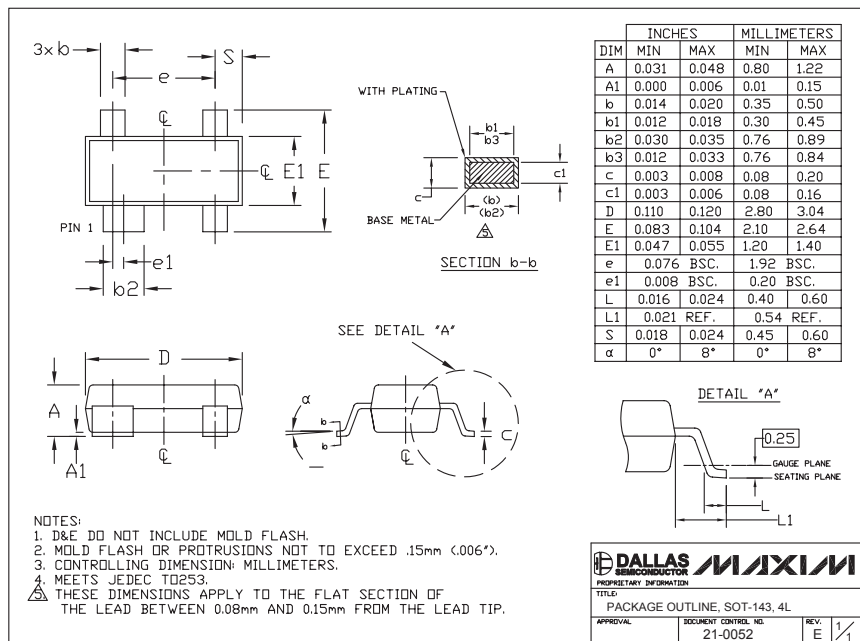


MAX6340/MAX6421-MAX6426

Low-Power, SC70/SOT μ P Reset Circuits with Capacitor-Adjustable Reset Timeout Delay

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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