MAX1788EUI
Rev. B

RELIABILITY REPORT

FOR

MAX1788EUI

PLASTIC ENCAPSULATED DEVICES

November 3, 2008

MAXIM INTEGRATED PRODUCTS

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Written by

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Conclusion

The MAX1788 is completing final qualification.

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I. Device Description

A. General

The MAX1788 smart battery-pack controller integrates a user programmable microcontroller core, a Coulomb-counting fuel gauge, a multi-channel data-acquisition unit, protection drivers, and SMBus™ v1.1 compliant master/slave SMBus interface. The 8-bit RISC microcontroller core integrates 8k bytes of user programmable flash and an 8k byte ROM library. This provides battery-pack designers with complete flexibility in developing fuel gauging and control algorithms. The MAX1788 is equipped with ISD (In System Debug) capability for efficient firmware development and debugging.

The MAX1788 includes a 12-bit data-acquisition unit to measure individual cell voltages, thermistors, instantaneous current and pack voltage. Individual cell voltage measurements with 0.5% accuracy and overcurrent protection to provide first level protection. Internally adjustable over-current thresholds and delay timers provide a flexible solution.

The integrating fuel gauge module has a typical input offset of 1µV, and gain accuracy of better than 1% with no trimming required during pack manufacture. The MAX1788 has a wide 4V to 25V operating voltage range, and is available in a 28 pin TSSOP. The MAX1788 EvKit, development tools and reference design are available..

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II. Manufacturing Information

A. Description/Function:	Advanced Smart Battery-Pack Controller
B. Process:	S4E
C. Number of Device Transistors:	333,920
D. Fabrication Location:	California, USA
E. Assembly Location:	Thailand or Philippines
F. Date of Initial Production:	April, 2008

III. Packaging Information

A. Package Type:	**28-Pin TSSOP**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-2933
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	108 x 169 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Cu (Cu = 0.5%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1, Metal2 & Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1, Metal2 & Metal3 = 0.4 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{135 \times 4340 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.4 \times 10^{-9}$

λ = 22.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S4E Process results in a FIT Rate of 0.9 @ 25C and 13.84 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The UC10 die type has been found to have all pins able to withstand a transient ESD pulse of 1000 V HBM per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX1788EUI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

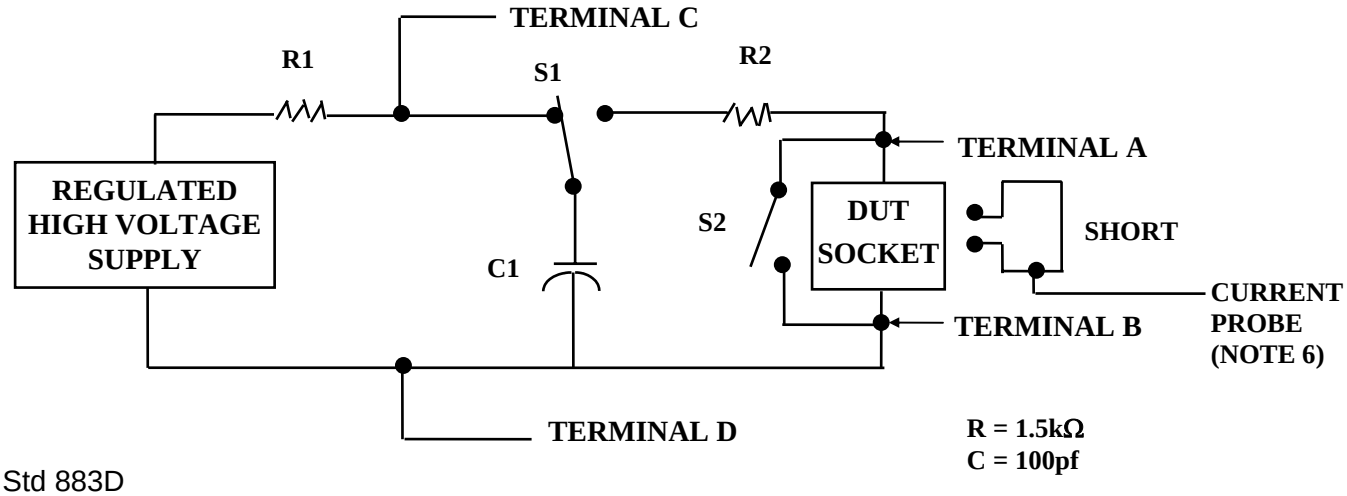
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_{S,}$ $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8