MP6400

Low Quiescent Current Programmable-Delay Supervisory Circuit

The Future of Analog IC Technology

DESCRIPTION

The MP6400 family is the microprocessor (µP) supervisory circuit which can monitor and provide reset function for system voltages from 0.4V. When either the SENSE voltage falls below its threshold (V_{IT}) or the voltage of manual reset ($\overline{MR}$) is pulled to a logic low, the $\overline{RESET}$ signal will be asserted. The reset voltage can be factory-set for standard voltage rails from 0.9V to 5V, while the MP6400DG(J)-01 reset voltage is adjustable with an external resistor divider. When SENSE voltage and $\overline{MR}$ exceed their thresholds, $\overline{RESET}$ is driven to a logic high after a user-programmable delay time.

The MP6400 has a very low quiescent current of 1.6µA typically, which makes it ideal suitable for battery-powered applications. It provides a precision reference to achieve ±1% threshold accuracy. The reset delay time can be selected by a capacitor which is connected between C_{DELAY} and GND, allowing the user to select any delay time from 2.1ms to 10s. 380ms delay time is selected by connecting the C_{DELAY} pin to V_{CC}, while 24ms delay time by leaving the C_{DELAY} pin float. MP6400 is available in TSOT23 and 2mm×2mm 6-pin QFN packages.

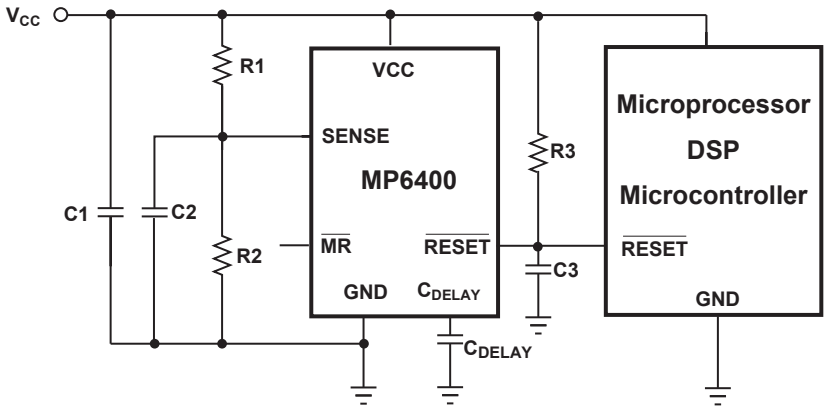
FEATURES

- Fixed Threshold Voltages for Standard Voltage Rails From 0.9V to 5V and Adjustable Voltage From 0.4V are Available
- Low Quiescent Current: 1.6uA typ
- Power-On Reset Generator with Adjustable Delay Time: 2.1ms to 10s
- High Threshold Accuracy: ±1% typ
- Manual Reset ($\overline{MR}$) Input
- Open-Drain $\overline{RESET}$ Output
- Immune to Short Negative SENSE voltage
- Guaranteed Reset Valid to V_{CC}=0.8V
- 6 Pin TSOT23 and 2mm×2mm QFN

APPLICATIONS

- DSP or Micro controller Applications
- Laptop/Desktop Computers
- PDAs/Hand-Held Products
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Free Air Temperature (T_A)
MP6400DG-XX	QFN6 (2x2mm)	–40°C to +85°C
MP6400DJ-XX	TSOT23-6	

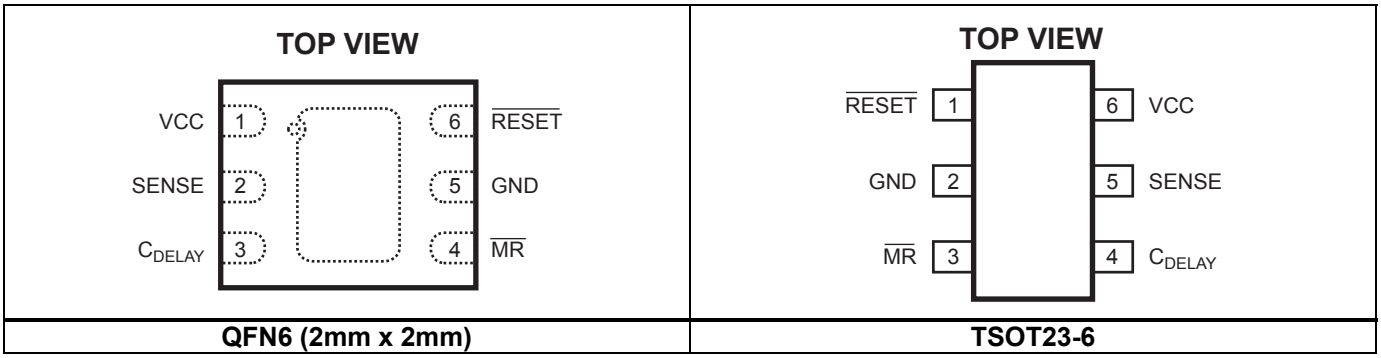
*For Tape & Reel, add suffix –Z (e.g. MP6400DG–XX-Z);

For RoHS compliant packaging, add suffix –LF (e.g. MP6400DG–XX-LF–Z).

**For Tape & Reel, add suffix –Z (e.g. MP6400DJ–XX-Z);

For RoHS compliant packaging, add suffix –LF(e.g. MP6400DJ–XX-LF–Z).

PACKAGE REFERENCE



QFN6 (2mm x 2mm)	TSOT23-6

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{CC} ..... -0.3 to 6.5 V
C_{DELAY} Voltage V_{CDELAY} ..... –0.3V to V_{CC} + 0.3V
SENSE Voltage V_{SENSE} ..... –0.3V to 6V
All Other Pins ..... –0.3V to +6.5V
RESET Current $I_{\overline{RESET}}$ 5mA
Continuous Power Dissipation (T_A = +25°C) (2)
QFN6 (2mmx2mm) 2.5W
TSOT23-6 ..... 0.57W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} ..... 1.8V to 6V
Operating Junct. Temp (T_J) ..... –40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN6 (2mmx2mm)	50	12 °C/W
TSOT23-6	220	110 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer board.

ELECTRICAL CHARACTERISTICS

1.8V≤V_{CC}≤6V, R_3 = 100kΩ, C_3 = 47pF, T_A= -40°C to +85°C, Typical values are at T_A=+25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply Range	V_{CC}		1.8		6	V
Supply Current (current into V_{CC} pin)	I_{CC}	V_{CC} = 3.3V, $\overline{RESET}$ not asserted. $\overline{MR}$, $\overline{RESET}$, C_{DELAY} open		1.6	3.5	µA
		V_{CC} = 6V, $\overline{RESET}$ not asserted.$\overline{MR}$, $\overline{RESET}$, C_{DELAY} open		1.85	12	µA
Low-level Output Voltage	V_{OL}	1.3V ≤ V_{CC} < 1.8V, I_{OL} = 0.4mA			0.3	V
		1.8V ≤ V_{CC} ≤ 6V, I_{OL} = 1.0mA			0.4	V
Power-up Reset Voltage(5)		V_{OL} (max) = 0.2V, $I_{\overline{RESET}}$ =15uA $T_{rise(Vcc)}$≥15µs/V			0.8	V
Negative-going Input Threshold Accuracy	V_{IT}	V_{SENSE} falling slowly		±1.0	±2.0	%
Hysteresis on V_{IT} Pin	V_{HYS}			1.5	3.5	V_{IT}%
$\overline{MR}$ Internal Pull-up Resistance	$R_{\overline{MR}}$		50	110		kΩ
Input Current at SENSE Pin	I_{SENSE}	MP6400DJ-01 V_{SENSE} = V_{IT}	-25		+25	nA
		Fixed versions V_{SENSE} = 6V		2.4		µA
$\overline{RESET}$ Leakage Current		$V_{\overline{RESET}}$ = 6V, $\overline{RESET}$ not asserted			300	nA
$\overline{MR}$ Logic Low Input	V_{IL}				0.25V_{CC}	V
$\overline{MR}$ Logic High Input	V_{IH}		0.7V_{CC}			V
SENSE Maximum Transient Duration	t_w	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		17.5		µs
$\overline{RESET}$ Delay Time	t_d	C_{DELAY} = Open	15	24	34	ms
		C_{DELAY} = V_{CC}(6)	230	380	530	ms
		C_{DELAY} = 150pF	1.3	2.1	3	ms
		C_{DELAY} = 10nF(6)	61	102	142	ms
$\overline{MR}$ to $\overline{RESET}$ Propagation Delay	t_{pHL1}	V_{IH} = 0.7 V_{CC}, V_{IL} = 0.25 V_{CC}		160		ns
High to Low Level $\overline{RESET}$ Delay, SENSE to $\overline{RESET}$	t_{pHL2}	V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}		17.5		µs

Note:

5) The lowest supply voltage (V_{CC}) at which $\overline{RESET}$ becomes active.

6) Guaranteed by design.

ORDERING INFORMATION (7)

Product	Package	Top Mark	Nominal Supply Voltage	Threshold Voltage (VIT)
MP6400DG-01	QFN	5B	Adjustable	0.4V
MP6400DJ-01	TSOT23	4B		
MP6400DG-09	QFN	Contact Factory	0.9V	0.84V
MP6400DJ-09	TSOT23	" "		
MP6400DG-12	QFN	" "	1.2V	1.12V
MP6400DJ-12	TSOT23	" "		
MP6400DG-125	QFN	" "	1.25V	1.16V
MP6400DJ-125	TSOT23	" "		
MP6400DG-15	QFN	" "	1.5V	1.40V
MP6400DJ-15	TSOT23	" "		
MP6400DG-18	QFN	" "	1.8V	1.67V
MP6400DJ-18	TSOT23	" "		
MP6400DG-25	QFN	" "	2.5V	2.33V
MP6400DJ-25	TSOT23	" "		
MP6400DG-30	QFN	9S	3.0V	2.79V
MP6400DJ-30	TSOT23	8S		
MP6400DG-33	QFN	9R	3.3V	3.07V
MP6400DJ-33	TSOT23	3S		
MP6400DG-50	QFN	Contact Factory	5.0V	4.65V
MP6400DJ-50	TSOT23	" "		

Note:

7) In "MP6400DG(J)- _ _", the "_ _" are placeholders for the monitored voltage levels of the devices. Desired monitored voltages are set by the suffix found in ordering information.

PIN FUNCTIONS

QFN Pin #	TSOT Pin #	Name	Description
6	1	$\overline{RESET}$	$\overline{RESET}$ is an open drain signal which will be asserted when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{MR}$) pin drops to a logic low. The $\overline{RESET}$ delay time is programmable from 2.1ms to 10s by using external capacitors. A pull-up resistor bigger than 10k should be connected this pin to supply line, and the $\overline{RESET}$ outputting a higher voltage than V_{CC} is allowable.
5	2	GND	Ground.
4	3	$\overline{MR}$	The manual reset ($\overline{MR}$) can introduce another logic signal to control the$\overline{RESET}$. It is internally connected to V_{CC} through a 90kΩ resistor.
3	4	C_{DELAY}	Programmable reset delay time pin. When C_{DELAY} connected to V_{CC} through a resistor between 50kΩ and 200kΩ, a 380ms delay time is selected. When C_{DELAY} floated, the delay time is 24ms. A capacitor bigger than 150pF connected C_{DELAY} to GND could be used to get the user's programmable time from 2.1ms to 10s.
2	5	SENSE	SENSE pin is connected to the monitored system voltage. When the monitored voltage is below desired threshold, $\overline{RESET}$ is asserted.
1	6	V_{CC}	Supply voltage. A 0.1uF decoupling ceramic capacitor should be put close to this pin.

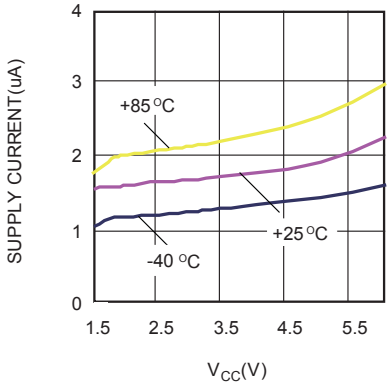
DETAIL DESCRIPTION

The MP6400 product family asserts a $\overline{RESET}$ signal when either the SENSE pin voltage is lower than V_{IT} or the manual reset ($\overline{MR}$) is driven low. The MP6400 family can be monitored a fixed voltage from 0.9V to 5.0V, while the MP6400DG(J)-01 can monitor any voltage above 0.4V by adjusting the external resistor divider. After both the manual reset ($\overline{MR}$) and SENSE voltages exceed their thresholds, the $\overline{RESET}$ output remains asserted for a user's programmable delay time. Two fixed $\overline{RESET}$ delay times are user-selectable: 380ms delay time by connecting the C_{DELAY} pin to V_{CC}, and 24ms delay time by leaving the C_{DELAY} pin float. Any delay time from 2.1ms to 10s could be gotten by connecting a capacitor between C_{DELAY} and GND. The wide monitor voltage and programmable reset delay time make MP6400 product family suitable for a broad array of applications.

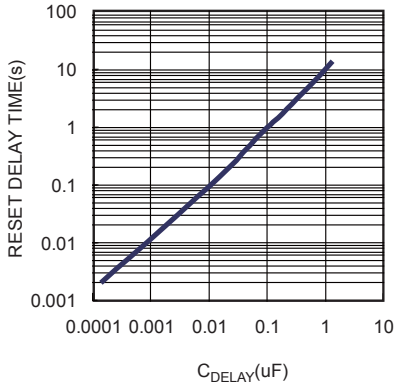
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC}=3.3V, R_3 = 100kΩ, C_3 = 47pF, T_A= -40°C to +85°C, Typical values are at T_A=+25°C, unless otherwise noted.

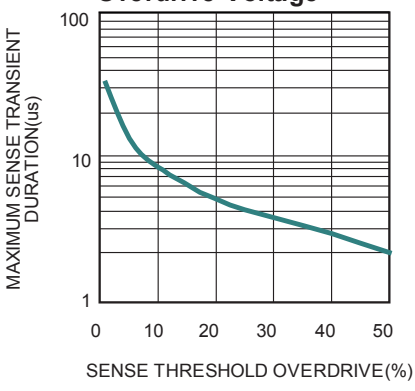
Supply Current vs. V_{CC}



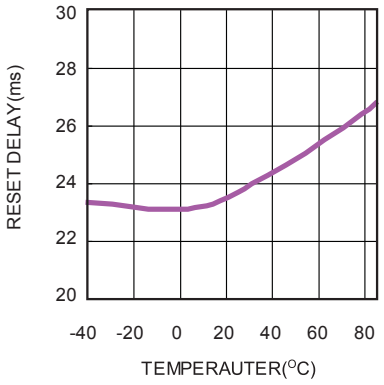
Reset Delay Time vs. C_{DELAY}



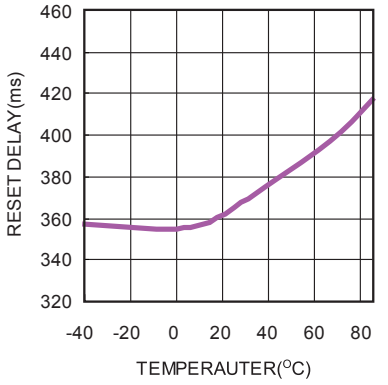
Maximum SENSE Transient Duration vs.SENSE Threshold Overdrive Voltage



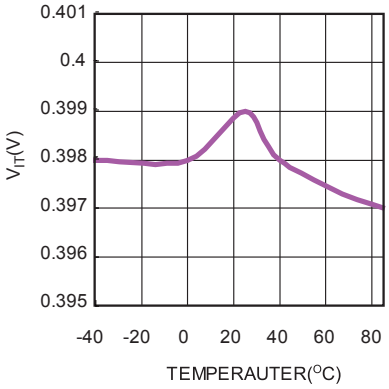
Reset Delay vs.Temperature
(C_{DELAY}=open)



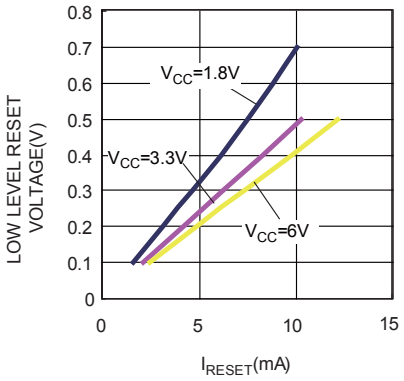
Reset Delay vs.Temperature
(C_{DELAY}=V_{CC})



V_{IT} vs. Temperature



I_{RESET} vs. Low Level RESET Voltage



FUNCTIONAL BLOCK DIAGRAM

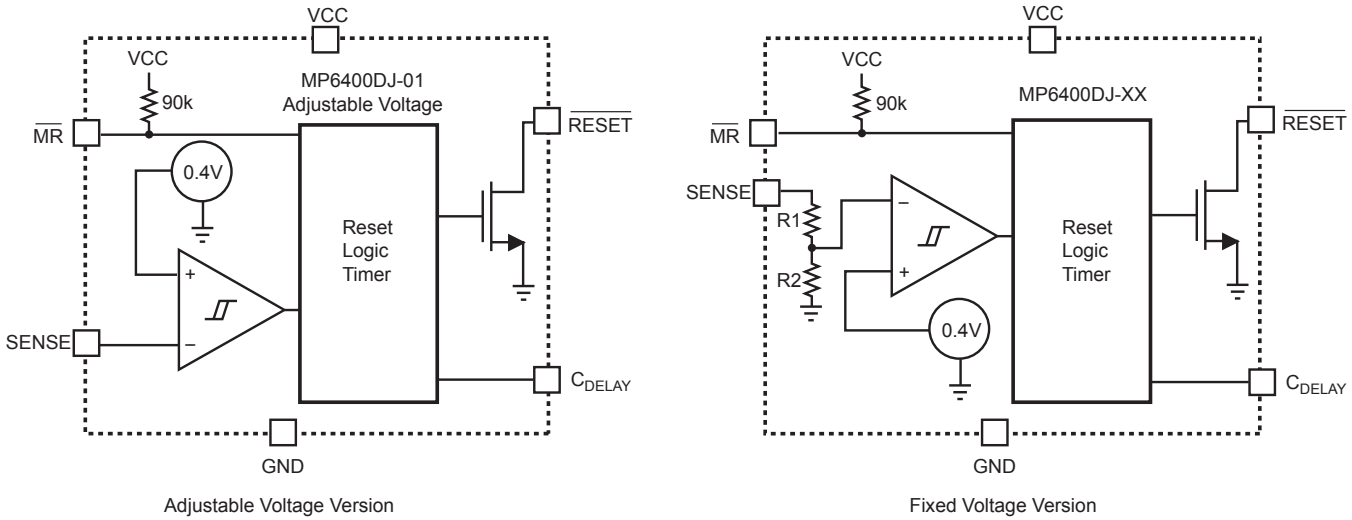


Figure 1—Functional Block Diagram

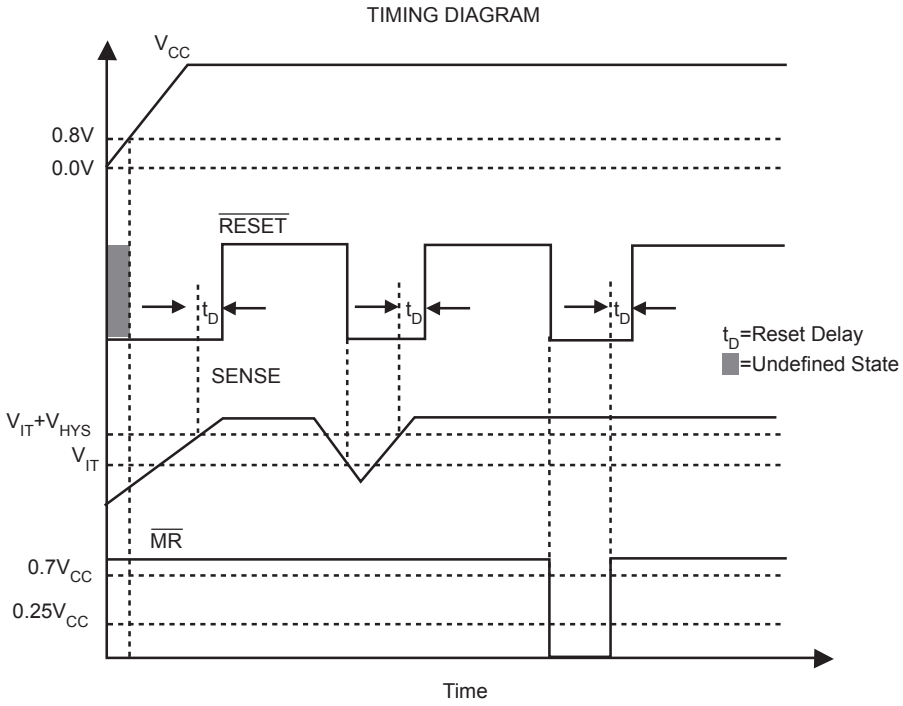


Figure 2—MP6400 Timing Diagram

TRUTH TABLE

$\overline{MR}$	SENSE > V_{IT}	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

APPLICATION INFORMATION

Reset Output Function

The MP6400 $\overline{RESET}$ output is typically connected to the $\overline{RESET}$ input of a microprocessor, as shown in Figure 3. When $\overline{RESET}$ is not asserted, a pull up resistor must be connected to hold this signal high. The voltage of reset signal is allowed to be higher than V_{CC} (up to 6V) through a resistor pulling up from supply line. If the voltage is below 0.8V, $\overline{RESET}$ output is undefined. This condition can be ignored generally because that most microprocessors do not function at this state. When both SENSE and $\overline{MR}$ are higher than their threshold voltage, $\overline{RESET}$ output holds logic high. Once either of the two drops below their threshold, $\overline{RESET}$ will be asserted.

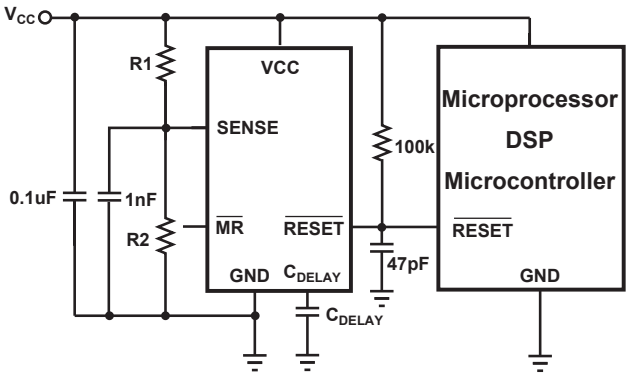


Figure 3—Typical Application of MP6400 with Microprocessor

From the point that $\overline{MR}$ is again logic high and SENSE is above V_{IT} + V_{HYS} (the threshold hysteresis), $\overline{RESET}$ will be driven to a logic high after a reset delay time. The reset delay time is programmable by C_{DELAY} pin. Due to the finite impedance of $\overline{RESET}$ pin, the pull up resistor should be bigger than 10kΩ.

Monitor a Voltage

The SENSE input pin is connected to the monitored system voltage directly or through a resistor network (on MP6400DJ-01). When the voltage on the pin is below V_{IT}, $\overline{RESET}$ is asserted. A threshold hysteresis will prevent the chip from responding perturbation on SENSE pin. A 1nF to 10nF bypass capacitor should be put on this pin to increase its immunity to noise. A typical application of the MP6400DJ-01 is shown in Figure 4. Two external resistors form a voltage divider from monitored voltage to GND. Its tap connects to the SENSE pin. The circuit can be used to monitor any voltage higher than 0.4V.

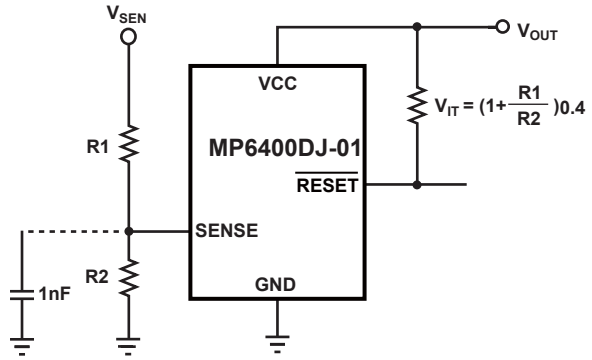


Figure 4—MP6400DJ-01 Monitoring a User-Defined Voltage

Monitor Multiple System Voltages

The manual reset ($\overline{MR}$) can introduce another logic signal to control the $\overline{RESET}$. When $\overline{MR}$ is a logic low (0.25V_{CC}), $\overline{RESET}$ will be asserted. After both SENSE and $\overline{MR}$ are above their thresholds, $\overline{RESET}$ will be driven to a logic high after a reset delay time. The $\overline{MR}$ is internally connected to V_{CC} through a 90kΩ resistor so this pin can float. See how multiple system voltages are monitored by $\overline{MR}$ in Figure 5. If the signal on $\overline{MR}$ isn't up to V_{CC}, there will be an additional current through internal 90kΩ pull up resistor. A logic-level FET can be used to minimize the leakage, as shown in Figure 6.

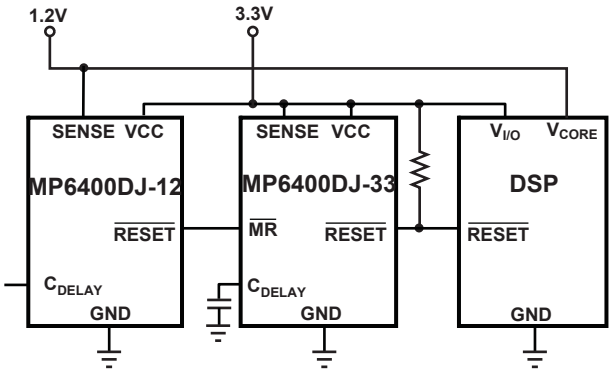


Figure 5— MP6400 Family Monitoring Multiple System Voltages

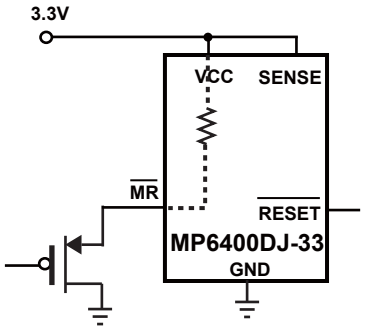


Figure 6—Minimizing I_{CC} When $\overline{MR}$ Signal isn't over V_{CC} by External MOSFET

Programmable Reset Delay Time

The reset delay time can be programmed by C_{DELAY} configure. When C_{DELAY} is connected to VCC through a resistor between 50kΩ and 200kΩ, the delay time is 380ms. When C_{DELAY} floated, the delay time is 24ms. In addition, a capacitor connected C_{DELAY} to GND could be used to get the user's programmable delay time from 2.1ms to 10s. The three configures can be found in Figure 7(a)(b)(c).

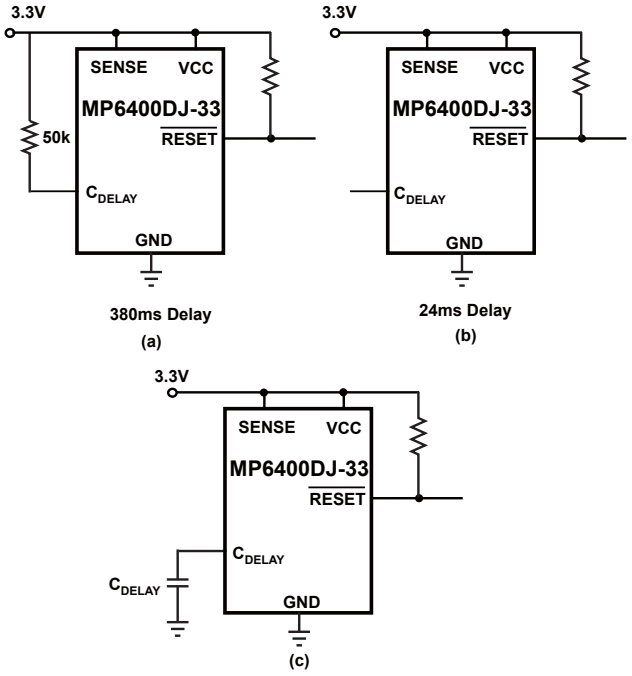


Figure 7—Programmable Configurations to the Reset Delay Time

The external capacitor C_{DELAY} must be larger than 150pF. For a given delay time, the capacitor value can be calculated using the following equation:

$$C_{DELAY}(nF) = [t_D(s) - 4.99 \times 10^{-4}(s)] \times 107$$

The reset delay time is determined by the charge time of external capacitor. While SENSE is above V_{IT} and $\overline{MR}$ is a logic high, the internal 140nA current source is enabled and starts to charge the capacitor to set the delay time. When the capacitor voltage rises to 1.13V, the $\overline{RESET}$ is de-asserted. The capacitor will be discharged when the $\overline{RESET}$ is again asserted. Stray capacitance may cause errors of the delay time. A ceramic capacitor with low leakage is strongly recommended.

SENSE Voltage Transients Immunity

The MP6400 can be immune to SENSE pin short negative transient. The maximum immune duration is 17us while overdrive is 5%. A shorter negative transient can not assert the $\overline{RESET}$ output. The effective duration is relative to the threshold overdrive, as shown in Figure 8.

Maximum SENSE Transient Duration vs.SENSE Threshold Overdrive Voltage

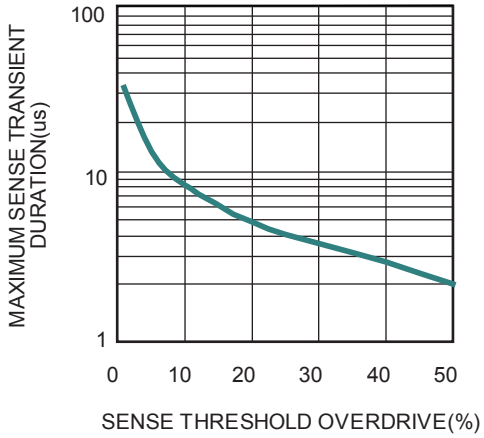
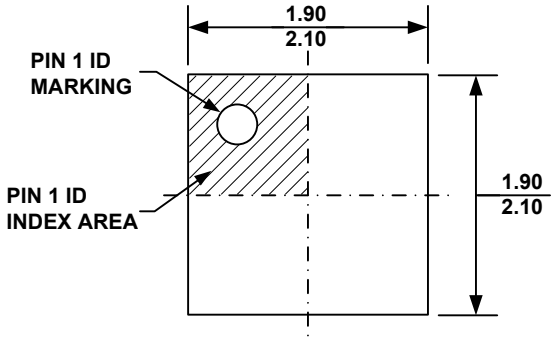


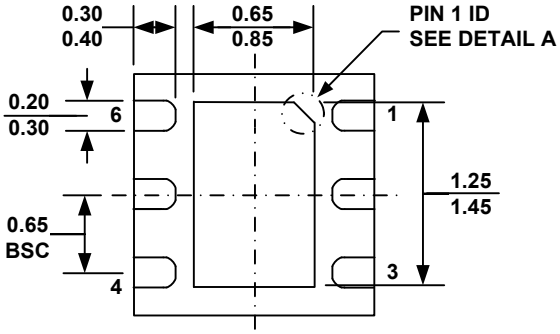
Figure 8—Maximum Transient Duration vs. Sense Threshold Overdrive Voltage

PACKAGE INFORMATION

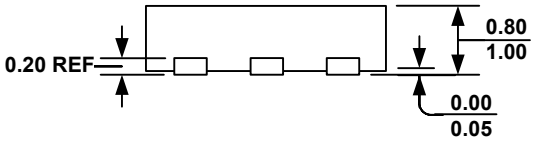
QFN6 (2mm x 2mm)



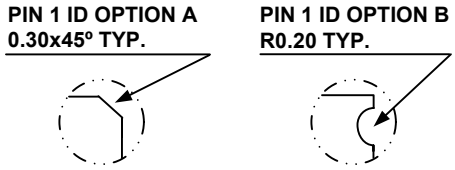
TOP VIEW



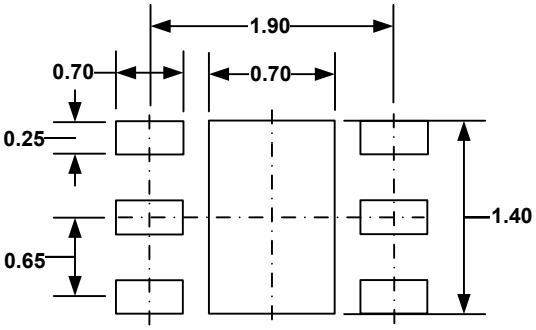
BOTTOM VIEW



SIDE VIEW



DETAIL A

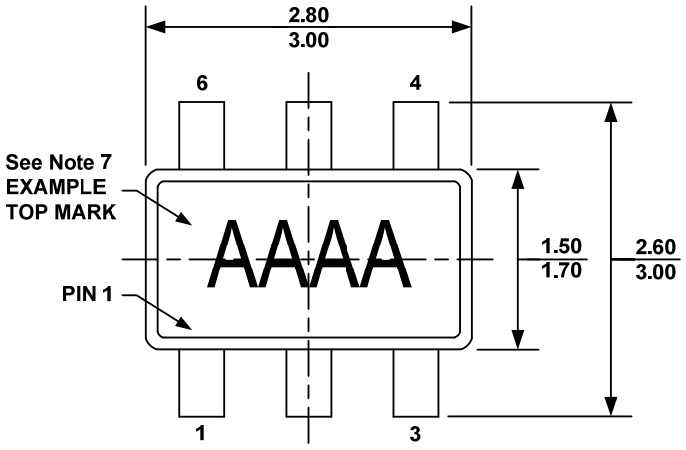


RECOMMENDED LAND PATTERN

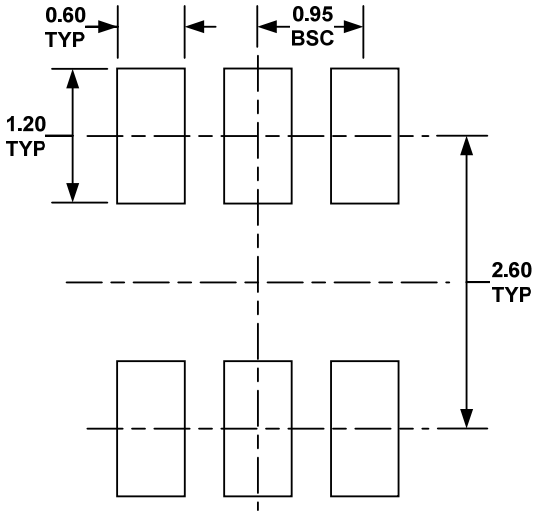
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-229, VARIATION VCCC.
5) DRAWING IS NOT TO SCALE.

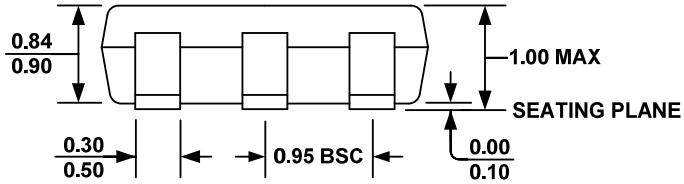
TSOT23-6



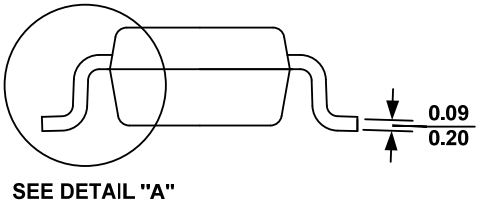
TOP VIEW



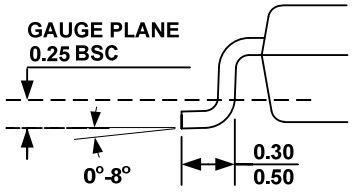
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)