19-1573; Rev 0; 10/99

MAXIM

3V Dual RS-232 Transceiver with LCD Supply and Contrast Controller

General Description

The MAX3325 integrates a two-transmitter, two-receiver RS-232 transceiver with an LCD supply plus temperature-compensated contrast control. It is intended for small 3V instruments requiring a 5V supply for either logic or an LCD display, an adjustable bias signal for contrast, LCD temperature compensation, and an RS-232 interface for serial communications.

The 5V supply is a regulated charge pump followed by a low-dropout (LDO) linear regulator capable of supplying 11mA for the 5V LCD power.

The MAX3325 has an internal 6-bit digital-to-analog converter (DAC) providing 64 contrast levels, plus an internal temperature sensor that compensates the LCD's contrast for changes in ambient temperature. The LCD contrast can be designed for any voltage range from -5V to +2V.

The MAX3325's 250kbps RS-232 transceiver meets all EIA-232E specifications with input voltages from +3.0V to +3.6V. Both the RS-232 section and the LCD supply circuitry can be independently placed in shutdown, tailoring power consumption for battery-powered equipment. The MAX3325 is available in 28-pin SSOP and narrow DIP packages.

Applications

PDAs and Palmtop Computers

Handy Terminals

GPS Receivers

Hand-Held Medical Equipment

Industrial Test Equipment

Typical Operating Circuit appears at end of data sheet.

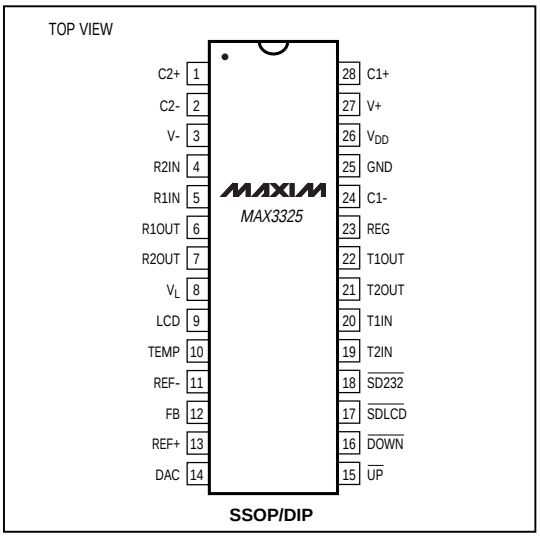
Features

- **+3.0V to +3.6V Single-Supply Operation**
- **Provides 5.0V Regulated Output at 11mA in 3V Systems**
- **6-Bit DAC with Up/Down Interface for LCD Contrast Adjustment**
- **Selectable Positive or Negative LCD Bias**
- **Meets EIA-232E Specifications at 250kbps—Guaranteed**
- **1µA Shutdown Mode**
- **Uses Small 0.22µF Capacitors—No Inductors Required**
- **Temperature Sensor for LCD Contrast Compensation**
- **Simple, Flexible Design Procedure for a Broad Range of LCD Displays**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3325CAI	0°C to +70°C	28 SSOP
MAX3325CNI	0°C to +70°C	28 Narrow Plastic DIP
MAX3325EAI	-40°C to +85°C	28 SSOP
MAX3325ENI	-40°C to +85°C	28 Narrow Plastic DIP

Pin Configuration



3V Dual RS-232 Transceiver with LCD Supply and Contrast Controller

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_L to GND .....-0.3V to +6V
LCD, REF-, TEMP to GND .....-6V to (V_{DD} + 0.3V)
V+ to GND (Note 1) .....-0.3V to +7V
V- to GND (Note 1) .....+0.3V to -7V
V+ to |V-| (Note 1) .....+13V
REF+, FB, R_OUT to GND .....-0.3V to (V_L + 0.3V)
Input Voltages
T_OUT, $\overline{SDLCD}$, $\overline{SD232}$, $\overline{UP}$, $\overline{DOWN}$ to GND.....-0.3V to +6V
R_IN to GND .....±25V
Output Voltages
T_OUT to GND.....±13V
R_OUT to GND.....-0.3V to (V_L + 0.3V)
REG to GND .....-0.3V to +6V
Short-Circuit Duration (T_OUT, REF+, REF-) .....Continuous
Continuous Output Current
REG.....75mA
LCD.....40mA
Continuous Power Dissipation
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
28-Pin NDIP (derate 14.3mW/°C above +70°C) 1143mW
Operating Temperature Range
MAX3325C_I .....0°C to +70°C
MAX3325E_I .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: V+ and V- can have maximum magnitudes of +7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, V_L = +3.3V, circuit and components of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
V_{DD} Supply Current	No load, V_{DD} = V_L = 3.3V, T_A = +25°C			2	4	mA
V_L Supply Current	No load, V_{DD} = V_L = 3.3V, T_A = +25°C			0.5	10	µA
V_{DD} Shutdown Supply Current	$\overline{SD232}$, $\overline{SDLCD}$ = GND; all input pins = GND or V_{DD}; V_{DD} = V_L = 3.3V; T_A = +25°C			0.5	10	µA
DIGITAL-TO-ANALOG CONVERTER						
Resolution	Guaranteed monotonic			6		Bits
Full-Scale Voltage	No load		1.13	1.2	1.27	V
Zero-Scale Voltage	No load		-15	0	10	mV
Output Impedance	0 < V_{DAC} < V_{REF}+, I_{DAC} ≤ 10µA		35	50	65	kΩ
TEMPERATURE SENSOR						
TEMP Output	T_A = +25°C			-3.2		V
TEMP Voltage Temperature Coefficient	I_{TEMP} < 22µA			-18		mV/°C
POSITIVE LINEAR REGULATOR						
REG Output Voltage	1 transmitter loaded with 5kΩ, T_A = +25°C	V_{CC} ≥ 3.15V, I_{REG} = 0 to 11mA	4.7	5	5.3	V
		V_{CC} ≥ 3.0V, I_{REG} = 0 to 7mA		5		
Line Regulation	3V < V_{DD} < 3.6V			6	50	mV
Short-Circuit Current				50		mA
NEGATIVE LINEAR REGULATOR—LCD BIAS						
Feedback Regulation Point			-20	0	20	mV
Input Leakage Current (Note 2)	V_{FB} = 0, CMOS input		-10	0	10	nA
LCD Load Regulation (Note 3)	V_{LCD} = -4.0V, load = 0 to -3mA			20		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.0V to +3.6V, V_L = +3.3V, circuit and components of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LCD Line Regulation	3V < V_{DD} < 3.6V, V_{LCD} = -4.0V		10		mV
LCD Adjustment Range	Load = -3mA	-5		+2	V
POSITIVE REFERENCE VOLTAGE					
Output Voltage	R_{REF}+ = 10kΩ	1.16	1.21	1.26	V
Load Regulation	Load = 12µA to 62µA (sourcing current)		4		mV
Short-Circuit Current			5		mA
NEGATIVE REFERENCE VOLTAGE					
Output Voltage	No load	-1.14	-1.21	-1.28	V
Load Regulation	Load = 0 to 50µA (sinking current)		35		mV
Short-Circuit Current			0.125		mA
LOGIC INPUTS ($\overline{SD232}$, $\overline{SDLCD}$, T1IN, T2IN, $\overline{UP}$, $\overline{DOWN}$)					
Logic Threshold High		2			V
Logic Threshold Low				0.8	V
Input Current	V_{IN} = GND or V_{DD}	-1		1	µA
RECEIVER OUTPUTS					
Output Voltage Low	I_{SINK} = 1.6mA			0.4	V
Output Voltage High	I_{SOURCE} = 1.0mA	0.8 • V_L			V
RECEIVER INPUTS					
Input Voltage Range		-25		+25	V
Input Threshold Low	T_A = +25°C, V_{DD} = 3.3V	0.6			V
Input Threshold High	T_A = +25°C, V_{DD} = 3.3V			2.4	V
Input Hysteresis			0.3		V
Input Resistance	-15V < V_{R_IN} < +15V, T_A = +25°C	3	5	7	kΩ
TRANSMITTER OUTPUTS					
Output Voltage Swing	All outputs loaded with 3kΩ to ground	±5	±5.4		V
Output Resistance	V_{DD} = V_L = V+ = V- = 0, V_{OUT} = ±2V	300	10M		Ω
Short-Circuit Current			±35	±60	mA
Output Leakage Current	V_{DD} = 0 or 3V to 3.6V, V_{OUT} = ±12V, transmitters disabled			±25	µA

TIMING CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, V_L = +3.3V, circuit and components of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DD} = +3.3V, T_A = +25°C.)

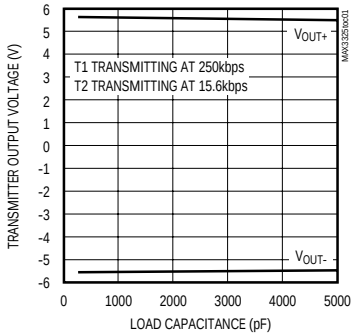
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Data Rate		R_L = 3kΩ, C_L = 1000pF, one transmitter switching	250			kbps
Receiver Propagation Delay	t_{PHL}	Receiver input to receiver output, C_L = 150pF		300		ns
	t_{PLH}			300		
Receiver Skew	$\lvert t_{PLH} - t_{PHL} \rvert$			300		ns
Transmitter Skew	$\lvert t_{PLH} - t_{PHL} \rvert$			200		ns
Transition-Region Slew Rate		V_{DD} = 3.3V, T_A = +25°C, R_L = 3kΩ to 7kΩ, C_L = 150pF to 1000pF, measured from +3V to -3V or -3V to +3V	6		30	V/µs

Note 2: Guaranteed by design and not production tested.
Note 3: No load on REG or transmitter outputs.

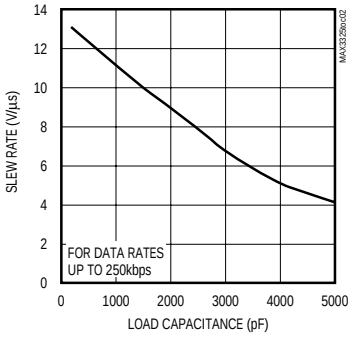
Typical Operating Characteristics

(V_{DD} = V_L = +3.3V, circuit and components of Figure 1, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

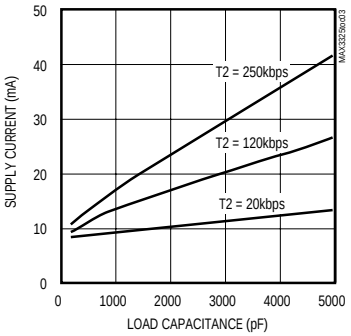
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



SLEW RATE vs. LOAD CAPACITANCE



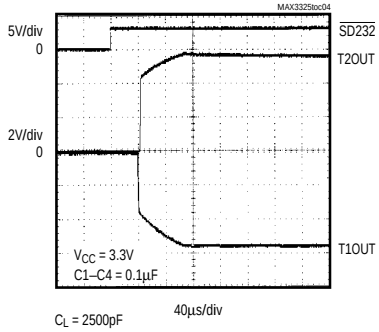
SUPPLY CURRENT vs. LOAD CAPACITANCE (T1 = 20kbps)



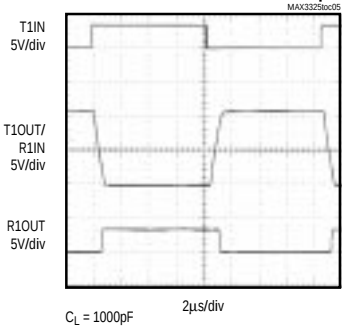
Typical Operating Characteristics (continued)

(V_{DD} = V_L = +3.3V, circuit and components of Figure 1, all transmitters loaded with 3kΩ and C_L, T_A = +25°C, unless otherwise noted.)

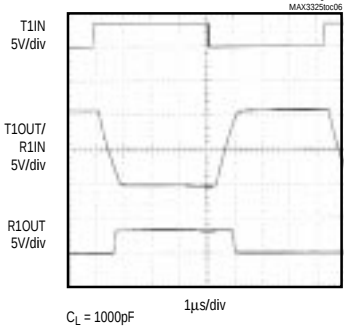
TRANSMITTER OUTPUTS EXITING SHUTDOWN OR POWERING UP



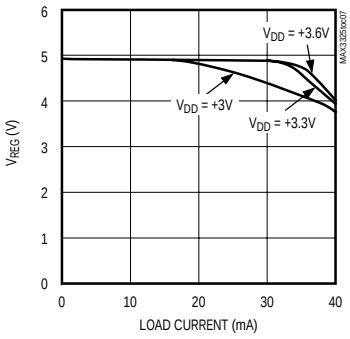
LOOPBACK WAVEFORMS AT 120kbps



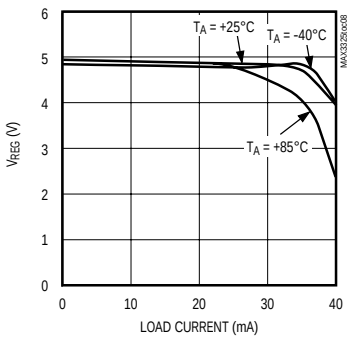
LOOPBACK WAVEFORMS AT 250kbps



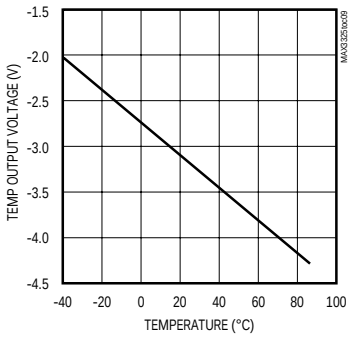
V_{REG} vs. LOAD CURRENT



V_{REG} vs. LOAD CURRENT AND TEMPERATURE



TEMP OUTPUT VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	C2+	Positive Terminal of Voltage-Inverting Charge-Pump Capacitor. Connect C2+ to C2- with a 0.22µF capacitor.
2	C2-	Negative Terminal of Voltage-Inverting Charge-Pump Capacitor. Connect C2- to C2+ with a 0.22µF capacitor.
3	V-	Output of Negative Charge Pump. Bypass V- to GND with a 0.22µF capacitor.
4, 5	R_IN	RS-232 Receiver Inputs
6, 7	R_OUT	TTL/CMOS Receiver Outputs
8	V_L	Supply Input for Receiver Outputs. Connect V_L to the system logic supply voltage.
9	LCD	Output of Negative Regulator. Connect LCD to FB with a series resistor. Bypass with a 0.47µF capacitor to GND.
10	TEMP	Output of Temperature Sensor. Connect TEMP to FB with a series resistor to compensate LCD contrast for changing temperature. Bypass TEMP with a 0.22µF capacitor to GND.
11	REF-	Output of Negative Reference, -1.2V. Bypass REF- with a 0.22µF capacitor to GND.
12	FB	Feedback Input for Negative Regulator. Regulates when FB is at zero (0).
13	REF+	Output of Positive Reference, +1.2V. Bypass REF+ with a 0.22µF capacitor to GND.
14	DAC	Output of Internal 6-Bit DAC. Connect DAC to FB with a series resistor to adjust LCD voltage.
15	$\overline{UP}$	DAC Adjust Input. A falling edge on $\overline{UP}$ increments the internal 6-bit DAC counter.
16	$\overline{DOWN}$	DAC Adjust Input. A falling edge on $\overline{DOWN}$ decrements the internal 6-bit DAC counter.
17	$\overline{SDLCD}$	Active-Low Shutdown-Control Input for Both Regulators, References, DAC, and Temperature Sensors. Drive $\overline{SDLCD}$ low to disable all analog circuitry. Drive high to enable the analog circuitry.
18	$\overline{SD232}$	Active-Low Shutdown-Control Input for Transmitter Outputs. Drive $\overline{SD232}$ low to disable the RS-232 transmitters. Drive high to enable the transmitters.
19, 20	T_IN	TTL/CMOS Transmitter Inputs
21, 22	T_OUT	RS-232 Transmitter Outputs
23	REG	Output of Positive Regulator. Bypass REG with a 4.7µF capacitor to GND.
24	C1-	Negative Terminal of Voltage-Doubling Charge-Pump Capacitor. Connect C1- to C1+ with a 0.22µF capacitor.
25	GND	Ground
26	V_{DD}	+3.0V to +3.6V Supply Voltage. Bypass V_{DD} with a 0.22µF capacitor to GND.
27	V+	Output of Positive Charge Pump. Bypass V+ to V_{DD} with a 0.22µF capacitor.
28	C1+	Positive Terminal of Voltage-Doubling Charge-Pump Capacitor. Connect C1+ to C1- with a 0.22µF capacitor.

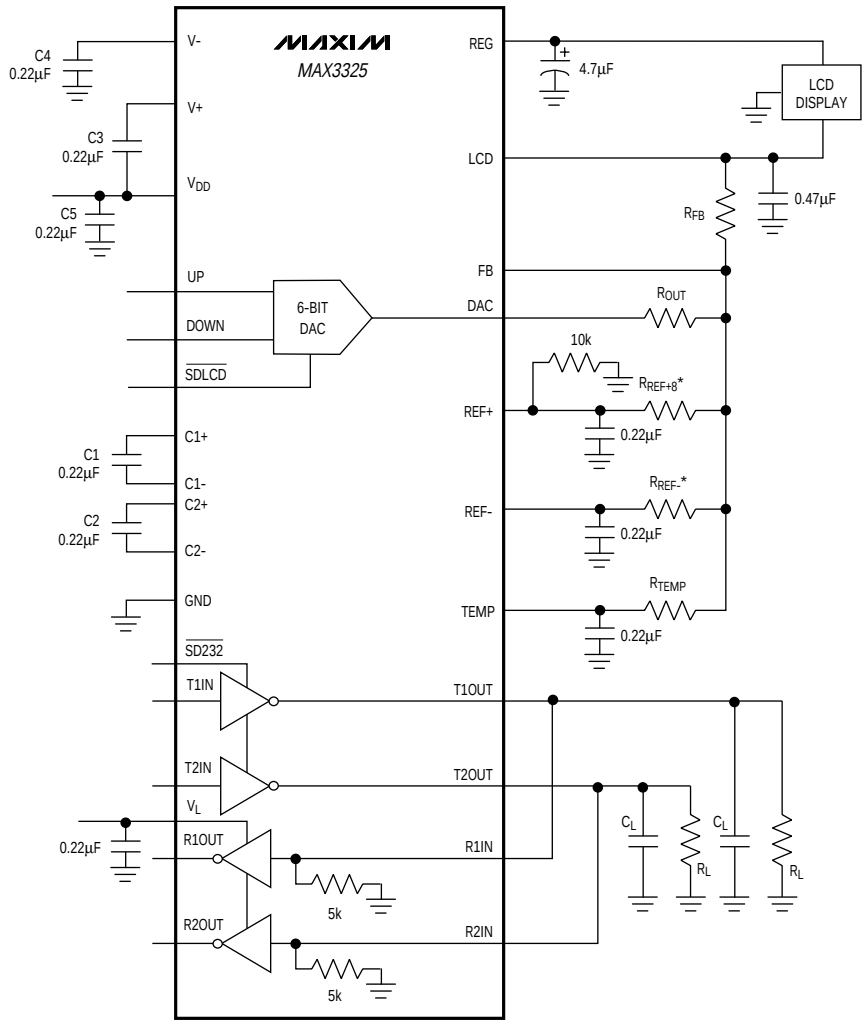


Figure 1. Application Circuit

3V Dual RS-232 Transceiver with LCD Supply and Contrast Controller

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3325's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump) over the 3.0V to 3.6V V_{DD} range. The charge pump operates in discontinuous mode; if the output voltages are less than 5.5V, the charge pump is enabled; if the output voltages exceed 5.5V, the charge pump is disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies (Figure 1).

RS-232 Transmitters

The transmitters are inverting level translators that convert logic levels to ±5.0V EIA/TIA-232 levels. The MAX3325 transmitters guarantee a 250kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™).

The MAX3325's transmitters are disabled and the outputs are forced into a high-impedance state when the RS-232 circuitry is in shutdown ($\overline{SD232}$ = low). The MAX3325 permits the outputs to be driven up to ±13V in shutdown.

The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{DD}.

RS-232 Receivers

The receivers convert RS-232 signals to logic output levels. The V_L pin controls the logic output high voltage. The receiver outputs are always active, regardless of the shutdown state.

Positive Voltage Regulator

The MAX3325 has a regulated +5V output suitable for powering +5V LCD modules or other circuits. The output of the boost charge pump is regulated with an LDO linear regulator. The REG output sources up to 11mA of current to external circuitry.

Adjustable LCD Supply

The LCD output provides a flexible output voltage to adjust the contrast of LCD modules. The output voltage range is determined by the external circuitry connected to LCD, FB, DAC, REF+ (or REF-, depending on contrast polarity). Additionally, the TEMP output can be used to automatically compensate the contrast adjustment for temperature variance.

The LCD output is a linear regulator powered by the negative charge pump. It is capable of sinking up to 3mA of current. Although the LCD regulator can be adjusted to positive voltages, it is not capable of sourcing current. A minimum output current of 100µA is required.

6-Bit DAC

The MAX3325's DAC output is an unbuffered inverted R2R structure with an output voltage range of 0 to +1.2V. The DAC output impedance is typically 50kΩ, and can be connected through a series resistor to the FB input of the LCD regulator. An internal power-on reset circuit sets the DAC to midscale on power-up.

DAC Control Inputs

The DAC code is controlled by $\overline{UP}$ and $\overline{DOWN}$ to adjust the contrast of the LCD module. These inputs are intended to interface to digital signals, but do not include debounce circuitry. See the *Applications* section. See Table 1 for the truth table.

Temperature Compensation

The MAX3325's TEMP output is used to minimize deviation in LCD contrast level due to temperature changes. The TEMP output is capable of sinking or sourcing up to 22µA to the external resistor network.

Shutdown Mode

Supply current falls below 1µA in shutdown mode ($\overline{SDLCD}$ = $\overline{SD232}$ = low). When shut down, the device's charge pumps are shut off, V+ is pulled down to V_{DD}, V- is pulled to ground, and the transmitter outputs are disabled (high impedance). The LCD section is also powered down. The REG, LCD, and both reference outputs become high impedance. The time required to exit shutdown is typically 100µs, as shown in the *Typical Operating Characteristics*. However, the TEMP output requires 50ms to fully stabilize. Connect $\overline{SDLCD}$ and $\overline{SD232}$ to V_{DD} if the shutdown mode is not used. See Table 2.

Table 1. DAC Truth Table

$\overline{UP}$	$\overline{DOWN}$	FUNCTION
0	0	DAC set to midscale
1	↓	DAC register decrements 1 count
↓	1	DAC register increments 1 count

Table 2. Shutdown Truth Table

$\overline{SDLCD}$	$\overline{SD232}$	FUNCTION
0	0	Low-power shutdown mode
1	X	LCD bias and REG outputs enabled
X	1	RS-232 transmitters enabled

X = Don't care

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Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. Ceramic chip capacitors with an X7R dielectric provide the best combination of performance, cost, and size. The charge pump requires 0.22µF capacitors for 3.3V operation. Do not use values smaller than those listed in Figure 1. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs, slightly reduces power consumption, and increases the available output current from V_{REG} and V_{LCD}. C2, C3, and C4 can be increased without changing C1's value. **However, do not increase C1 without also increasing the values of C2, C3, C4, and C5 to maintain the proper ratios.**

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperature or voltage. This is typical of Y5V and Z5U dielectric ceramic capacitors. If in doubt, use capacitors with a larger nominal value, or specify X7R dielectric. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Power-Supply Decoupling

In most circumstances, a 0.22µF V_{DD} bypass capacitor (C5) is adequate. Choosing larger values for C5 increases performance and decreases the induced ripple on the V_{DD} supply line. Note that capacitor C2, connected to V+, is returned to C5. This connection also improves the performance of the MAX3325. Locate all bypass capacitors as close as possible to the IC. Keep metal traces as wide as possible. Return all capacitor ground connections directly to a solid-copper ground plane.

Transmitter Outputs when Exiting Shutdown

The *Typical Operating Characteristics* show the MAX3325 transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately -3V.

High Data Rates

The MAX3325 maintains the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 1 shows a transmitter loopback test circuit. The *Typical Operating Characteristics* show loopback test results at 120kbps and 250kbps. For 120kbps, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For 250kbps, a single transmitter was driven at 250kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

Interconnection with Lower Logic Voltages

The MAX3325 provides a separate supply for the logic interface to optimize input and output levels. Connect V_L to the system's logic supply voltage, and bypass it with a 0.1µF capacitor to GND. If the logic supply is the same as V_{DD}, connect V_L to V_{DD}. The V_L pin can be operated from +1.8V to +5.0V to accommodate various logic levels.

Setting V_{LCD} Output Voltage

The LCD output can be configured in a variety of ways to suit the requirements of the LCD display. First, determine the nominal voltage range that the LCD will require for adequate contrast adjustment. If the display requires temperature compensation for contrast, include the TEMP output in all calculations. The output voltage is defined by:

$$V_{LCD} = -R_{FB}\left(\frac{code \cdot V_{DAC}}{\left(R_O + R_{DAC}\right)} + \frac{V_{REF+}}{R_{REF+}} + \frac{V_{REF-}}{R_{REF-}} + \frac{-3.3V - V_{TEMP} \cdot (T - 25°C)}{R_{TEMP}}\right)$$

where code is the current digital code in the DAC, and R_O is the nominal DAC output impedance (50kΩ). The other terms in the equation are due to external resistances connected to the indicated pins. A spreadsheet program is an excellent tool for helping to select components and evaluate their effect on the output voltage range.

Although the above equation has terms for both REF+ and REF- offset resistors, only one or the other is used.

Design Example

The first step in designing for a particular display is to obtain the manufacturer's device specifications for the nominal values as well as the temperature characteristics. For example, consider the Optrex DMC series of dot matrix LCD modules. The manufacturer specifies a nominal contrast bias voltage of 6V at +25°C, where bias voltage is V_{REG} - V_{LCD}. The temperature coefficient needed

to maintain the nominal contrast is -16mV/°C. In this case, data for a spread of nominal bias voltages is not available, so a range of ±1V is chosen by experimentation.

Feedback Resistor (R_{FB})

The first step in designing the MAX3325 LCD bias is to select a feedback resistor. This can be arbitrary, but values between 220kΩ to 1MΩ are a good starting point. We will choose 330kΩ. If the design can't reach its target range in later calculations, the feedback resistor can be adjusted accordingly.

DAC Output Resistor (R_{OUT})

Given the above criterion of a ±1V output range, the DAC's output should be multiplied by the ratio of the desired output swing (±1V) divided by the available output from the DAC (0 to 1.2V). Assuming that we've used a 330kΩ feedback resistor, this corresponds to a total DAC resistance of 200kΩ. Because the DAC has an intrinsic output impedance of 50kΩ, set R_{OUT} to 200kΩ - 50kΩ = 150kΩ.

Temperature Compensation Resistor (R_{TEMP})

Next, the temperature compensation resistor is selected. Because the MAX3325 regulates FB to virtual ground, adding or removing the remaining resistors in this design does not affect the transfer function set in the previous section. The TEMP output has a temperature coefficient of -17.5mV per °C, and the LCD's is -16mV/°C. To scale these two values, multiply the feedback resistor (330kΩ) by the ratio of the TEMP coefficient divided by the display's coefficient. For this example, the result is 360kΩ.

Reference Resistance ($R_{REF\_}$)

To complete the design, the DC output is biased to the final desired value at DAC midscale. Because the previous steps concentrated on the transfer function only, we now have a large offset of +1.94V. This is calculated from the entire equation, where the reference resistors are assumed to be infinite, the DAC voltage is +0.6V, and V_{TEMP} is -3.2V. Connecting a 130kΩ resistor from REF+ to FB forces V_{LCD} to -1.1V, resulting in a nominal contrast voltage (V_{REG} - V_{LCD}) of +6.1V. This is close to the target value of +6V.

Actual Performance

The graph in Figure 2 shows the actual LCD display's data curve, along with the MAX3325's performance with various DAC codes. Note that changing the DAC code does not affect the slope of the temperature compensation. If a wider scale of contrast adjustments is desired, change the DAC output resistor, and readjust the offset voltage.

Interfacing to the $\overline{UP}$ and $\overline{DOWN}$ Inputs

The $\overline{UP}$ and $\overline{DOWN}$ inputs to the MAX3325 are edge-triggered digital inputs. For proper operation, the signals must be standard logic signals. Mechanical switch outputs, (toggle or membrane types) are unsuitable and require proper debouncing before connecting to the MAX3325. The best solution is to use the MAX6817 dual switch debouncer. This sends the correct signal levels to the $\overline{UP}$ and $\overline{DOWN}$ inputs, and provides a robust interface to the switch inputs. The $\overline{UP}$ and $\overline{DOWN}$ inputs can be driven directly from a microprocessor.

System Considerations

Because the MAX3325 is the temperature transducer for the LCD bias compensation, optimal performance is obtained by placing the IC as close as possible to the LCD.

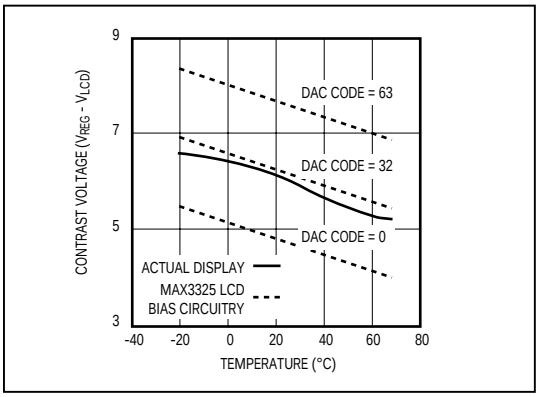
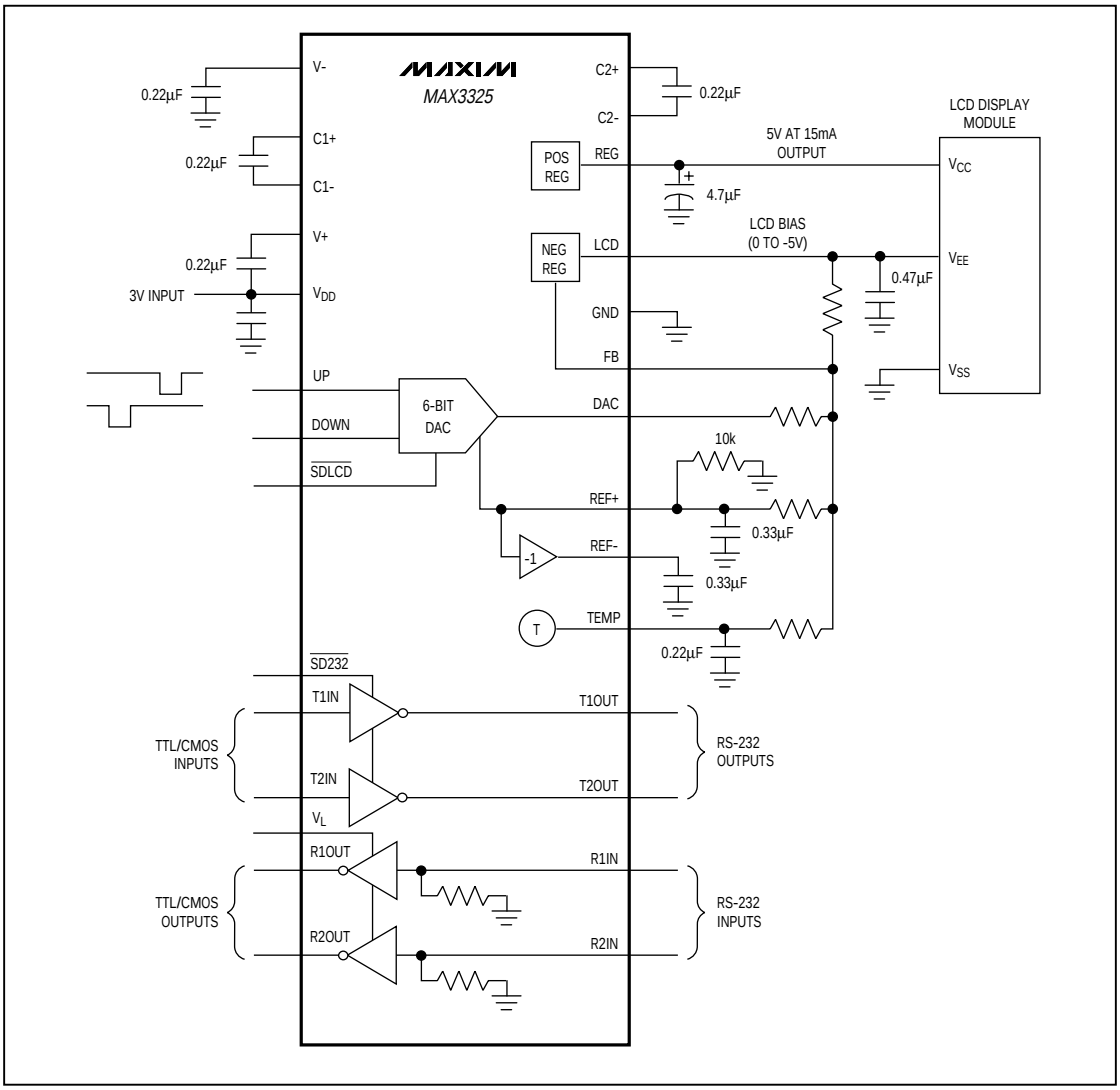


Figure 2. Design Example for Optrex DMC Display

Chip Information

TRANSISTOR COUNT: 1957

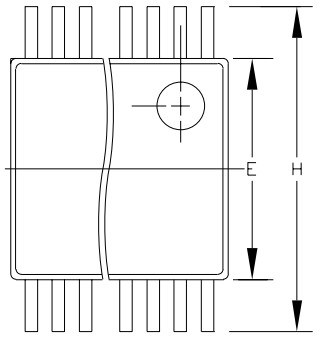
Typical Operating Circuit



3V Dual RS-232 Transceiver with LCD Supply and Contrast Controller

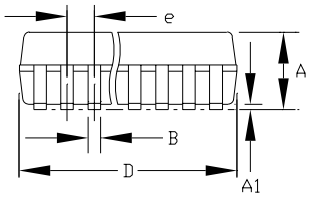
Package Information

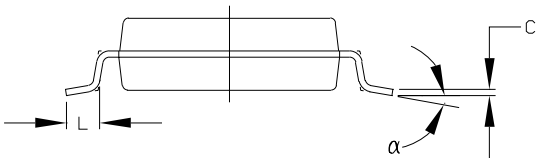
SSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 5.3X.65mm
APPROVAL | DOCUMENT CONTROL NO. 21-0056 | REV. A | 1/1