FAIRCHILD SEMICONDUCTOR®

February 2008

74LVX132
Low Voltage Quad 2-Input NAND Schmitt Trigger

Features

- Input voltage level translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

General Description

The LVX132 contains four 2-input NAND Schmitt Trigger Gates. The pin configuration and function are the same as the LVX00 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals, thus providing greater noise margins than conventional gates.

The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

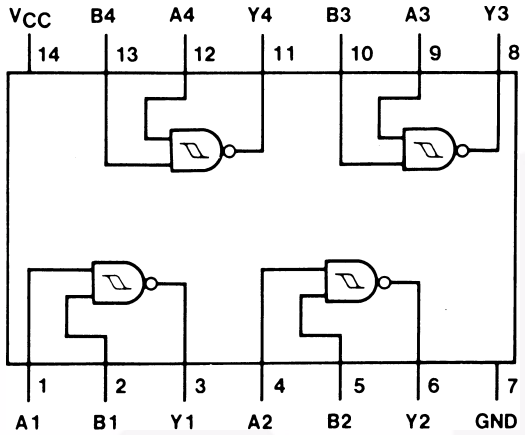
Ordering Information

Order Number	Package Number	Package Description
74LVX132M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74LVX132SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX132MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

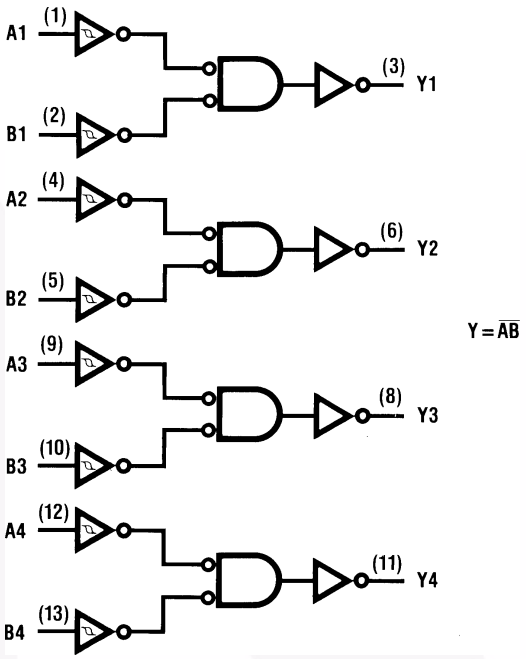
Device also available in Tape and Reel. Specify by appending suffix letter “X” to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram



Logic Diagram



Pin Description

Pin Names	Descriptions
A_n, B_n	Inputs
Y_n	Outputs

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current, V_I = –0.5V	–20mA
V_I	DC Input Voltage	–0.5V to 7V
I_{OK}	DC Output Diode Current	
	V_O = –0.5V	–20mA
	V_O = V_{CC} + 0.5V	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±25mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
P	Power Dissipation	180mW

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	2.0V to 3.6V
V_I	Input Voltage	0V to 5.5V
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta t / \Delta V$	Input Rise and Fall Time	0ns/V to 100ns/V

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_t+	Positive Threshold	3.0				2.2		2.2	V
V_t–	Negative Threshold	3.0		0.9			0.9		V
V_H	Hysteresis	3.0		0.3		1.2	0.3	1.2	V
V_{OH}	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –50µA	1.9	2.0		1.9		V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –50µA	2.9	3.0		2.9		
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OH} = –4mA	2.58			2.48		
V_{OL}	LOW Level Output Voltage	2.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 50 µA		0.0	0.1		0.1	V
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 50 µA		0.0	0.1		0.1	
		3.0	$V_{IN} = V_{IL}$ or V_{IH}, I_{OL} = 4 mA			0.36		0.44	
I_{IN}	Input Leakage Current	3.6	V_{IN} = 5.5V or GND			±0.1		±1.0	µA
I_{CC}	Quiescent Supply Current	3.6	$V_{IN} = V_{CC}$ or GND			2.0		20	µA

Noise Characteristics[2]

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = 25°C		Units
				Typ.	Limit	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3	50	0.3	0.5	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3	50	–0.3	–0.5	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	3.3	50		2.0	V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	3.3	50		0.8	V

Note:

2. Input $t_r = t_f$ = 3ns

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	C_L (pF)	T_A = +25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t_{PLH}, t_{PHL}	Propagation Delay Time	2.7	15		7.0	11.5	1.0	13.0	ns
			50		10.5	16.0	1.0	18.7	
		3.3 ± 0.3	15		6.1	10.6	1.0	12.5	
			50		9.0	15.4	1.0	17.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew(3)	2.7	50			1.5		1.5	ns
		3.3				1.5		1.5	

Note:

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} – t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} – t_{PHLn}|$

Capacitance

Symbol	Parameter	T_A = +25°C			T_A = –40°C to +85°C		Units
		Min.	Typ.	Max.	Min.	Max.	
C_{IN}	Input Capacitance		4	10		10	pF
C_{PD}	Power Dissipation Capacitance(4)		18				pF

Note:

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

   Average operating current can be obtained by the eqation: $I_{CC(opr.)} = \dfrac{C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}}{6 \text{ (per Gate)}}$

Physical Dimensions

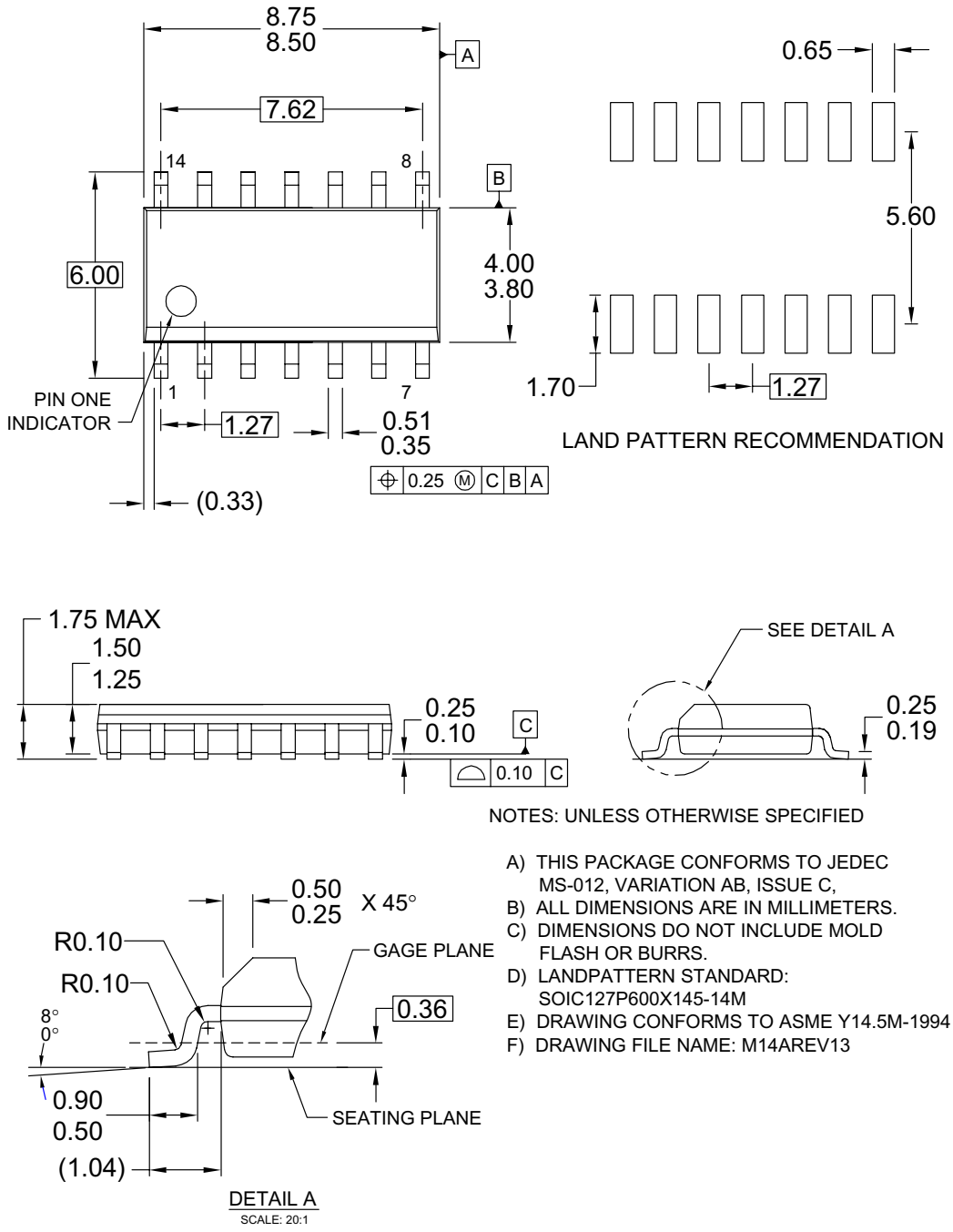


Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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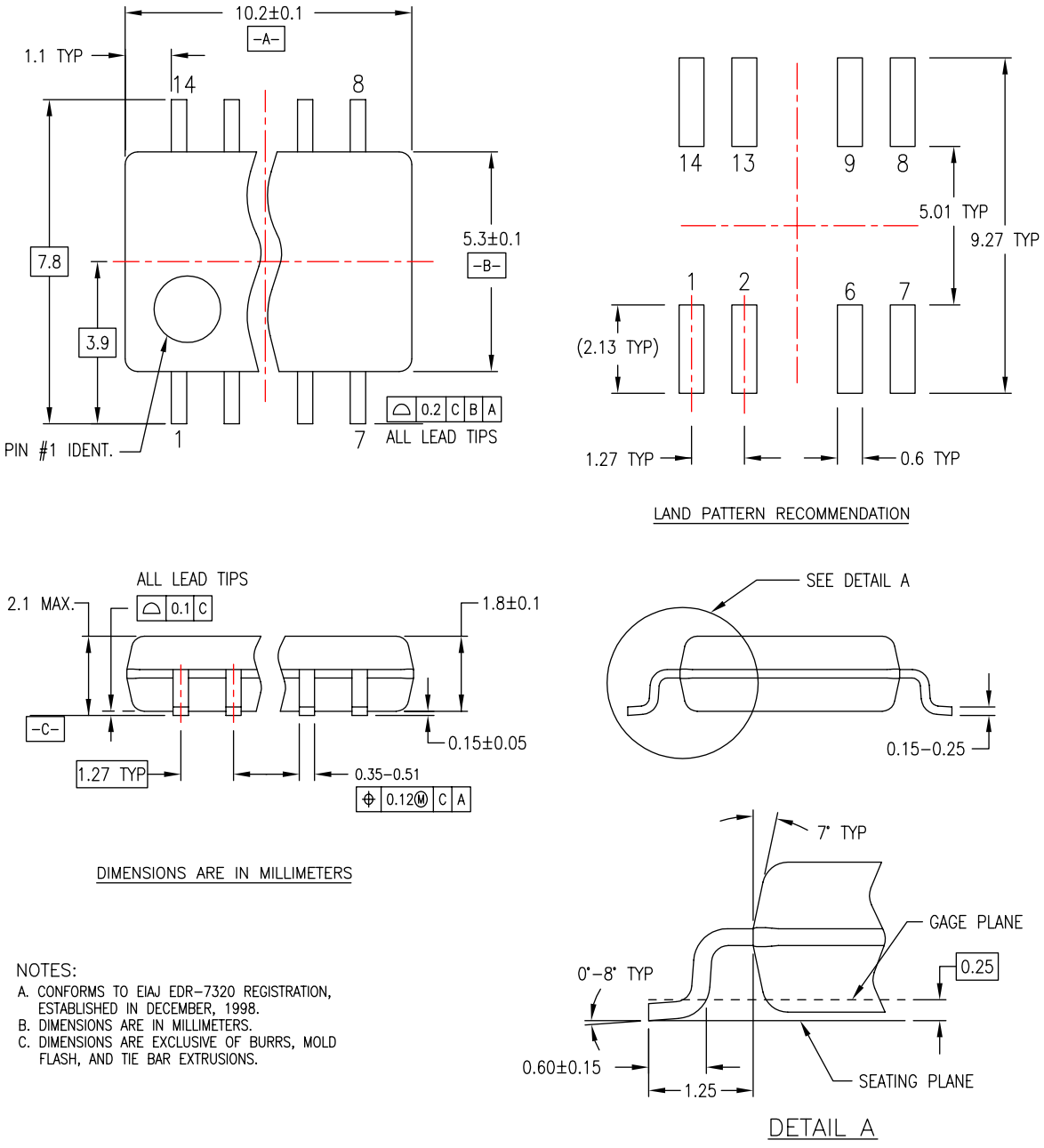
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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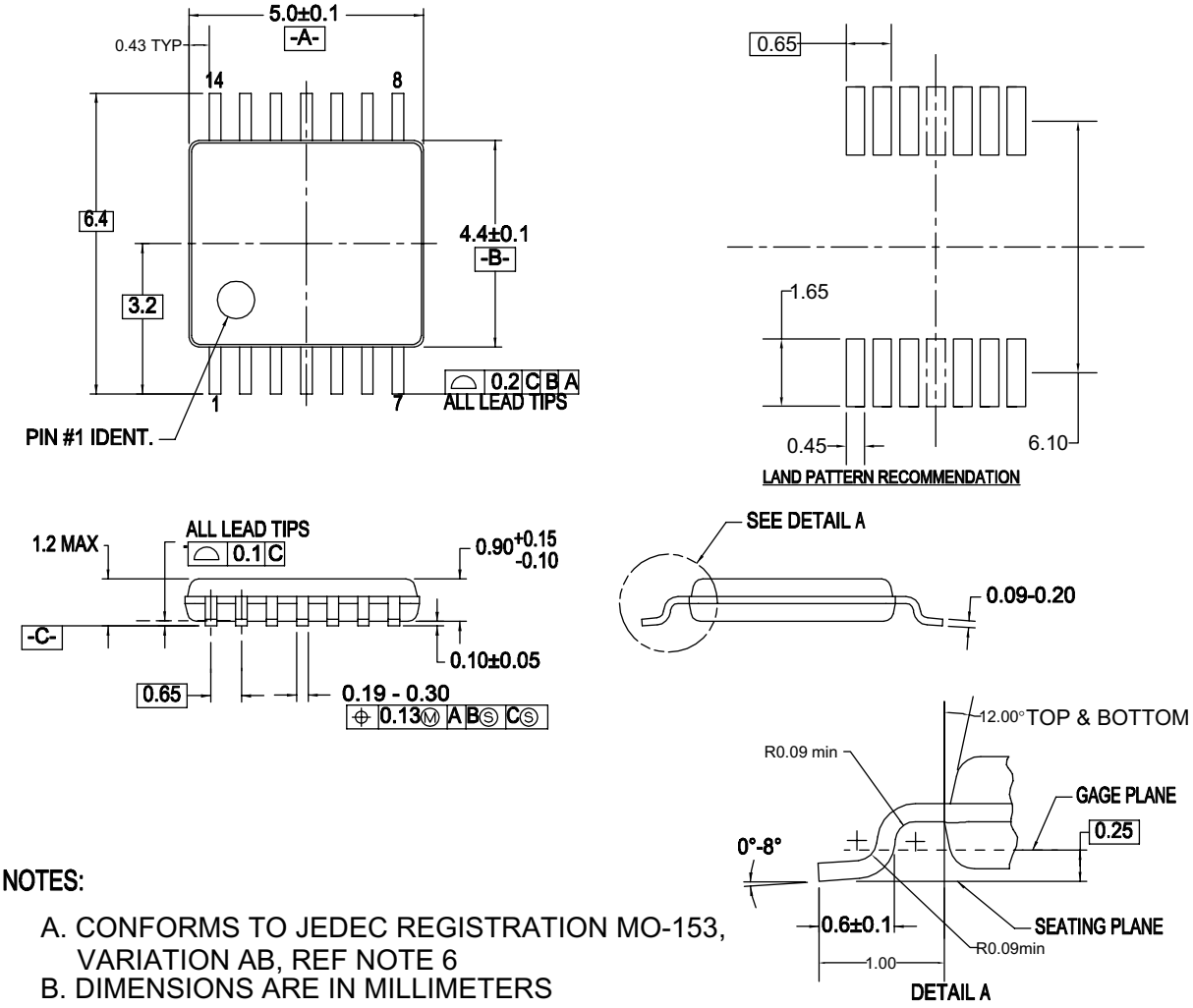
Physical Dimensions (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

E. LANDPATTERN STANDARD: SOP65P640X110-14M

F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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