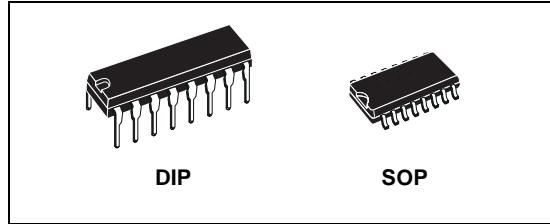


## MULTIFUNCTION EXPANDABLE 8-INPUT GATE

- THREE STATE OUTPUT
- MULTIPLE LOGIC FUNCTIONS AVAILABLE IN ONE PACKAGE
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_I = 100\text{nA}$  (MAX) AT  $V_{DD} = 18\text{V}$   $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



## ORDER CODES

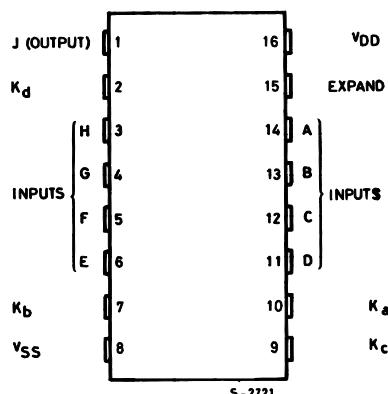
PACKAGE	TUBE	1 & R
DIP	HCF4048BEY	
SOP	HCF4048BM1	HCF4048M013TR

## DESCRIPTION

HCF4048B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4048B is an 8-input gate having four control inputs. Three binary control inputs  $K_a$ ,  $K_b$ , and  $K_c$  provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth control input  $K_d$  provides the user with a 3 state output. When control input  $K_d$  is high

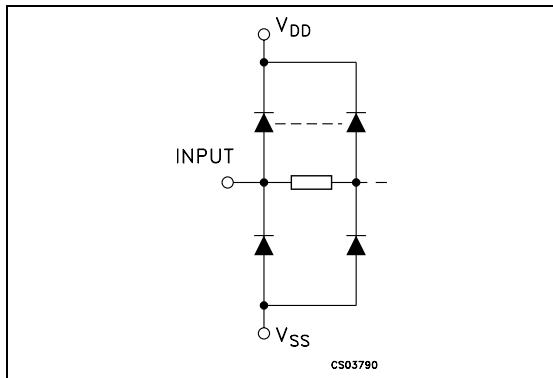
the output is either a logic 1 or a logic 0 depending on the inner states. When control input  $K_d$  is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line. In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one HCF4048B. For example, two HCF4048Bs can be cascaded to provide a 16 input multifunction gate. When the EXPAND input is not used, it should be connected to  $V_{SS}$ .

## PIN CONNECTION



# HCF4048B

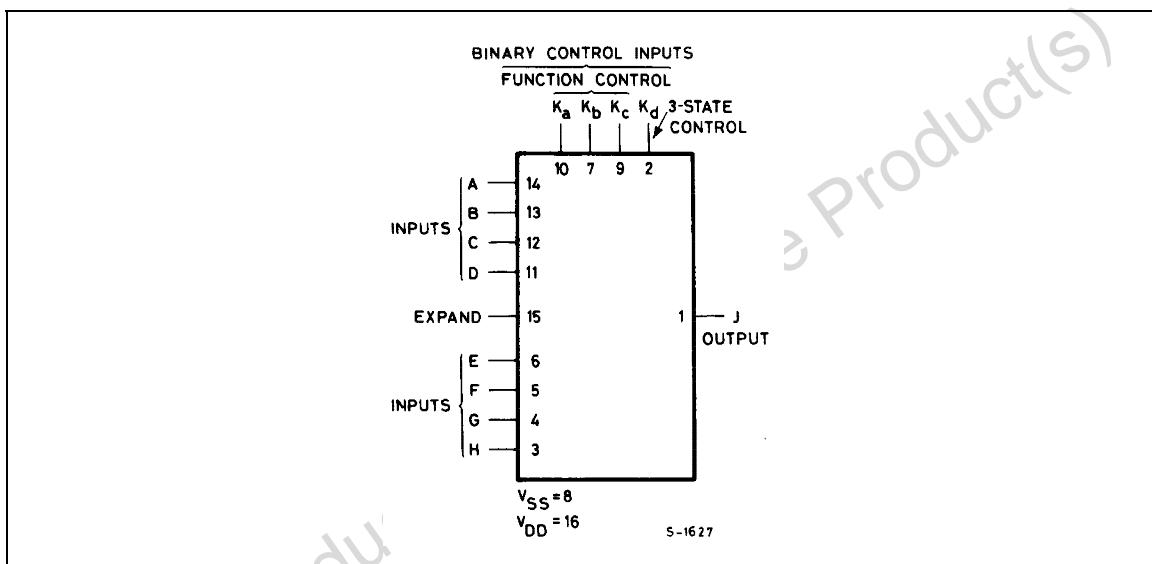
## INPUT EQUIVALENT CIRCUIT



## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
14, 13, 12, 11	A, B, C, D	Data Inputs
6, 5, 4, 3	E, F, G, H	Data Inputs
10, 7, 9	K <sub>a</sub> , K <sub>b</sub> , K <sub>c</sub>	Function Control Inputs
2	K <sub>d</sub>	3-State Control Inputs
1	J	Data Output
15	EXPAND	Expand Input
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

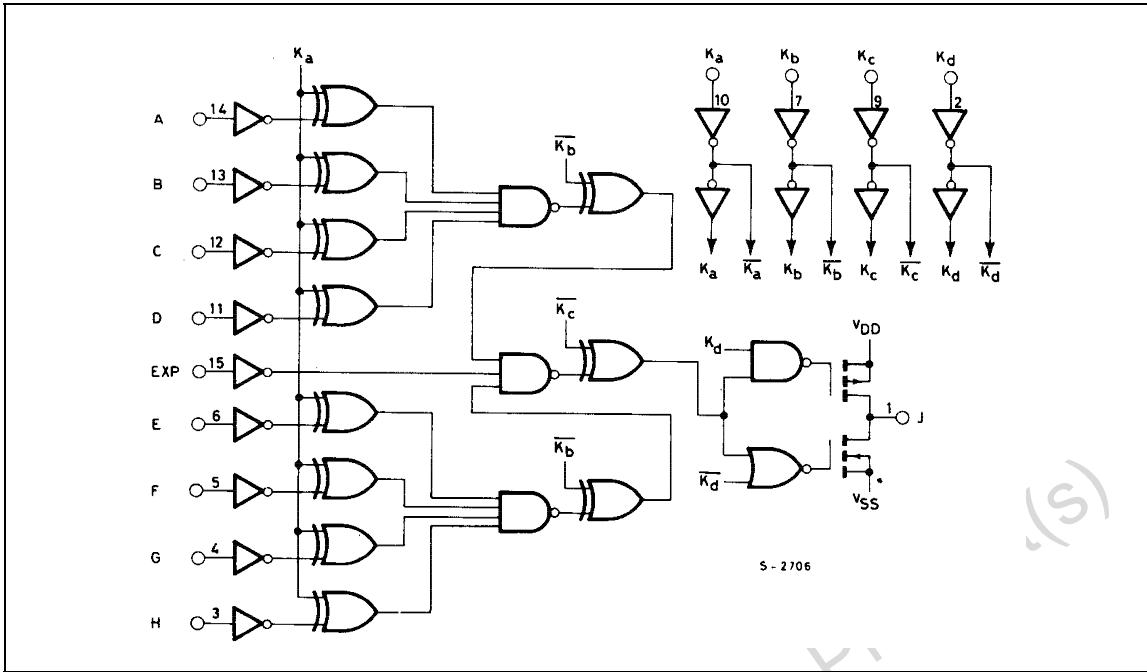
## FUNCTIONAL DIAGRAM



## TRUTH TABLE

Output Function	Boolean Expression	K <sub>a</sub>	K <sub>b</sub>	K <sub>c</sub>	Unused Input
NOR	J = $\overline{A + B + C + D + E + F + G + H}$	0	0	0	V <sub>SS</sub>
OR	J = $A + B + C + D + E + F + G + H$	0	0	1	V <sub>SS</sub>
OR/AND	J = $(A + B + C + D) \bullet (E + F + G + H)$	0	1	0	V <sub>SS</sub>
OR/NAND	J = $\overline{(A + B + C + D) \bullet (E + F + G + H)}$	0	1	1	V <sub>SS</sub>
AND	J = ABCDEFGH	1	0	0	V <sub>DD</sub>
NAND	J = $\overline{ABCDEFGH}$	1	0	1	V <sub>DD</sub>
AND/NOR	J = $\overline{ABCD} + EFGH$	1	1	0	V <sub>DD</sub>
AND/OR	J = $ABCD + EFGH$	1	1	1	V <sub>DD</sub>
K <sub>d</sub> = 1 - NORMAL INVERTER ACTION					
K <sub>d</sub> = 0 - HIGH IMPEDANCE OUTPUT					

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

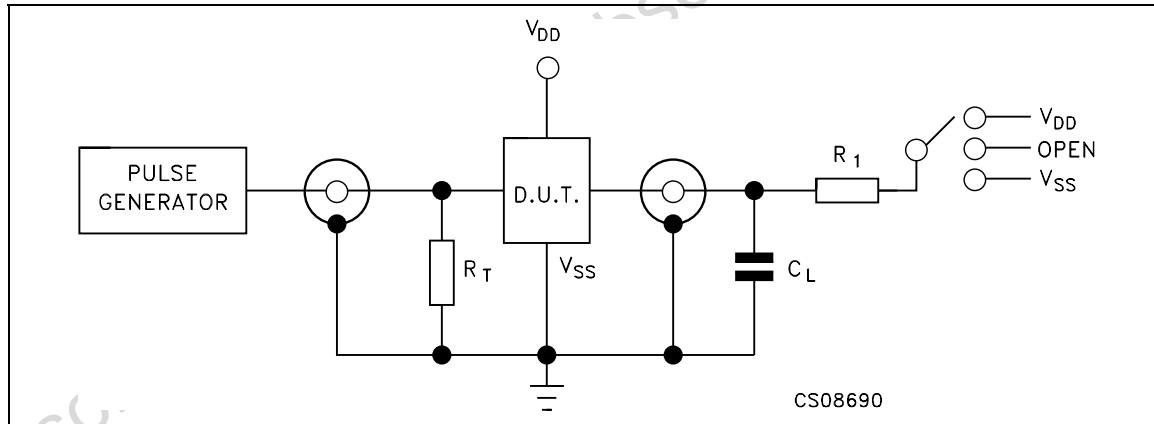
## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit		
		$V_I$ (V)	$V_O$ (V)	$I_{OL}$ ( $\mu$ A)	$V_{DD}$ (V)	$T_A = 25^\circ C$			$-40 \text{ to } 85^\circ C$		$-55 \text{ to } 125^\circ C$			
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
$I_L$	Quiescent Current	0/5			5		0.01	0.25		7.5		7.5	$\mu A$	
		0/10			10		0.01	0.5		15		15		
		0/15			15		0.01	1		30		30		
		0/20			20		0.02	5		150		150		
$V_{OH}$	High Level Output Voltage	0/5	<1	5	4.95				4.95		4.95		V	
		0/10	<1	10	9.95				9.95		9.95			
		0/15	<1	15	14.95				14.95		14.95			
$V_{OL}$	Low Level Output Voltage	5/0	<1	5		0.05				0.05		0.05	V	
		10/0	<1	10		0.05				0.05		0.05		
		15/0	<1	15		0.05				0.05		0.05		
$V_{IH}$	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V	
			1/9	<1	10	7			7		7			
			1.5/13.5	<1	15	11			11		11			
$V_{IL}$	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V	
			9/1	<1	10			3		3		3		
			13.5/1.5	<1	15			4		4		4		
$I_{OH}$	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		mA	
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36			
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9			
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4			
$I_{OL}$	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA	
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9			
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4			
$I_I$	Input Leakage Current	0/18	Any Input			18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu A$
$I_{OZ}$	3-State Output Current	0/18	Any Input			18		$\pm 10^{-4}$	$\pm 0.4$		$\pm 1$		$\pm 12$	$\mu A$
$C_I$	Input Capacitance		Any Input					5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with  $V_{DD}=5V$ , 2V min. with  $V_{DD}=10V$ , 2.5V min. with  $V_{DD}=15V$

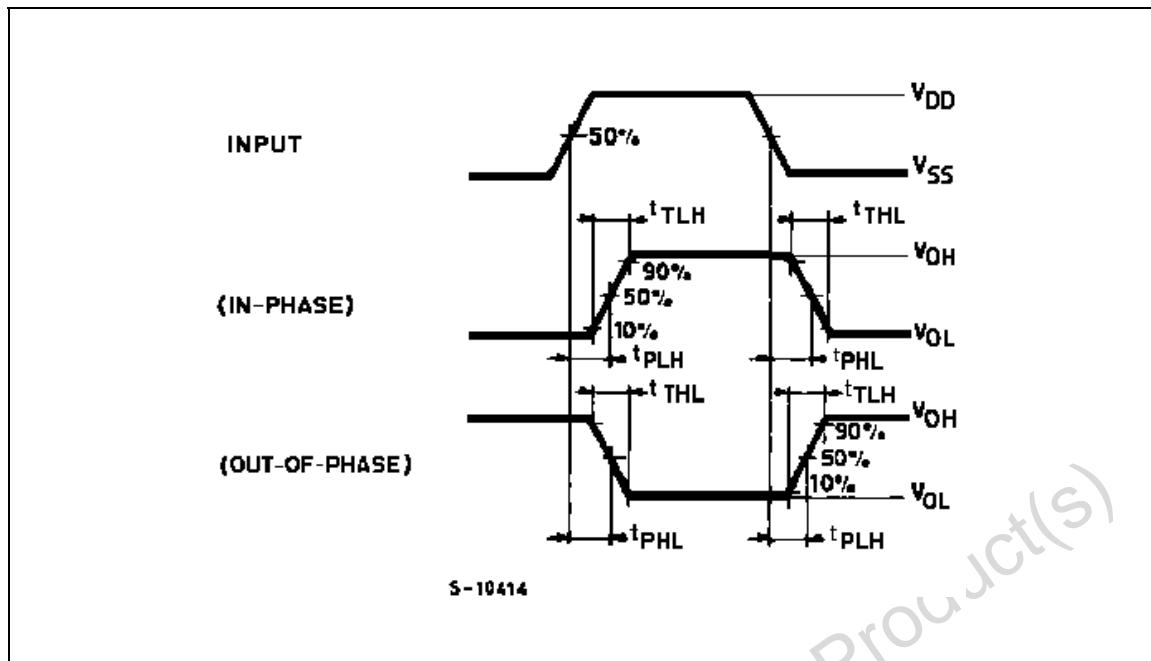
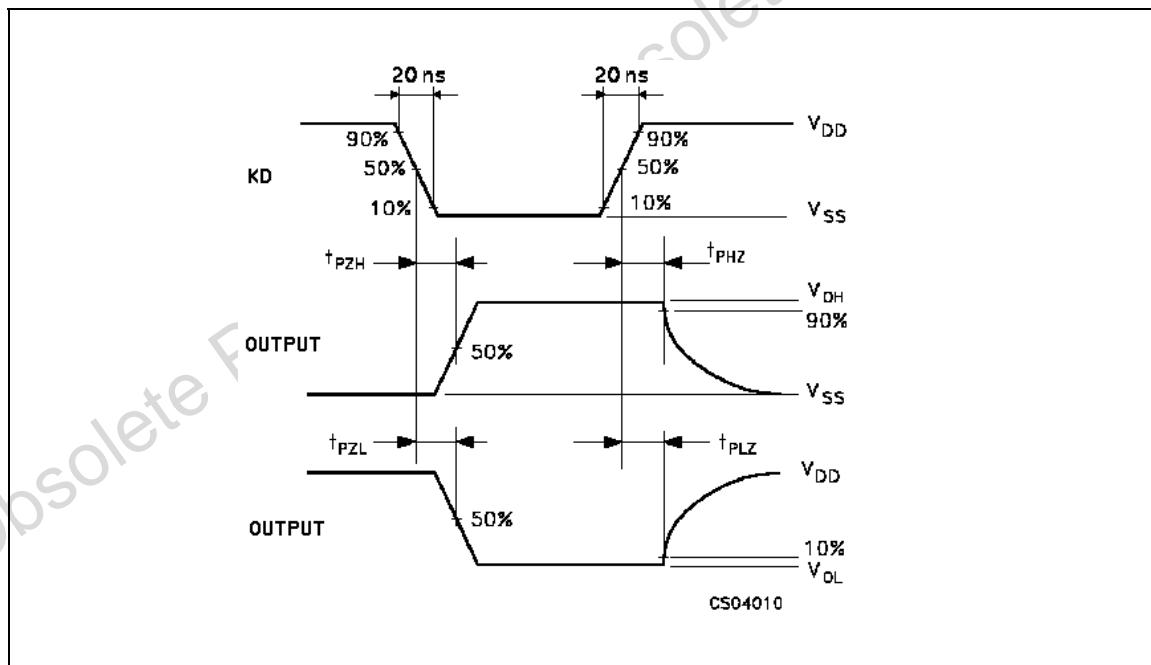
**DYNAMIC ELECTRICAL CHARACTERISTICS ( $T_{amb} = 25^\circ C$ ,  $C_L = 50pF$ ,  $R_L = 200K\Omega$ ,  $t_r = t_f = 20 ns$ )**

Symbol	Parameter	Test Condition			Value (*)		Unit	
		$V_{DD}$ (V)			Min.	Typ.		
$t_{PHL}, t_{PLH}$	Propagation Delay Time Inputs to Output and $K_a$ to Output	5				300	600	ns
		10				150	300	
		15				120	240	
	Propagation Delay Time $K_b$ to Output	5				225	450	ns
		10				85	170	
		15				55	110	
	Propagation Delay Time $K_c$ to Output	5				140	280	ns
		10				50	100	
		15				40	80	
	Propagation Delay Time EXPAND Input to Output	5				190	380	ns
		10				90	180	
		15				65	130	
$t_{PHZ}, t_{PLZ}$ $t_{PZH}, t_{PZL}$	3 - State Propagation Delay Time $K_d$ to Output	5	RL = 1KΩ			80	160	ns
		10				35	70	
		15				25	50	
$t_{TLH}, t_{THL}$	Output Transition Time	5				100	200	ns
		10				50	100	
		15				40	80	
3-State Output Capacitance						5	10	pF

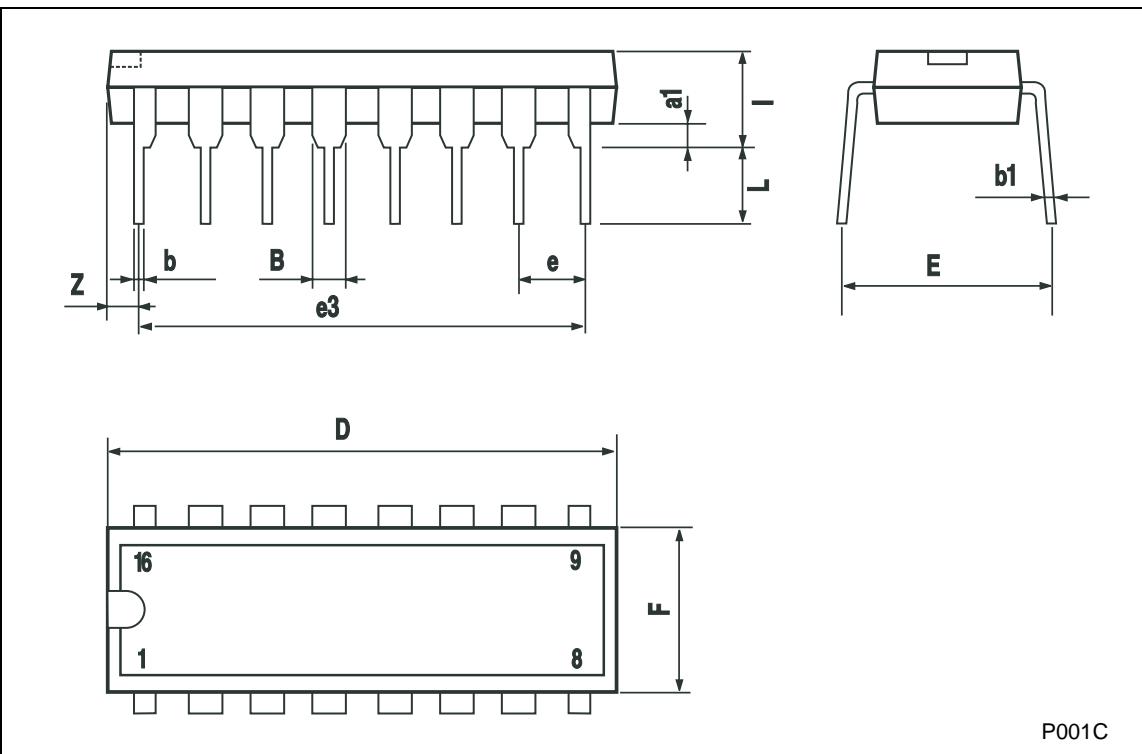
( \*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/ $^\circ C$ .**TEST CIRCUIT**

TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	$V_{DD}$
$t_{PZH}, t_{PHZ}$	$V_{SS}$

 $C_L = 50pF$  or equivalent (includes jig and probe capacitance) $R_1 = 200K\Omega$  $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

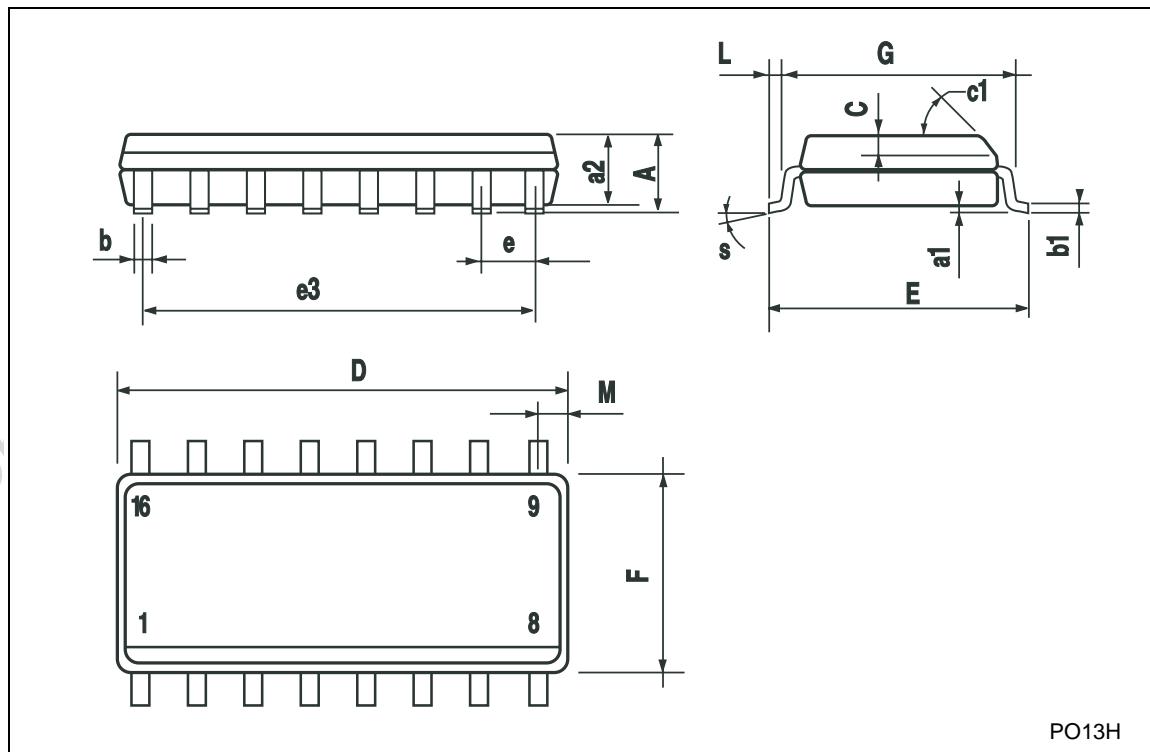
**WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)****WAVEFORM 2 : OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)**

Plastic DIP-16 (0.25) MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45° (typ.)				
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S		8° (max.)				





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