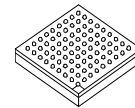




MCIMX6SxAxxxxxB
MCIMX6UxAxxxxxB

i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors



Package Information
Plastic Package
BGA Case 2240 21 x 21 mm, 0.8 mm pitch

Ordering Information

See [Table 1 on page 3](#)

1 Introduction

The i.MX 6Solo/6DualLite automotive and infotainment processors represent Freescale Semiconductor's latest achievement in integrated multimedia-focused products offering high-performance processing with a high degree of functional integration. These processors are designed considering the needs of the growing automotive infotainment, telematics, HMI, and display-based cluster markets.

The processors feature Freescale's advanced implementation of single/dual ARM Cortex™-A9 core, which operates at speeds of up to 800 MHz. They include 2D and 3D graphics processors, 1080p video processing, and integrated power management. Each processor provides a 32/64-bit DDR3/LVDDR3/LPDDR2-800 memory interface and a number of other interfaces for connecting peripherals,

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such as WLAN, Bluetooth™, GPS, hard drive, displays, and camera sensors.

The i.MX 6Solo/6DualLite processors are specifically useful for applications such as:

- Automotive navigation and entertainment
- Graphics rendering for Human Machine Interfaces (HMI)
- High-performance speech processing with large databases
- Audio playback
- Video processing and display

The i.MX 6Solo/6DualLite processors have some very exciting features, for example:

- **Multilevel memory system**—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, low voltage DDR3, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4.
- **Smart speed technology**—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- **Dynamic voltage and frequency scaling**—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- **Multimedia powerhouse**—The multimedia performance of each processor is enhanced by a multilevel cache system, Neon MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), and a programmable smart DMA (SDMA) controller.
- **Powerful graphics acceleration**—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- **Interface flexibility**—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller, and a variety of other popular interfaces (such as UART, I²C, and I²S serial audio, and PCIe-II).
- **Automotive environment support**—Each processor includes interfaces, such as two CAN ports, an MLB150/50 port, an ESAI audio interface, and an asynchronous sample rate converter for multichannel/multisource audio.
- **Advanced security**—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features will be discussed in detail in the *i.MX 6Solo/6DualLite Security Reference Manual* (to be released soon).

- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

1.1 Ordering Information

Table 1 shows the orderable part numbers covered by this datasheet. Table 1 does not include all possible orderable part numbers. The latest part numbers are available on the web page freescale.com/imx6series. If the desired part number is not listed in Table 1, or there may be any questions about available parts, see the web page freescale.com/imx6series or contact a Freescale representative.

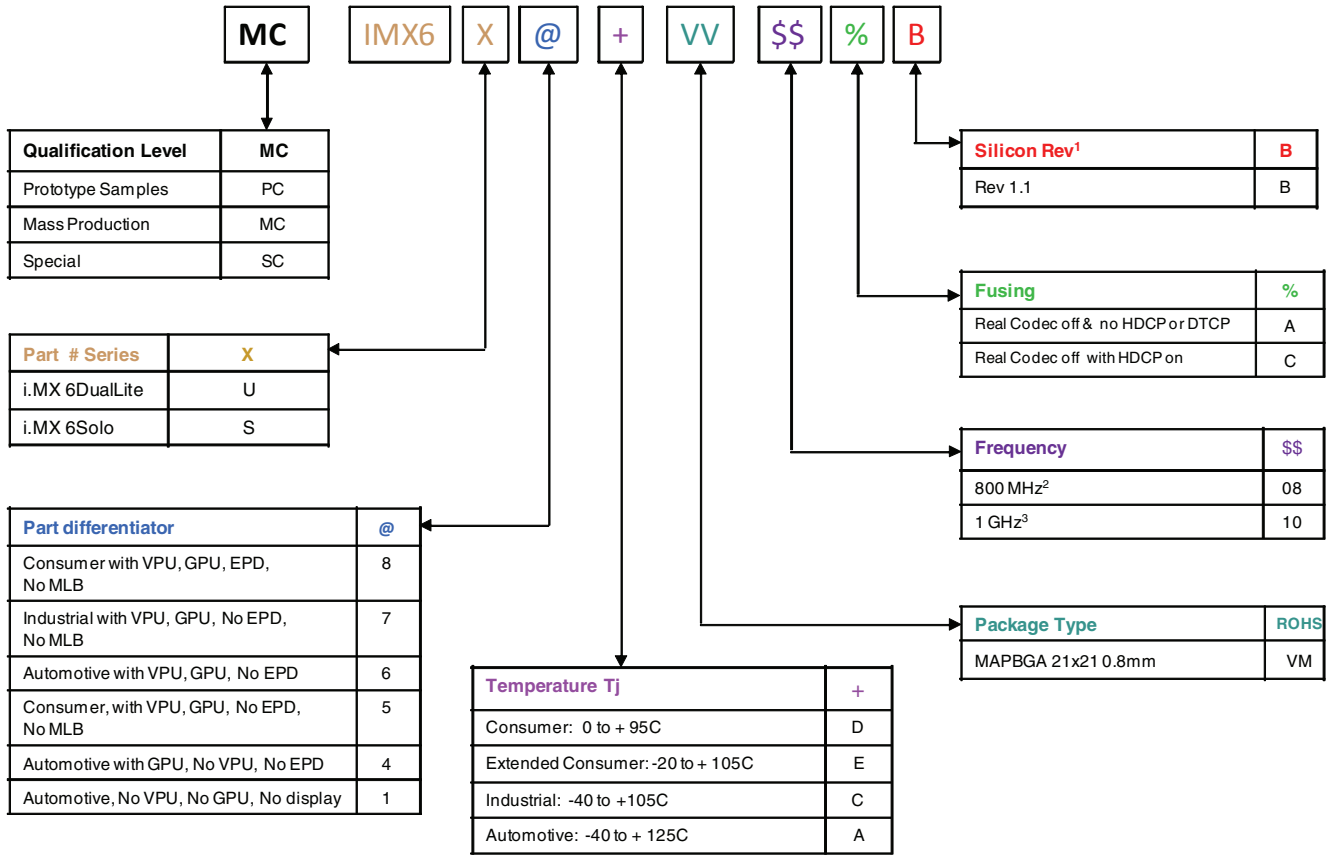
Table 1. Orderable Part Numbers

Part Number	Solo/DualLite CPU	Options	Speed Grade	Temperature Grade	Package
MCIMX6U6AVM08AB	i.MX 6DualLite	With VPU, GPU, no EPD	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U4AVM08AB	i.MX 6DualLite	With GPU, no VPU, no EPD	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6U1AVM08AB	i.MX 6DualLite	no GPU, no VPU, no display	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S6AVM08AB	i.MX 6Solo	With VPU, GPU, no EPD	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S4AVM08AB	i.MX 6Solo	With GPU, no VPU, no EPD	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA
MCIMX6S1AVM08AB	i.MX 6Solo	no GPU, no VPU, no display	800 MHz	Automotive	21 mm x 21 mm, 0.8 mm pitch, MAPBGA

Figure 1 describe the part number nomenclature so that the users can identify the characteristics of the specific part number they have (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which datasheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors datasheet (IMX6SDLAEC) covers parts listed with an “A (Automotive temp)”
- The i.MX 6Solo/6DualLite Applications Processors for Consumer Products datasheet (IMX6SDLCEC) covers parts listed with a “D (Consumer temp)” or “E (Extended Consumer temp)”
- The i.MX 6Solo/6DualLite Applications Processors for Industrial Products datasheet (IMX6SDLIEC) covers parts listed with “C (Industrial temp)”

Ensure to have the proper datasheet for specific part by verifying the temperature grade (junction) field and matching it to the proper datasheet. If there will be any questions, visit see the web page freescale.com/imx6series or contact a Freescale representative for details.



1. See the [freescale.com\imx6series](http://freescale.com/imx6series) Web page for latest information on the available silicon revision.
2. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 792 MHz.
3. If a 24 MHz input clock is used (required for USB), the maximum SoC speed is limited to 996 MHz.

Figure 1. Part Number Nomenclature—i.MX 6DualLite and 6Solo

1.2 Features

The i.MX 6Solo/6DualLite processors are based on ARM Cortex-A9 MPCore™ Platform, which has the following features:

- The i.MX 6Solo supports single ARM Cortex-A9 MPCore (with TrustZone)
- The i.MX 6DualLite supports dual ARM Cortex-A9 MPCore (with TrustZone)
- The core configuration is symmetric, where each core includes:
 - 32 KByte L1 Instruction Cache
 - 32 KByte L1 Data Cache
 - Private Timer and Watchdog
 - Cortex-A9 NEON MPE (Media Processing Engine) Co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer

- Snoop Control Unit (SCU)
- 512 KB unified I/D L2 cache:
 - Used by one core in i.MX 6Solo
 - Shared by two cores in i.MX 6DualLite
- Two Master AXI bus interfaces output of L2 cache
- Frequency of the core (including Neon and L1 cache), as per [Table 9, "Operating Ranges,"](#) on page 24.
- NEON MPE coprocessor
 - SIMD Media Processing Architecture
 - NEON register file with 32x64-bit general-purpose registers
 - NEON Integer execute pipeline (ALU, Shift, MAC)
 - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
 - NEON load/store and permute pipeline

The memory system consists of the following components:

- Level 1 Cache—32 KB Instruction, 32 KB Data cache per core
- Level 2 Cache—Unified instruction and data (512 KB)
- On-Chip Memory:
 - Boot ROM, including HAB (96 KB)
 - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
 - Secure/non-secure RAM (16 KB)
- External memory interfaces: The i.MX 6Solo/6DualLite processors support latest, high volume, cost effective handheld DRAM, NOR, and NAND Flash memory standards.
 - 16/32-bit LP-DDR2-800, 16/32-bit DDR3-800 and LV-DDR3-800 in i.MX 6Solo; 16/32/64-bit LP-DDR2-800, 16/32/64-bit DDR3-800 and LV-DDR3-800, supporting DDR interleaving mode for 2x32 LPDDR2-800 in i.MX 6DualLite
 - 8-bit NAND-Flash, including support for Raw MLC/SLC, 2 KB, 4 KB, and 8 KB page size, BA-NAND, PBA-NAND, LBA-NAND, OneNAND™ and others. BCH ECC up to 40 bit.
 - 16/32-bit NOR Flash. All WEIMv2 pins are muxed on other interfaces.
 - 16/32-bit PSRAM, Cellular RAM

Each i.MX 6Solo/6DualLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total four interfaces available. Total raw pixel rate of all interfaces is up to 450 Mpixels/sec, 24 bpp. Up to two interfaces may be active in parallel.
 - One Parallel 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz or dual HD1080 and WXGA at 60 Hz)
 - LVDS serial ports—One port up to 165 Mpixels/sec or two ports up to 85 MP/sec (for example, WUXGA at 60 Hz) each
 - HDMI 1.4 port

- MIPI/DSI, two lanes at 1 Gbps
- Camera sensors:
 - Two parallel Camera ports (up to 20 bit and up to 240 MHz peak)
 - MIPI CSI-2 Serial port, supporting from 80 Mbps to 1 Gbps speed per data lane. The CSI-2 Receiver core can manage one clock lane and up to two data lanes. Each i.MX 6Solo/6DualLite processor has two lanes.
- Expansion cards:
 - Four MMC/SD/SDIO card ports all supporting:
 - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
 - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
- USB:
 - One high speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
 - Three USB 2.0 (480 Mbps) hosts:
 - One HS host with integrated High Speed Phy
 - Two HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Expansion PCI Express port (PCIe) v2.0 one lane
 - PCI Express (Gen 2.0) dual mode complex, supporting Root complex operations and Endpoint operations. Uses x1 PHY configuration.
- Miscellaneous IPs and interfaces:
 - Three I2S/SSI/AC97, up to 1.4 Mbps each
 - Enhanced Serial Audio Interface (ESAI), up to 1.4 Mbps per channel
 - Five UARTs, up to 4.0 Mbps each:
 - Providing RS232 interface
 - Supporting 9-bit RS485 multidrop mode
 - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
 - Four eCSPI (Enhanced CSPI)
 - Four I²C, supporting 400 kbps
 - Gigabit Ethernet Controller (IEEE1588 compliant), 10/100/1000¹ Mbps
 - Four Pulse Width Modulators (PWM)
 - System JTAG Controller (SJC)
 - GPIO with interrupt capabilities
 - 8x8 Key Pad Port (KPP)
 - Sony Philips Digital Interconnect Format (SPDIF), Rx and Tx

1. The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).

- Two Controller Area Network (FlexCAN), 1 Mbps each
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)
- MLB (MediaLB) provides interface to MOST Networks (MOST25, MOST50, MOST150) with the option of DTCP cipher accelerator

The i.MX 6Solo/6DualLite processors integrate advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use SW State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6Solo/6DualLite processors use dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6Solo/6DualLite processors incorporate the following hardware accelerators:

- VPU—Video Processing Unit
- IPUv3H—Image Processing Unit version 3H
- GPU3Dv5—3D Graphics Processing Unit (OpenGL ES 2.0) version 5
- GPU2Dv2—2D Graphics Processing Unit (BitBlt)
- ASRC—Asynchronous Sample Rate Converter

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, etc.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- CAAM—Cryptographic Acceleration and Assurance Module, containing cryptographic and hash engines, 16 KB secure RAM, and True and Pseudo Random Number Generator (NIST certified).
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSES and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

NOTE

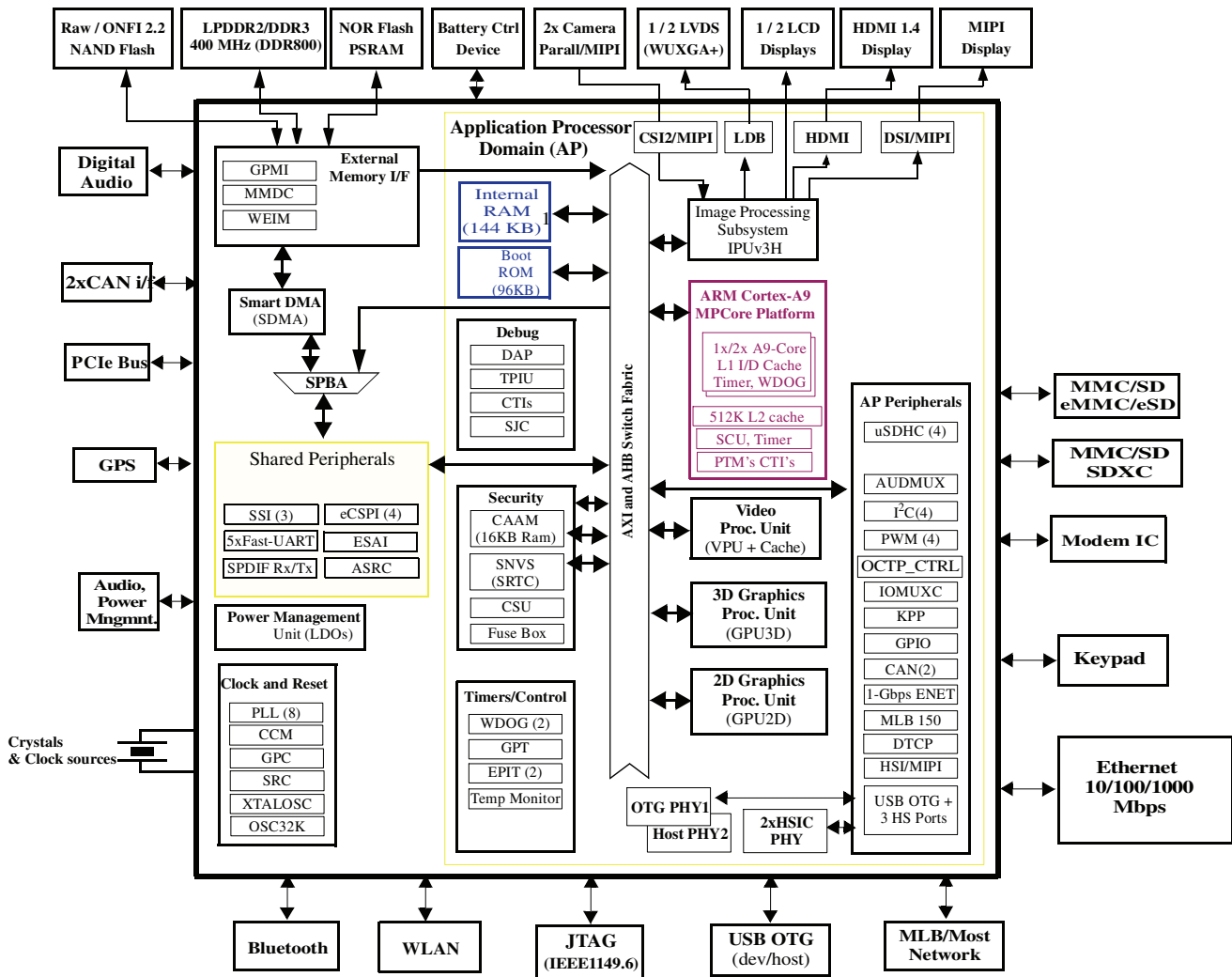
The actual feature set depends on the part numbers as described in [Table 1, "Orderable Part Numbers," on page 3](#). Functions, such as video hardware acceleration, and 2D and 3D hardware graphics acceleration may not be enabled for specific part numbers.

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6Solo/6DualLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6Solo/6DualLite processor system.



¹ 144 KB RAM including 16 KB RAM inside the CAAM.

² For i.MX 6Solo, there is only one A9-core platform in the chip; for i.MX 6DualLite, there are two A9-core platforms.

Figure 2. i.MX 6Solo/6DualLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

3 Modules List

The i.MX 6Solo/6DualLite processors contain a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6Solo/6DualLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
ARM	ARM Platform	ARM	The ARM Core Platform includes 1x (Solo) Cortex-A9 core for i.MX 6Solo and 2x (Dual) Cortex-A9 cores for i.MX 6DualLite. It also includes associated sub-blocks, such as the Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, watchdog, and CoreSight debug modules.
APBH-DMA	NAND Flash and BCH ECC DMA controller	System Control Peripherals	DMA controller used for GPMI2 operation
ASRC	Asynchronous Sample Rate Converter	Multimedia Peripherals	The Asynchronous Sample Rate Converter (ASRC) converts the sampling rate of a signal associated to an input clock into a signal associated to a different output clock. The ASRC supports concurrent sample rate conversion of up to 10 channels of about -120dB THD+N. The sample rate conversion of each channel is associated to a pair of incoming and outgoing sampling rates. The ASRC supports up to three sampling rate pairs.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
BCH40	Binary-BCH ECC Processor	System Control Peripherals	The BCH40 module provides up to 40-bit ECC encryption/decryption for NAND Flash controller (GPMI)
CAAM	Cryptographic accelerator and assurance module	Security	CAAM is a cryptographic accelerator and assurance module. CAAM implements several encryption and hashing functions, a run-time integrity checker, and a Pseudo Random Number Generator (PRNG). The pseudo random number generator is certified by Cryptographic Algorithm Validation Program (CAVP) of National Institute of Standards and Technology (NIST). Its DRBG validation number is 94 and its SHS validation number is 1455. CAAM also implements a Secure Memory mechanism. In i.MX 6Solo/6DualLite processors, the security memory provided is 16 KB.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
CCM GPC SRC	Clock Control Module, Global Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSI	MIPI CSI-2 i/f	Multimedia Peripherals	The CSI IP provides MIPI CSI-2 standard camera interface port. The CSI-2 interface supports from 80 Mbps to 1 Gbps speed per data lane.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6Solo/6DualLite platform.
CTI-0 CTI-1 CTI-2 CTI-3 CTI-4	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: <ul style="list-style-type: none"> • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCIC-0 DCIC-1	Display Content Integrity Checker	Automotive IP	The DCIC provides integrity check on portion(s) of the display. Each i.MX 6Solo/6DualLite processor has two such modules.
DSI	MIPI DSI i/f	Multimedia Peripherals	The MIPI DSI IP provides DSI standard display port interface. The DSI interface support 80 Mbps to 1 Gbps speed per data lane.
DTCP	DTCP	Multimedia Peripherals	Provides encryption function according to Digital Transmission Content Protection standard for traffic over MLB150.
eCSPI1-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
ENET	Ethernet Controller	Connectivity Peripherals	<p>The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The module has dedicated hardware to support the IEEE 1588 standard. See the ENET chapter of the reference manual for details.</p> <p>Note: The theoretical maximum performance of 1 Gbps ENET is limited to 470 Mbps (total for Tx and Rx) due to internal bus throughput limitations. The actual measured performance in optimized environment is up to 400 Mbps. For details, see the ERR004512 erratum in the i.MX 6Solo/6DualLite errata document (IMX6SDLCE).</p>
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	<p>Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.</p>
ESAI	Enhanced Serial Audio Interface	Connectivity Peripherals	<p>The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other processors. The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. All serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the word frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is also intended for periodic transfers; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast, the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available.</p> <p>The ESAI has 12 pins for data and clocking connection to external devices.</p>

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-3 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	<p>i.MX 6Solo/6DualLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are:</p> <ul style="list-style-type: none"> Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4 including high-capacity (size > 2 GB) cards HC MMC. Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB. Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v3.0 <p>All four ports support:</p> <ul style="list-style-type: none"> 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) <p>However, the SoC level integration and I/O muxing logic restrict the functionality to the following:</p> <ul style="list-style-type: none"> Instances #1 and #2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. Instances #3 and #4 are primarily intended to serve interfaces to embedded MMC memory or interfaces to on-board SDIO devices. These ports do not have “Card detection” and “Write Protection” pads and do support hardware reset. All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports #1 and #2 in four bit configuration (SD interface). Port #3 is placed in his own independent power domain and port #4 shares power domain with some other interfaces.
FlexCAN-1 FlexCAN-2	Flexible Controller Area Network	Connectivity Peripherals	<p>The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the Electromagnetic interference (EMI) environment of a vehicle, cost-effectiveness and required bandwidth. The FlexCAN module is a full implementation of the CAN protocol specification, Version 2.0 B, which supports both standard and extended message frames.</p>

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
512x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6Solo/6DualLite processors consist of 512x8-bit fuse box accessible through OCOTP_CTRL interface.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5 GPIO-6 GPIO-7	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPMI	General Media Interface	Connectivity Peripherals	The GPMI module supports up to 8x NAND devices. 40-bit ECC encryption/decryption for NAND Flash controller (GPMI2). The GPMI supports separate DMA channels per NAND device.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU3Dv5	Graphics Processing Unit, ver.5	Multimedia Peripherals	The GPU3Dv5 provides hardware acceleration for 3D graphics algorithms with sufficient processor power to run desktop quality interactive graphics applications on displays up to HD1080 resolution. The GPU3D provides OpenGL ES 2.0, including extensions, OpenGL ES 1.1, and OpenVG 1.1
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
HDMI Tx	HDMI Tx i/f	Multimedia Peripherals	The HDMI module provides HDMI standard i/f port to an HDMI 1.4 compliant display.
HSI	MIPI HSI i/f	Connectivity Peripherals	The MIPI HSI provides a standard MIPI interface to the applications processor.
I ² C-1 I ² C-2 I ² C-3 I ² C-4	I ² C Interface	Connectivity Peripherals	I ² C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
IPUV3H	Image Processing Unit, ver.3H	Multimedia Peripherals	IPUV3H enables connectivity to displays and video sources, relevant processing and synchronization and control capabilities, allowing autonomous operation. The IPUv3H supports concurrent output to two display ports and concurrent input from two camera ports, through the following interfaces: <ul style="list-style-type: none"> • Parallel Interfaces for both display and camera • Single/dual channel LVDS display interface • HDMI transmitter • MIPI/DSI transmitter • MIPI/CSI-2 receiver The processing includes: <ul style="list-style-type: none"> • Image conversions: resizing, rotation, inversion, and color space conversion • A high-quality de-interlacing filter • Video/graphics combining • Image enhancement: color adjustment and gamut mapping, gamma correction, and contrast enhancement • Support for display backlight reduction
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8x8 external key pad matrix. KPP features are: <ul style="list-style-type: none"> • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LDB	LVDS Display Bridge	Connectivity Peripherals	LVDS Display Bridge is used to connect the IPU (Image Processing Unit) to External LVDS Display Interface. LDB supports two channels; each channel has following signals: <ul style="list-style-type: none"> • One clock pair • Four data pairs Each signal pair contains LVDS special differential pad (PadP, PadM).
MLB150	MediaLB	Connectivity / Multimedia Peripherals	The MLB interface module provides a link to a MOST [®] data network, using the standardized MediaLB protocol (up to 6144 fs). The module is backward compatible to MLB-50.
MMDC	Multi-Mode DDR Controller	Connectivity Peripherals	DDR Controller has the following features: <ul style="list-style-type: none"> • Supports 16/32-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6Solo • Supports 16/32/64-bit DDR3-800 (LV) or LPDDR2-800 in i.MX 6DualLite • Supports 2x32 LPDDR2-800 in i.MX 6DualLite • Supports up to 4 GByte DDR memory space

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
OCOTP_CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSES). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6Solo/6DualLite processors, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OSC32KHz	OSC32KHz	Clocking	Generates 32.768 KHz clock from external crystal.
PCIe	PCI Express 2.0	Connectivity Peripherals	The PCIe IP provides PCI Express Gen 2.0 functionality.
PMU	Power-Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RAM 16 KB	Secure/non-secure RAM	Secured Internal Memory	Secure/non-secure Internal RAM, interfaced through the CAAM.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SDMA	Smart Direct Memory Access	System Control Peripherals	<p>The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features:</p> <ul style="list-style-type: none"> • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	<p>The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6Solo/6DualLite processors use JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards.</p> <p>The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6Solo/6DualLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.</p>
SPDIF	Sony Philips Digital Interconnect Format	Multimedia Peripherals	<p>A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.</p>
SNVS	Secure Non-Volatile Storage	Security	<p>Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.</p>

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	<p>The SSI is a full-duplex synchronous interface, which is used on the AP to provide connectivity with off-chip audio peripherals. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock / frame sync options.</p> <p>The SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream that reduces CPU overhead in use cases where two time slots are being used simultaneously.</p>
TEMPMON	Temperature Monitor	System Control Peripherals	<p>The Temperature sensor IP is used for detecting die temperature. The temperature read out does not reflect case or ambient temperature. It reflects the temperature in proximity of the sensor location on the die.</p> <p>Temperature distribution may not be uniformly distributed, therefore the read out value may not be the reflection of the temperature value of the entire die.</p>
TZASC	Trust-Zone Address Space Controller	Security	<p>The TZASC (TZC-380 by ARM) provides security address region control functions required for intended application. It is used on the path to the DRAM controller.</p>
UART-1 UART-2 UART-3 UART-4 UART-5	UART Interface	Connectivity Peripherals	<p>Each of the UARTv2 modules support the following serial data transmit/receive protocols and configurations:</p> <ul style="list-style-type: none"> • 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and the i.MX31 UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USBOH3	USB 2.0 High Speed OTG and 3x HS Hosts	Connectivity Peripherals	<p>USBOH3 contains:</p> <ul style="list-style-type: none"> • One high-speed OTG module with integrated HS USB PHY • One high-speed Host module with integrated HS USB PHY • Two identical high-speed Host modules connected to HSIC USB ports.
VDOA	VDOA	Multimedia Peripherals	<p>Video Data Order Adapter (VDOA): used to re-order video data from the “tiled” order used by the VPU to the conventional raster-scan order needed by the IPU.</p>

Table 2. i.MX 6Solo/6DualLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level and HD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing, such as rotation and mirroring. See the <i>i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)</i> for complete list of VPU's decoding/encoding capabilities.
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
WEIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The WEIM NOR-FLASH / PSRAM provides: <ul style="list-style-type: none"> • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
XTALOSC	Crystal Oscillator I/F	Clocks, Resets, and Power Control	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator to provide USB required frequency.

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6Solo/6DualLite processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, “Package Information and Contact Assignments.” Signal descriptions are provided in the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 3. Special Signal Considerations

Signal Name	Remarks
CLK1_P/CLK1_N CLK2_P/CLK2_N	<p>Two general purpose differential high speed clock Input/outputs are provided. Any or both of them could be used:</p> <ul style="list-style-type: none"> To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for PCIe, Video/Audio interfaces, etc. To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals, for example it could be used as an output of the PCIe master clock (root complex use) <p>See the i.MX 6Solo/6DualLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximal frequency range supported is 0...600 MHz. Alternatively one may use single ended signal to drive CLKx_P input. In this case corresponding CLKx_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the CLKx inputs/outputs could be disabled (if not used). If unused any or both of the CLKx_N/P pairs may be left floating.</p>
RTC_XTALI/RTC_XTALO	<p>If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal, (≤ 100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI the RTC_XTALO pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In case when high accuracy real time clock are not required system may use internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and keep RTC_XTALO floating.</p>
XTALI/XTALO	<p>A 24.0 MHz crystal should be connected between XTALI and XTALO. level and the frequency should be <32 MHz under typical conditions. The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typical 80 Ω is recommended. Freescale BSP (board support package) software requires 24 MHz on XTALI/XTALO. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO is floated. The XTALI signal level must swing from $\sim 0.8 \times$ NVCC_PLL_OUT to ~ 0.2 V. If this clock is used as a reference for USB and PCIe, then there are strict frequency tolerance and jitter requirements. See OSC24M chapter and relevant interface specifications chapters for details.</p>

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
DRAM_VREF	<p>When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DDR_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 μF capacitor.</p> <p>To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the \pm 2% DDR_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6Solo/6DualLite are drawing current on the resistor divider.</p> <p>It is recommended to use regulated power supply for “big” memory configurations (more than eight devices)</p>
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.
NVCC_LVDS2P5	The DDR pre-drivers share the NVCC_LVDS2P5 ball with the LVDS interface. This ball can be shorted to VDDHIGH_CAP on the circuit board.
VDD_FA FA_ANA	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
GPANAIO	This signal is reserved for Freescale manufacturing use only. User must leave this connection floating.
JTAG_nnnn	<p>The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.</p> <p>JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.</p> <p>JTAG_MOD is referenced as SJC_MOD in the i.MX 6Solo/6DualLite reference manual. Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MOD set to hi configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.</p>
NC	These signals are No Connect (NC) and should be floated by the user.
POR_B	This cold reset negative logic input resets all modules and logic in the IC. May be used in addition to internally generated power on reset signal (logical AND, both internal and external signals are considered active low).
ONOFF	In normal mode may be connected to ON/OFF button (De-bouncing provided at this input). Internally this pad is pulled up. Short connection to GND in OFF mode causes internal power management state machine to change state to ON. In ON mode short connection to GND generates interrupt (intended to SW controllable power down). Long above ~5s connection to GND causes “forced” OFF.
TEST_MODE	TEST_MODE is for Freescale factory use. This signal is internally connected to an on-chip pull-down device. The user must either float this signal or tie it to GND.
PCIE_REXT	The impedance calibration process requires connection of reference resistor 200 Ω 1% precision resistor on PCIE_REXT pad to ground.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
CSI_REXT	MIPI CSI PHY reference resistor. Use 6.04 K Ω 1% resistor connected between this pad and GND
DSI_REXT	MIPI DSI PHY reference resistor. Use 6.04 K Ω 1% resistor connected between this pad and GND

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-chip Termination
JTAG_TCK	Input	47 k Ω pull-up
JTAG_TMS	Input	47 k Ω pull-up
JTAG_TDI	Input	47 k Ω pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 k Ω pull-up
JTAG_MOD	Input	100 k Ω pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
CCM	CLK1_N, CLK1_P, CLK2_N, CLK2_P	Float
CSI	CSI_CLK0M, CSI_CLK0P, CSI_D0M, CSI_D0P, CSI_D1M, CSI_D1P, CSI_REXT	Float
DSI	DSI_CLK0M, DSI_CLK0P, DSI_D0M, DSI_D0P, DSI_D1M, DSI_D1P, DSI_REXT	Float
HDMI	HDMI_CLKM, HDMI_CLKP, HDMI_D0M, HDMI_D0P, HDMI_D1M, HDMI_D1P, HDMI_D2M, HDMI_D2P, HDMI_DDCEC, HDMI_HPD, HDMI_REF	Float
	HDMI_VP, HDMI_VPH	Ground
LDB	LVDS0_CLK_N, LVDS0_CLK_P, LVDS0_TX0_N, LVDS0_TX0_P, LVDS0_TX1_N, LVDS0_TX1_P, LVDS0_TX2_N, LVDS0_TX2_P, LVDS0_TX3_N, LVDS0_TX3_P, LVDS1_CLK_N, LVDS1_CLK_P, LVDS1_TX0_N, LVDS1_TX0_P, LVDS1_TX1_N, LVDS1_TX1_P, LVDS1_TX2_N, LVDS1_TX2_P, LVDS1_TX3_N, LVDS1_TX3_P	Float
MLB	MLB_CN, MLB_CP, MLB_DN, MLB_DP, MLB_SN, MLB_SP	Float
PCIe	PCIE_REXT, PCIE_RXM, PCIE_RXP, PCIE_TXM, PCIE_TXP	Float
	PCIE_VP, PCIE_VPH, PCIE_VPTX	Ground ¹
RGMII	RGMII_RD0, RGMII_RD1, RGMII_RD2, RGMII_RD3, RGMII_RX_CTL, RGMII_RXC, RGMII_TD0, RGMII_TD1, RGMII_TD2, RGMII_TD3, RGMII_TX_CTL, RGMII_TXC	Float
USB	USB_H1_DN, USB_H1_DP, USB_H1_VBUS, USB_OTG_CHD_B, USB_OTG_DN, USB_OTG_DP, USB_OTG_VBUS	Float

¹ In this case, the BSR chain will not work.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6Solo/6DualLite processors.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See [Table 6](#) for a quick reference to the individual tables and sections.

Table 6. i.MX 6Solo/6DualLite Chip-Level Conditions

For these characteristics, ...	Topic appears ...
Absolute Maximum Ratings	on page 22
BGA Case 2240 Package Thermal Resistance	on page 23
Operating Ranges	on page 24
External Clock Sources	on page 26
Maximal Supply Currents	on page 27
Low Power Mode Supply Currents	on page 29
USB PHY Current Consumption	on page 30
PCIe 2.0 Power Consumption	on page 30

4.1.1 Absolute Maximum Ratings

Table 7. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Core supply voltages	VDDARM_IN VDDSOC_IN	-0.3	1.5	V
Internal supply voltages	VDDARM_CAP VDDSOC_CAP VDDPU_CAP	-0.3	1.3	V
GPIO supply voltage	Supplies denoted as I/O supply	-0.5	3.6	V
DDR I/O supply voltage	Supplies denoted as I/O supply	-0.4	1.975	V
MLB I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
LVDS I/O supply voltage	Supplies denoted as I/O supply	-0.3	2.8	V
VDD_SNVS_IN supply voltage	VDD_SNVS_IN	-0.3	3.3	V
VDDHIGH_IN supply voltage	VDDHIGH_IN	-0.3	3.6	V
USB VBUS	VBUS	—	5.25	V
Input voltage on USB_OTG_DP, USB_OTG_DN, USB_H1_DP, USB_H1_DN pins	USB_DP/USB_DN	-0.3	3.63	V
Input/output voltage range	V_{in}/V_{out}	-0.5	OVDD ¹ +0.3	V

Table 7. Absolute Maximum Ratings (continued)

Parameter Description	Symbol	Min	Max	Unit
ESD damage immunity: <ul style="list-style-type: none"> • Human Body Model (HBM) • Charge Device Model (CDM) 	V_{esd}	— —	2000 500	V
Storage temperature range	T_{STORAGE}	-40	150	°C

¹ OVDD is the I/O supply voltage.

4.1.2 Thermal Resistance

4.1.2.1 BGA Case 2240 Package Thermal Resistance

Table 8 displays the thermal resistance data.

Table 8. Thermal Resistance Data

Rating	Test Conditions	Symbol	Value	Unit
Junction to Ambient ¹	Single-layer board (1s); natural convection ²	$R_{\theta\text{JA}}$	38	°C/W
	Four-layer board (2s2p); natural convection ²	$R_{\theta\text{JA}}$	23	°C/W
Junction to Ambient ¹	Single-layer board (1s); airflow 200 ft/min ^{2,3}	$R_{\theta\text{JA}}$	30	°C/W
	Four-layer board (2s2p); airflow 200 ft/min ^{2,3}	$R_{\theta\text{JA}}$	20	°C/W
Junction to Board ^{1,4}		$R_{\theta\text{JB}}$	14	°C/W
Junction to Case ^{1,5}		$R_{\theta\text{JC}}$	6	°C/W
Junction to Package Top ^{1,6}	Natural Convection	Ψ_{JT}	2	°C/W

¹ Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

² Per JEDEC JESD51-2 with the single layer board horizontal. Thermal test board meets JEDEC specification for the specified package.

³ Per JEDEC JESD51-6 with the board horizontal.

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

4.1.3 Operating Ranges

Table 9 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment
Run mode: LDO enabled	VDDARM_IN	1.275 ²	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.150 V minimum for operation up to 792 MHz.
		1.175 ²	—	1.5	V	LDO Output Set Point (VDDARM_CAP) = 1.05 V minimum for operation up to 396 MHz.
	VDDSOC_IN ³	1.275 ^{2,4}	—	1.5	V	VPU <= 328 MHz, VDDSOC and VDDPU LDO outputs (VDDSOC_CAP and VDDPU_CAP) = 1.225 V maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDDARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.05	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDDSOC_IN ³	1.15 ⁴	—	1.225	V	LDO bypassed for operation VPU <= 328 MHz
Standby/DSM mode	VDDARM_IN	0.9	—	1.3	V	Refer to Table 13, "Stop Mode Current and Power Consumption," on page 29.
	VDDSOC_IN	0.9	—	1.225	V	
VDDHIGH internal regulator	VDDHIGH_IN	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN ⁵	2.9	—	3.3	V	Should be supplied from the same supply as VDDHIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	
	USB_H1_VBUS	4.4	—	5.25	V	
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2, DDR3-U
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3_L
Supply for RGMII I/O power group ⁶	NVCC_RGMII	1.15	—	2.625	V	1.15 V – 1.30 V in HSIC 1.2 V mode 1.43 V – 1.58 V in RMGII 1.5 V mode 1.70 V – 1.90 V in RMGII 1.8 V mode 2.25 V – 2.625 V in RMGII 2.5 V mode

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max ¹	Unit	Comment
GPIO supply voltages ⁶	NVCC_CSI, NVCC_EIM, NVCC_ENET, NVCC_GPIO, NVCC_LCD, NVCC_NANDF, NVCC_SD1, NVCC_SD2, NVCC_SD3, NVCC_JTAG	1.65	1.8, 2.8, 3.3	3.6	V	
	NVCC_LVDS2P5 ⁷ NVCC_MIPI	2.25	2.5	2.75	V	
HDMI supply voltages	HDMI_VP	0.99	1.1	1.3	V	
	HDMI_VPH	2.25	2.5	2.75	V	
PCIe supply voltages	PCIE_VP	1.023	1.1	1.225	V	
	PCIE_VPH	2.325	2.5	2.75	V	
	PCIE_VPTX	1.023	1.1	1.225	V	
Junction temperature	T _J	-40	—	125	°C	Refer to Automotive qualification report for details.

¹ Applying the maximum voltage results in maximum power consumption and heat generation. Freescale recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

² VDDARM_IN and VDDSOC_IN must be 125 mV higher than the LDO Output Set Point for correct regulator supply voltage.

³ VDDSOC_CAP and VDDPU_CAP must be equal.

⁴ VDDSOC and VDDPU output voltage must be set to this rule: VDDARM - VDDSOC/PU < 100 mV.

⁵ While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

⁶ All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not and associated IO pins need to have a Pullup or Pulldown resistor applied to limit any floating gate current.

⁷ This supply also powers the pre-drivers of the DDR IO pins, hence, it must be always provided, even when LVDS is not used

Table 10 shows on-chip LDO regulators that can supply on-chip loads.

Table 10. On-Chip LDOs¹ and their On-Chip Loads

Voltage Source	Load	Comment
VDDHIGH_CAP	NVCC_LVDS2P5	Board-level connection to VDDHIGH_CAP
	NVCC_MIPI	
	HDMI_VPH	
	PCIE_VPH	

Table 10. On-Chip LDOs¹ and their On-Chip Loads (continued)

Voltage Source	Load	Comment
VDDSOC_CAP	HDMI_VP	Board-level connection to VDDSOC_CAP ^{2 3}
	PCIE_VP	
	PCIE_VPTX	

¹ On-chip LDOs are designed to supply i.MX6 loads and must not be used to supply external loads.

² VDDARM_CAP should not exceed VDDSOC_CAP by more than 50 mV.

³ There is no requirement for VDDSOC_CAP to track within 50 mV as long as it is greater than VDDARM_CAP.

4.1.4 External Clock Sources

Each i.MX 6Solo/6DualLite processor has two external input system clocks: a low frequency (CKIL) and a high frequency (XTAL).

The CKIL is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watch-dog counters. The clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the CKIL, in case accuracy is not important.

The system clock input XTAL is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either external oscillator or a crystal using internal oscillator amplifier.

Table 11 shows the interface frequency requirements.

Table 11. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
CKIL Oscillator ^{1,2}	f_{ckil}	—	32.768 ³ /32.0	—	kHz
XTAL Oscillator ^{2,4}	f_{xtal}		24		MHz

¹ External oscillator or a crystal with internal oscillator amplifier.

² The required frequency stability of this clock source is application dependent. For recommendations, see the Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

³ Recommended nominal frequency 32.768 kHz.

⁴ External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in [Table 11](#) are required for use with Freescale BSPs to ensure precise time keeping and USB operation. For RTC_XTAL operation, two clock sources are available.

On-chip 40 kHz ring oscillator—this clock source has the following characteristics:

Approximately 25 μ A more I_{dd} than crystal oscillator

Approximately $\pm 50\%$ tolerance

No external component required

Starts up quicker than 32 kHz crystal oscillator

External crystal oscillator with on-chip support circuit:

At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.

Higher accuracy than ring oscillator

If no external crystal is present, then the ring oscillator is utilized

The decision of choosing a clock source should be taken based on real-time clock use and precision timeout.

4.1.5 Maximal Supply Currents

The Power Virus numbers shown in [Table 12](#) represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The MMPF0100xxxx, Freescale's power management IC targeted for the i.MX 6x family, supports the Power Virus mode operating at 1% duty cycle. Higher duty cycles are allowed, but a robust thermal design is required for the increased system power dissipation.

See the i.MX 6Solo/6DualLite Power Consumption Measurement Application Note (AN4576) for more details on typical power consumption under various use case definitions.

Table 12. Maximal Supply Currents

Power Line	Conditions	Max Current	Unit
VDDARM_IN	996 MHz ARM clock based on Power Virus operation	2200	mA
VDDSOC_IN	996 MHz ARM clock	1260	mA
VDDHIGH_IN		125 ¹	mA
VDD_SNVS_IN		275 ²	μ A
USB_OTG_VBUS/USB_H1_VBUS (LDO 3P0)		25 ³	mA
Primary Interface (IO) Supplies			

Table 12. Maximal Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_DRAM	—	— ⁴	
NVCC_ENET	N=10	Use maximal IO equation ⁵	
NVCC_LCD	N=29	Use maximal IO equation ⁵	
NVCC_GPIO	N=24	Use maximal IO equation ⁵	
NVCC_CSI	N=20	Use maximal IO equation ⁵	
NVCC_EIM	N=53	Use maximal IO equation ⁵	
NVCC_JTAG	N=6	Use maximal IO equation ⁵	
NVCC_RGMII	N=12	Use maximal IO equation ⁵	
NVCC_SD1	N=6	Use maximal IO equation ⁵	
NVCC_SD2	N=6	Use maximal IO equation ⁵	
NVCC_SD3	N=11	Use maximal IO equation ⁵	
NVCC_NANDF	N=26	Use maximal IO equation ⁵	
MISC			
DDR_VREF	—	1	mA

- ¹ The actual maximum current drawn from VDDHIGH_IN will be as shown plus any additional current drawn from the VDDHIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS2P5, NVCC_MIPI, or HDMI and PCIe VPH supplies).
- ² The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.
- ³ This is the maximum current per active USB physical interface.
- ⁴ The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.
- ⁵ General equation for estimated, maximal power consumption of an IO power supply:

$$I_{max} = N \times C \times V \times (0.5 \times F)$$

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.

4.1.6 Low Power Mode Supply Currents

Table 13 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 13. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical ¹	Units
WAIT	<ul style="list-style-type: none"> ARM, SoC, and PU LDOs are set to 1.225 V HIGH LDO set to 2.5 V Clocks are gated. DDR is in self refresh. PLLs are active in bypass (24MHz) Supply Voltages remain ON 	VDDARM_IN (1.4V)	4.5	mA
		VDDSOC_IN (1.4V)	23	
		VDDHIGH_IN (3.0V)	13.5	
		Total	79	mW
STOP_ON	<ul style="list-style-type: none"> ARM LDO set to 0.9V SoC and PU LDOs set to 1.225 V HIGH LDO set to 2.5 V PLLs disabled DDR is in self refresh. 	VDDARM_IN (1.4V)	4	mA
		VDDSOC_IN (1.4V)	22	
		VDDHIGH_IN (3.0V)	8.5	
		Total	61.9	mW
STOP_OFF	<ul style="list-style-type: none"> ARM LDO set to 0.9V SoC LDO set to: 1.225 V PU LDO is power gated HIGH LDO set to 2.5 V PLLs disabled DDR is in self refresh 	VDDARM_IN (1.4V)	4	mA
		VDDSOC_IN (1.4V)	13.5	
		VDDHIGH_IN (3.0V)	7.5	
		Total	47	mW
STANDBY	<ul style="list-style-type: none"> ARM and PU LDOs are power gated SoC LDO is in bypass HIGH LDO is set to 2.5V PLLs are disabled Low Voltage Well Bias ON XTAL is enabled 	VDDARM_IN (0.9V)	0.1	mA
		VDDSOC_IN (0.9V)	5	
		VDDHIGH_IN (3.0V)	5	
		Total	19.6	mW
Deep Sleep Mode (DSM)	<ul style="list-style-type: none"> ARM and PU LDOs are power gated SoC LDO is in bypass HIGH LDO is set to 2.5V PLLs are disabled Low Voltage Well Bias ON XTAL and bandgap are disabled 	VDDARM_IN (0.9V)	0.1	mA
		VDDSoC_IN (0.9V)	2	
		VDDHIGH_IN (3.0V)	0.5	
		Total	3.4	mW

¹ The typical values shown here are for information only and are not guaranteed. These values are average values measured on a typical wafer at 25°C.

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the VBUS valid detectors in typical condition. Table 14 shows the USB interface current consumption in power down mode..

Table 14. USB PHY Current Consumption in Power Down Mode

	VDDUSB_CAP (3.0 V)	VDDHIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 μ A	1.7 μ A	<0.5 μ A

NOTE

The currents on the VDDHIGH_CAP and VDDUSB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

Table 15 provides PCIe PHY currents under certain Tx operating modes.

Table 15. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
PO: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
POs: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State		PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	
Power Down		PCIE_VP (1.1 V)	1.3	mA
		PCIE_VPTX (1.1 V)	0.18	
		PCIE_VPH (2.5 V)	0.36	

4.1.9 HDMI Power Consumption

Table 16 provides HDMI PHY currents for both Active 3D Tx with LFSR15 data and power-down modes.

Table 16. HDMI PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
Active	Bit rate 251.75 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.1	mA
	Bit rate 279.27 Mbps	HDMI_VPH	14	mA
		HDMI_VP	4.2	mA
	Bit rate 742.5 Mbps	HDMI_VPH	17	mA
		HDMI_VP	7.5	mA
	Bit rate 1.485 Gbps	HDMI_VPH	17	mA
		HDMI_VP	12	mA
	Bit rate 2.275 Gbps	HDMI_VPH	16	mA
		HDMI_VP	17	mA
	Bit rate 2.97 Gbps	HDMI_VPH	19	mA
		HDMI_VP	22	mA
Power-down		HDMI_VPH	49	μA
		HDMI_VP	1100	μA

4.2 Power Supplies Requirements and Restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

4.2.1 Power-Up Sequence

The below restrictions must be followed:

- VDD_SNVS_IN supply must be turned on before any other power supply or be connected (shorted) with VDDHIGH_IN supply.
- If a coin cell is used to power VDD_SNVS_IN, then ensure that it is connected before any other supply is switched on.
- If VDDARM_IN and VDDSOC_IN are connected to different external supply sources, then the following restrictions apply:

- VDDARM_IN supply must be turned ON together with VDDSOC_IN supply or not delayed more than 1 ms
- VDDARM_CAP must not exceed VDDSOC_CAP by more than 50 mV.

NOTE

The POR_B input (if used) must be immediately asserted at power-up and remain asserted until after the last power rail reaches its working voltage. In the absence of an external reset feeding the POR_B input, the internal POR module takes control. See the *i.MX 6Solo/6DualLite Reference Manual* for further details and to ensure that all necessary requirements are being met.

NOTE

Need to ensure that there is no back voltage (leakage) from any supply on the board towards the 3.3 V supply (for example, from the external components that use both the 1.8 V and 3.3 V supplies).

NOTE

USB_OTG_VBUS and USB_H1_VBUS are not part of the power supply sequence and may be powered at any time.

4.2.2 Power-Down Sequence

No special restrictions for i.MX 6Solo/6DualLite IC.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_XXX) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Rail” columns in pin list tables of [Section 6, “Package Information and Contact Assignments.”](#)

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for details on the power tree scheme.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of

their input supply ripple rejection and their on-die trimming. This translates into more stable voltage for the on-chip logics.

These regulators have three basic modes:

- Bypass. The regulation FET is switched fully on passing the external voltage, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2 Analog Regulators

4.3.2.1 LDO_1P1

The LDO_1P1 regulator implements a programmable linear-regulator function from VDDHIGH_IN (see [Table 9](#) for minimum and maximum input requirements). Typical Programming Operating Range is 1.0 V to 1.2 V with the nominal default setting as 1.1 V. Since the accuracy or the % regulation is not tested, and only tested with the LDO set to either 1.0V or 1.2V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.2 LDO_2P5

The LDO_2P5 module implements a programmable linear-regulator function from VDDHIGH_IN (see [Table 9](#) for minimum and maximum input requirements). Typical Programming Operating Range is 2.25 V to 2.75 V with the nominal default setting as 2.5 V. Since the accuracy or the % regulation is not tested, and only tested with the LDO set to either 2.25V or 2.75V, this is the only range that is guaranteed. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μ F (2.2 μ F should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. Current-limiting can be enabled to allow for in-rush current requirements during start-up, if needed. Active-pull-down can also be enabled for systems requiring this feature. An alternate self-biased low-precision weak-regulator is included that can be

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enabled for applications needing to keep the output voltage alive during low-power modes where the main regulator driver and its associated global bandgap reference module are disabled. The output of the weak-regulator is not programmable and is a function of the input supply as well as the load current. Typically, with a 3 V input supply the weak-regulator output is 2.525 V and its output impedance is approximately 40 Ω .

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.3.2.3 LDO_USB

The LDO_USB module implements a programmable linear-regulator function from the USB_OTG_VBUS and USB_H1_VBUS voltages (4.4 V–5.25 V) to produce a nominal 3.0 V output voltage. The regulator has been designed to be stable with a minimum external low ESR decoupling capacitor of 1 μF (2.2 μF should be considered the recommended minimum value for component selection), though the actual capacitance required should be determined by the application. A programmable brown-out detector is included in the regulator that can be used by the system to determine when the load capability of the regulator is being exceeded, to take the necessary steps. This regulator has a built in power-mux that allows the user to select to run the regulator from either VBUS supply, when both are present. If only one of the VBUS voltages is present, then, the regulator automatically selects this supply. Current limit is also included to help the system meet in-rush current targets.

For additional information, see the i.MX 6Solo/6DualLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 17. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.2 528 MHz PLL

Table 18. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.3 Ethernet PLL

Table 19. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles

4.4.4 480 MHz PLL

Table 20. 480 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<383 reference cycles

4.4.5 MLB PLL

The MediaLB PLL is necessary in the MediaLB 6-Pin implementation to phase align the internal and external clock edges, effectively tuning out the delay of the differential clock receiver and is also responsible for generating the higher speed internal clock, when the internal-to-external clock ratio is not 1:1.

Table 21. MLB PLL's Electrical Parameters

Parameter	Value
Lock time	<1 ms

4.4.6 ARM PLL

Table 22. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDDHIGH_IN such as the oscillator consumes power from VDDHIGH_IN when that supply is available and transitions to the back up battery when VDDHIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to a crude internal ring oscillator. The frequency range of this block is approximately 10–45 kHz. It highly depends on the process, voltage, and temperature.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from the VDDHIGH_IN/VDD_SNVS_IN. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDHIGH_IN range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell. For example, for Panasonic ML621:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, $R_s = (3.2-2.5)/0.6 \text{ m} = 1.17 \text{ k}$

Table 23. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Fosc		32.768 KHz		This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption		4 μ A		The 4 μ A is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 μ A when ring oscillator is inactive, 20 μ A when the ring oscillator is running. Another 1.5 μ A is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 μ A on vdd_rtc when the ring oscillator is not running.

Table 23. OSC32K Main Characteristics

	Min	Typ	Max	Comments
Bias resistor		14 M Ω		This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Crystal Properties				
Cload		10 pF		Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR		50 k Ω	100 k Ω	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes
- LVDS I/O
- MLB I/O

NOTE

The term 'OVDD' in this section refers to the associated supply rail of an input or output.

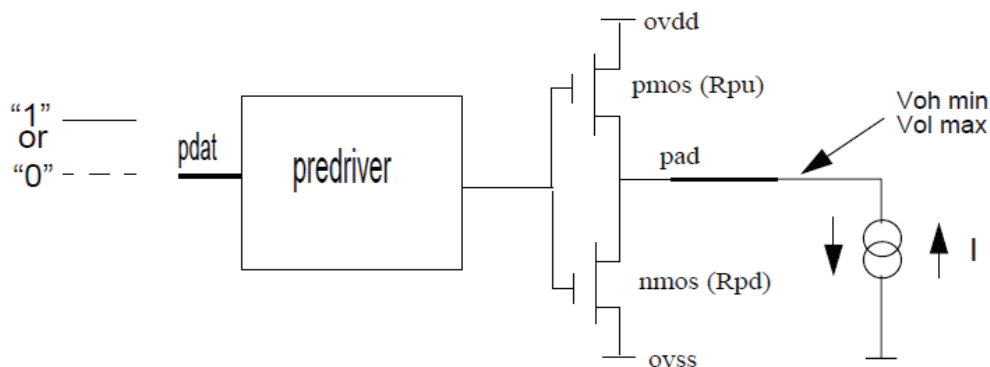


Figure 3. Circuit for Parameters V_{oh} and V_{ol} for I/O Cells

4.6.1 General Purpose I/O (GPIO) DC Parameters

Table 24 shows DC parameters for GPIO pads. The parameters in Table 24 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 24. GPIO DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Units
GPIO DC Electrical Characteristics					
High-level output voltage ¹	V _{OH}	I _{oh} = -0.1mA (ipp_dse=001,010) I _{oh} = -1mA (ipp_dse=011,100,101,110,111)	OVDD-0.15		V
Low-level output voltage ¹	V _{OL}	I _{ol} = 0.1mA (ipp_dse=001,010) I _{ol} = 1mA (ipp_dse=011,100,101,110,111)	0.15	V	
High-Level input voltage ^{1,2}	V _{IH}		0.7*OVDD	OVDD	V
Low-Level input voltage ^{1,2}	V _{IL}		0	0.3*OVDD	V
Input Hysteresis(OVDD= 1.8V)	VHYS_LowVDD	OVDD=1.8V	250		mV
Input Hysteresis(OVDD=3.3V)	VHYS_HighVDD	OVDD=3.3V	250		mV
Schmitt trigger VT ^{2,3}	VTH+		0.5*OVDD		mV
Schmitt trigger VT ^{2,3}	VTH-			0.5*OVDD	mV
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=0V		212	uA
Pull-up resistor (22_kΩ PU)	RPU_22K	Vin=OVDD		1	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=0V		100	uA
Pull-up resistor (47_kΩ PU)	RPU_47K	Vin=OVDD		1	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=0V		48	uA
Pull-up resistor (100_kΩ PU)	RPU_100K	Vin=OVDD		1	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=OVDD		48	uA
Pull-down resistor (100_kΩ PD)	RPD_100K	Vin=0V		1	uA
Input current (no PU/PD)	IIN	V _I = 0, V _I = OVDD	-1	1	uA
Keeper Circuit Resistance	R_Keeper	V _I = .3*OVDD, V _I = .7* OVDD	105	175	kΩ

¹ Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

- ² To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, V_{il} or V_{ih} . Monotonic input transition time is from 0.1 ns to 1 s.
- ³ Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.2 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3/DDR3L operational modes.

4.6.2.1 LPDDR2 Mode I/O DC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009.

Table 25. LPDDR2 I/O DC Electrical Parameters¹

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	V_{OH}	$I_{oh} = -0.1\text{mA}$	$0.9 \cdot OVDD$		V
Low-level output voltage	V_{OL}	$I_{ol} = 0.1\text{mA}$		$0.1 \cdot OVDD$	V
Input Reference Voltage	V_{ref}		$0.49 \cdot OVDD$	$0.51 \cdot OVDD$	V
DC High-Level input voltage	V_{ih_DC}		$V_{ref} + 0.13$	$OVDD$	V
DC Low-Level input voltage	V_{il_DC}		$OVSS$	$V_{ref} - 0.13$	V
Differential Input Logic High	V_{ih_diff}		0.26	Note ²	
Differential Input Logic Low	V_{il_diff}		Note ³	-0.26	
Pull-up/Pull-down Impedance Mismatch	$Mmpupd$		-15	15	%
240 Ω unit calibration resolution	R_{res}			10	Ω
Keeper Circuit Resistance	R_{keep}		110	175	$k\Omega$
Input current (no pull-up/down)	I_{in}	$V_I = 0, V_I = OVDD$	-2.5	2.5	μA

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

² The single-ended signals need to be within the respective limits ($V_{ih}(dc)$ max, $V_{il}(dc)$ min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.2.2 DDR3/DDR3L Mode I/O DC Parameters

The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008. The parameters in Table 26 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

Table 26. DDR3/DDR3L I/O DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	VOH	I _{oh} = -0.1mA V _{oh} (for ipp_dse=001)	0.8*OVDD ¹		V
Low-level output voltage	VOL	I _{ol} = 0.1mA V _{ol} (for ipp_dse=001)	0.2*OVDD	V	
High-level output voltage	VOH	I _{oh} = -1mA V _{oh} (for all except ipp_dse=001)	0.8*OVDD		V
Low-level output voltage	VOL	I _{ol} = 1mA V _{ol} (for all except ipp_dse=001)	0.2*OVDD	V	
Input Reference Voltage	Vref		0.49*ovdd	0.51*ovdd	V
DC High-Level input voltage	Vih_DC		Vref ² +0.1	OVDD	V
DC Low-Level input voltage	Vil_DC		OVSS	Vref-0.1	V
DifferentialInput Logic High	Vih_diff		0.2	See Note ³	V
DifferentialInput Logic Low	Vil_diff		See Note ³	-0.2	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	0.49*OVDD	0.51*OVDD	V
Pull-up/Pull-down Impedance Mismatch	Mmpupd		-10	10	%
240 Ω unit calibration resolution	Rres			10	Ω
Keeper Circuit Resistance	Rkeep		105	165	kΩ
Input current (no pull-up/down)	Iin	V _I = 0, V _I = OVDD	-2.9	2.9	μA

¹ OVDD – I/O power supply (1.425 V–1.575 V for DDR3 and 1.283 V–1.45 V for DDR3L)

² Vref – DDR3/DDR3L external reference voltage

³ The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.

4.6.3 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

Table 27 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 27. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS		1.125	1.2	1.375	V

4.6.4 MLB I/O DC Parameters

The MLB interface complies with Analog Interface of 6-pin differential Media Local Bus specification version 4.1. See 6-pin differential MLB specification v4.1, “MediaLB 6-pin interface Electrical Characteristics” for details.

NOTE

The MLB 6-pin interface does not support speed mode 8192 fs.

Table 28 shows the Media Local Bus (MLB) I/O DC parameters.

Table 28. MLB I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output Differential Voltage	VOD	Rload-50Ω Diff	300	500	mV
Output High Voltage	VOH	Rload-50Ω Diff	1.25	1.75	V
Output Low Voltage	VOL	Rload-50Ω Diff	0.75	1.25	V
Common-mode output voltage ((Vpadp*+Vpadn*)/2)	Vocm	Rload-50Ω Diff	1	1.5	V
Differential output impedance	Zo		1.6		kΩ

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 4 and Figure 5.

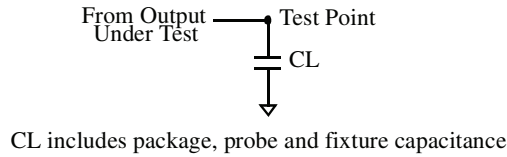


Figure 4. Load Circuit for Output

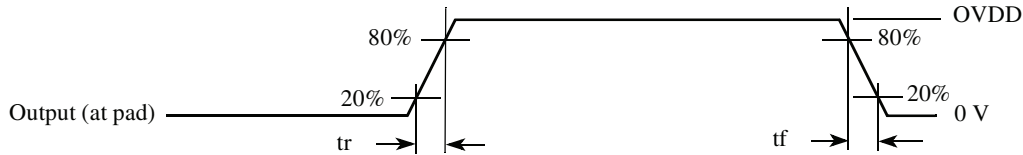


Figure 5. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the [Table 29](#) and [Table 30](#), respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 29. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 30. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive, ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times ¹	trm	—	—	—	25	ns

¹ Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.7.2 DDR I/O AC Parameters

The LPDDR2 interface mode fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3/DDR3L interface mode fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 31 shows the AC parameters for DDR I/O operating in LPDDR2 mode.

Table 31. DDR I/O LPDDR2 Mode AC Parameters¹

Parameter	Symbol	Test Condition	Min	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	OVDD	V
AC input logic low	Vil(ac)	—	0	Vref - 0.22	V
AC differential input high voltage ²	Vidh(ac)	—	0.44	—	V
AC differential input low voltage	Vidl(ac)	—	—	0.44	V
Input AC differential cross point voltage ³	Vix(ac)	Relative to Vref	-0.12	0.12	V
Over/undershoot peak	Vpeak	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	0.3	V-ns
Single output slew rate, measured between Vol(ac) and Voh(ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 40 Ω \pm 30%	1.5	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω \pm 30%	1	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t _{SKD}	clk = 400 MHz	—	0.1	ns

¹ Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

Electrical Characteristics

- ² Vid(ac) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The Minimum value is equal to $V_{ih}(ac) - V_{il}(ac)$.
- ³ The typical value of $V_{ix}(ac)$ is expected to be about $0.5 \times OVDD$. and $V_{ix}(ac)$ is expected to track variation of $OVDD$. $V_{ix}(ac)$ indicates the voltage at which differential input signal must cross.

Table 32 shows the AC parameters for DDR I/O operating in DDR3/DDR3L mode.

Table 32. DDR I/O DDR3/DDR3L Mode AC Parameters¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	$V_{ih}(ac)$	—	$V_{ref} + 0.175$	—	$OVDD$	V
AC input logic low	$V_{il}(ac)$	—	0	—	$V_{ref} - 0.175$	V
AC differential input voltage ²	$V_{id}(ac)$	—	0.35	—	—	V
Input AC differential cross point voltage ³	$V_{ix}(ac)$	Relative to V_{ref}	$V_{ref} - 0.15$	—	$V_{ref} + 0.15$	V
Over/undershoot peak	V_{peak}	—	—	—	0.4	V
Over/undershoot area (above $OVDD$ or below $OVSS$)	V_{area}	400 MHz	—	—	0.5	V-ns
Single output slew rate, measured between $V_{ol}(ac)$ and $V_{oh}(ac)$	t_{sr}	Driver impedance = 34Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

¹ Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

² Vid(ac) specifies the input differential voltage $|V_{tr} - V_{cp}|$ required for switching, where V_{tr} is the “true” input signal and V_{cp} is the “complementary” input signal. The Minimum value is equal to $V_{ih}(ac) - V_{il}(ac)$.

³ The typical value of $V_{ix}(ac)$ is expected to be about $0.5 \times OVDD$. and $V_{ix}(ac)$ is expected to track variation of $OVDD$. $V_{ix}(ac)$ indicates the voltage at which differential input signal must cross.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 6.

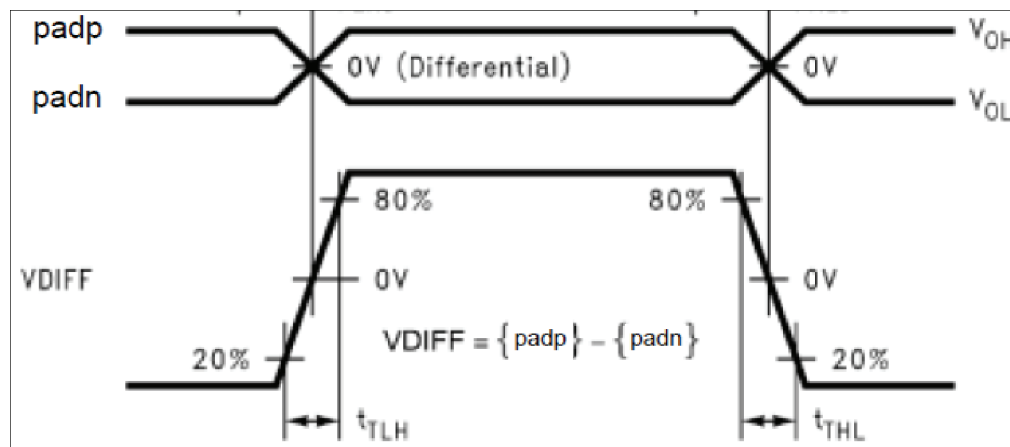


Figure 6. Differential LVDS Driver Transition Time Waveform

Table 33 shows the AC parameters for LVDS I/O.

Table 33. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew ¹	t_{SKD}	Rload = 100 Ω , Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time ²	t_{TLH}		—	—	0.5	
Transition High to Low Time ²	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

¹ $t_{SKD} = |t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

4.7.4 MLB I/O AC Parameters

The differential output transition time waveform is shown in Figure 7.

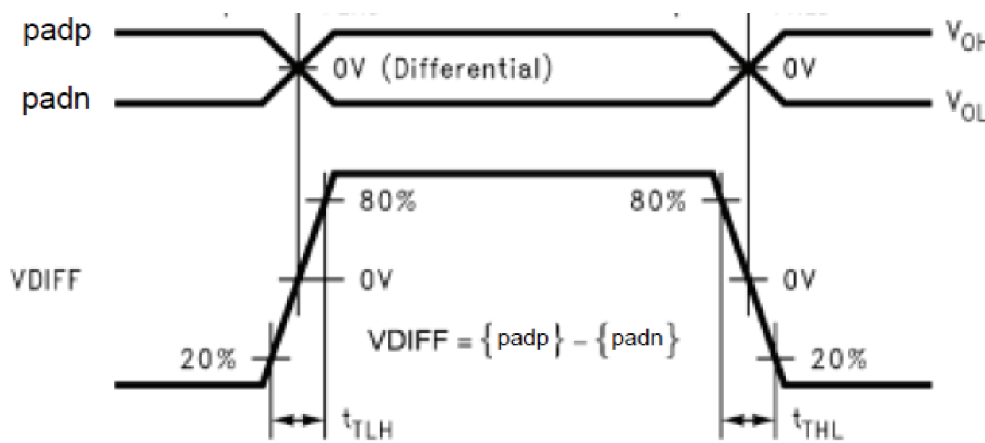


Figure 7. Differential MLB Driver Transition Time Waveform

A 4-stage pipeline is utilized in the MLB 6-pin implementation in order to facilitate design, maximize throughput, and allow for reasonable PCB trace lengths. Each cycle is one $ipp_clk_in^*$ (internal clock from MLB PLL) clock period. Cycles 2, 3, and 4 are MLB PHY related. Cycle 2 includes clock-to-output delay of Signal/Data sampling flip-flop and Transmitter, Cycle 3 includes clock-to-output delay of Signal/Data clocked receiver, Cycle 4 includes clock-to-output delay of Signal/Data sampling flip-flop.

MLB 6-pin pipeline diagram is shown in Figure 8.

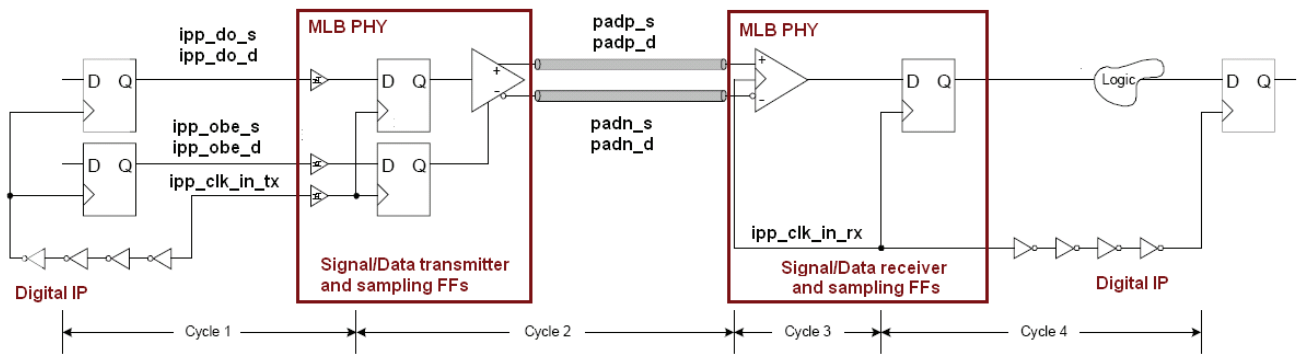


Figure 8. MLB 6-Pin Pipeline Diagram

Table 34 shows the AC parameters for MLB I/O.

Table 34. I/O AC Parameters of MLB PHY

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew ¹	t_{SKD}	Rload = 50 Ω between padp and padn	—	—	0.1	ns
Transition Low to High Time ²	t_{TLH}		—	—	1	
Transition High to Low Time	t_{THL}		—	—	1	
MLB external clock Operating Frequency	fclk_ext	—	—	—	102.4	MHz
MLB PLL clock Operating Frequency	fclk_pll	—	—	—	307.2	MHz

¹ $t_{SKD} = |t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

² Measurement levels are 20-80% from output voltage.

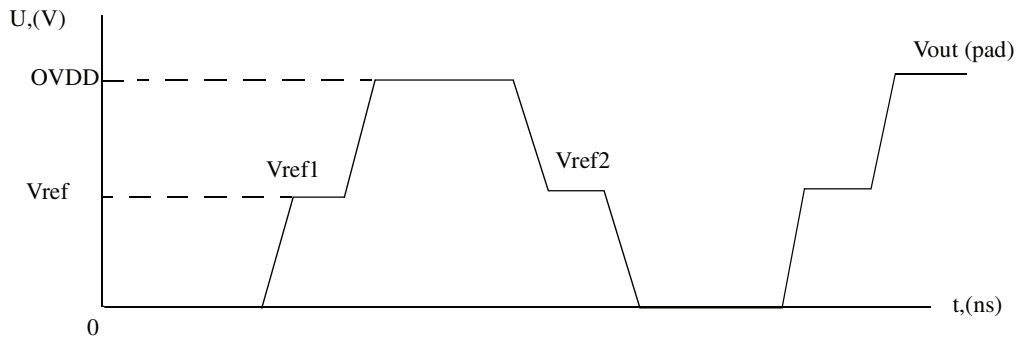
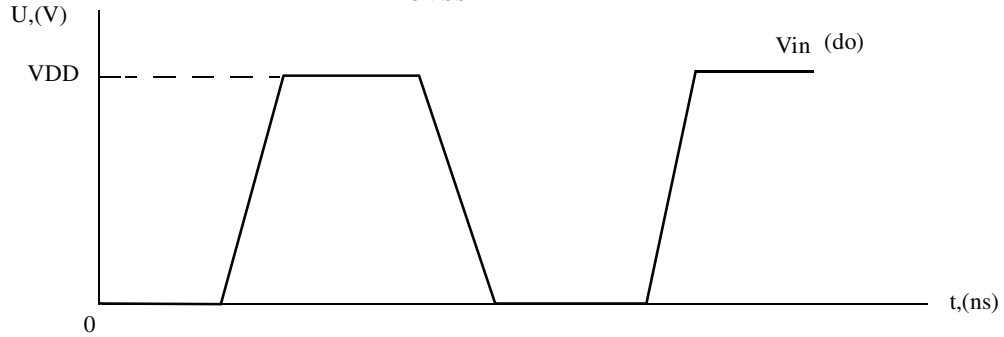
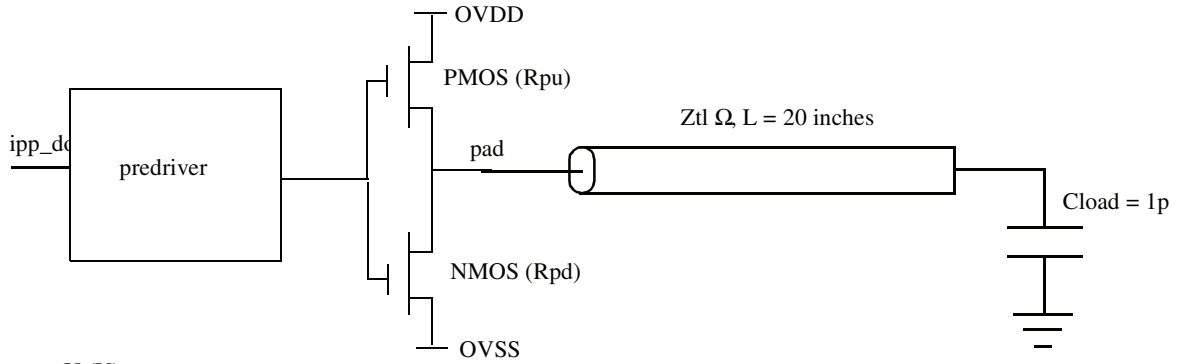
4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O
- MLB I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Z_{tl} attached to I/O pad and incident wave launched into transmission line. R_{pu}/R_{pd} and Z_{tl} form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 9).



$$R_{pu} = \frac{V_{ovdd} - V_{ref1}}{V_{ref1}} \times Z_{tl}$$

$$R_{pd} = \frac{V_{ref2}}{V_{ovdd} - V_{ref2}} \times Z_{tl}$$

Figure 9. Impedance Matching Load for Measurement

4.8.1 GPIO Output Buffer Impedance

Table 35 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 35. GPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	260	Ω
		010	130	
		011	90	
		100	60	
		101	50	
		110	40	
		111	33	

Table 36 shows the GPIO output buffer impedance (OVDD 3.3 V).

Table 36. GPIO Output Buffer Average Impedance (OVDD 3.3 V)

Parameter	Symbol	Drive Strength (DSE)	Typ Value	Unit
Output Driver Impedance	Rdrv	001	150	Ω
		010	75	
		011	50	
		100	37	
		101	30	
		110	25	
		111	20	

4.8.2 DDR I/O Output Buffer Impedance

The LPDDR2 interface fully complies with JESD209-2B LPDDR2 JEDEC standard release June, 2009. The DDR3 interface fully complies with JESD79-3D DDR3 JEDEC standard release April, 2008.

Table 37 shows DDR I/O output buffer impedance of i.MX 6Solo/6DualLite processors.

Table 37. DDR I/O Output Buffer Impedance

Parameter	Symbol	Test Conditions DSE(Drive Strength)	Typical		Unit
			NVCC_DRAM=1.5 V (DDR3) DDR_SEL=11	NVCC_DRAM=1.2 V (LPDDR2) DDR_SEL=10	
Output Driver Impedance	Rdrv	000	Hi-Z	Hi-Z	Ω
		001	240	240	
		010	120	120	
		011	80	80	
		100	60	60	
		101	48	48	
		110	40	40	
		111	34	34	

Note:

1. Output driver impedance is controlled across PVTs using ZQ calibration procedure.

2. Calibration is done against 240 Ω external reference resistor.
3. Output driver impedance deviation (calibration accuracy) is $\pm 5\%$ (max/min impedance) across PVTs.

4.8.3 LVDS I/O Output Buffer Impedance

The LVDS interface complies with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits” for details.

4.8.4 MLB I/O Differential Output Impedance

Table 38 shows MLB I/O differential output impedance of the i.MX 6Solo/6DualLite processors.

Table 38. MLB I/O Differential Output Impedance

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Differential Output Impedance	Zo		1.6 K		—	Ω

4.9 System Modules Timing

This section contains the timing and electrical parameters for the modules in each i.MX 6Solo/6DualLite processor.

4.9.1 Reset Timings Parameters

Figure 10 shows the reset timing and Table 39 lists the timing parameters.

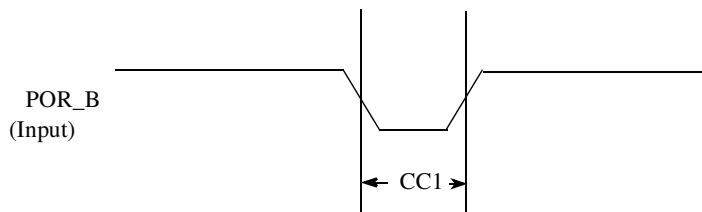


Figure 10. Reset Timing Diagram

Table 39. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid (input slope = 5 ns)	1	—	RTC_XTALI cycle

4.9.2 WDOG Reset Timing Parameters

Figure 11 shows the WDOG reset timing and Table 40 lists the timing parameters.

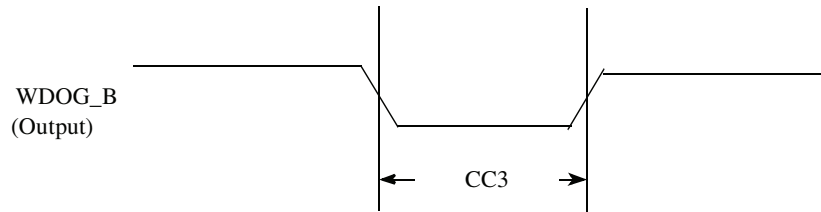


Figure 11. WDOG_B Timing Diagram

Table 40. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 μ s.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3 External Interface Module (EIM)

The following subsections provide information on the EIM.

4.9.3.1 EIM Signal Cross Reference

Table 41 is a guide intended to help the user identify signals in the External Interface Module chapter of the reference manual that are identical to those mentioned in this data sheet.

Table 41. EIM Signal Cross Reference

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx_B	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx

Table 41. EIM Signal Cross Reference (continued)

Reference Manual EIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUXC Controller Chapter Nomenclature
ADV_B	EIM_LBA
ADDR	EIM_A[25:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.9.3.2 EIM Interface Pads Allocation

EIM supports 32-bit, 16-bit and 8-bit devices operating in address/data separate or multiplexed modes. Table 42 provides EIM interface pads allocation in different modes.

Table 42. EIM Internal Module Multiplexing¹

Setup	Non Multiplexed Address/Data Mode							Multiplexed Address/Data mode	
	8 Bit				16 Bit		32 Bit	16 Bit	32 Bit
	MUM = 0, DSZ = 100	MUM = 0, DSZ = 101	MUM = 0, DSZ = 110	MUM = 0, DSZ = 111	MUM = 0, DSZ = 001	MUM = 0, DSZ = 010	MUM = 0, DSZ = 011	MUM = 1, DSZ = 001	MUM = 1, DSZ = 011
A[15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]	WEIM_DA_A [15:0]
A[25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_A [25:16]	WEIM_D [9:0]
D[7:0], EIM_EB0	WEIM_D [7:0]	—	—	—	WEIM_D [7:0]	—	WEIM_D [7:0]	WEIM_DA_A [7:0]	WEIM_DA_A [7:0]
D[15:8], EIM_EB1	—	WEIM_D [15:8]	—	—	WEIM_D [15:8]	—	WEIM_D [15:8]	WEIM_DA_A [15:8]	WEIM_DA_A [15:8]
D[23:16], EIM_EB2	—	—	WEIM_D [24:16]	—	—	WEIM_D [23:16]	EIM_D [23:16]	—	WEIM_D [7:0]
D[31:24], EIM_EB3	—	—	—	WEIM_D [31:24]	—	WEIM_D [31:24]	EIM_D [31:24]	—	WEIM_D [15:8]

¹ For more information on configuration ports mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

4.9.3.3 General EIM Timing-Synchronous Mode

Figure 12, Figure 13, and Table 43 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

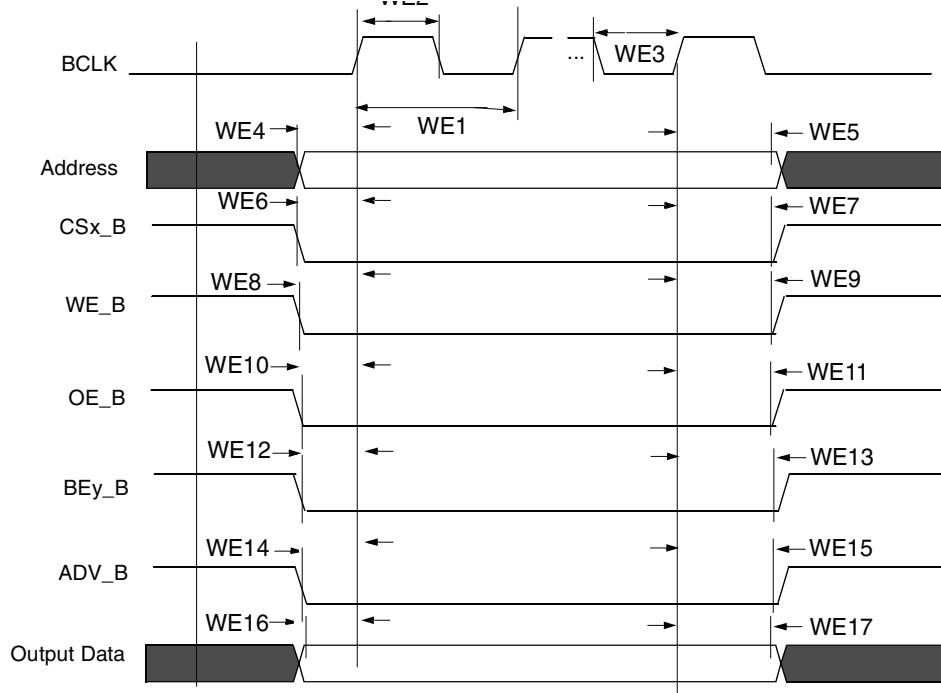


Figure 12. EIM Outputs Timing Diagram

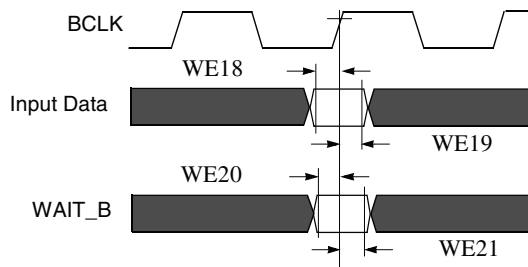


Figure 13. EIM Inputs Timing Diagram

4.9.3.4 Examples of EIM Synchronous Accesses

Table 43. EIM Bus Timing Parameters ¹

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time ²	t	—	2 x t		3 x t	—	4 x t	—
WE2	BCLK Low Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE3	BCLK High Level Width	0.4 x t	—	0.8 x t		1.2 x t	—	1.6 x t	—
WE4	Clock rise to address valid ³	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2	—	4	—	—	—	—	—

Table 43. EIM Bus Timing Parameters (continued)¹

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE19	Input Data hold time from Clock rise	2	—	2	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2	—	4	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2	—	2	—	—	—	—	—

¹ t is the maximal EIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency depends on the fixed/non-fixed latency configuration, whereas the maximum allowed BCLK frequency is:

- Fixed latency for both read and write is 132 MHz.
- Variable latency for read only is 132 MHz.
- Variable latency for write only is 52 MHz.

In variable latency configuration for write, if BCD = 0 & WBCDD = 1 or BCD = 1, axi_clk must be 104 MHz. Write BCD = 1 and 104 MHz axi_clk, will result in a BCLK of 52 MHz. When the clock branch to EIM is decreased to 104 MHz, other buses are impacted which are clocked from this source. See the CCM chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for a detailed clock tree description.

² BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

³ For signal measurements, “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

Figure 14 to Figure 17 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

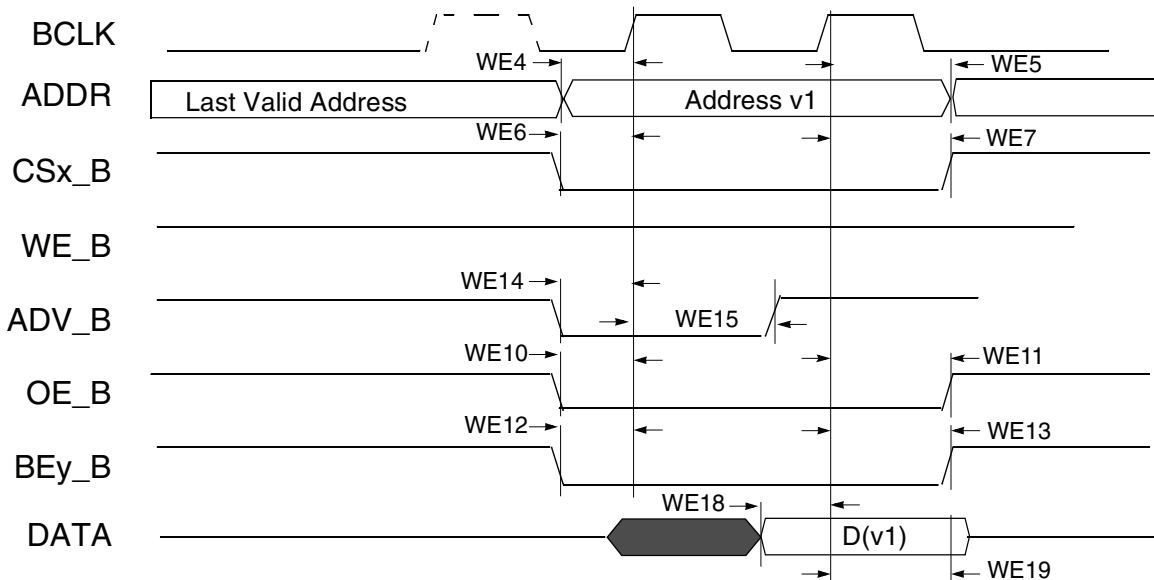


Figure 14. Synchronous Memory Read Access, WSC=1

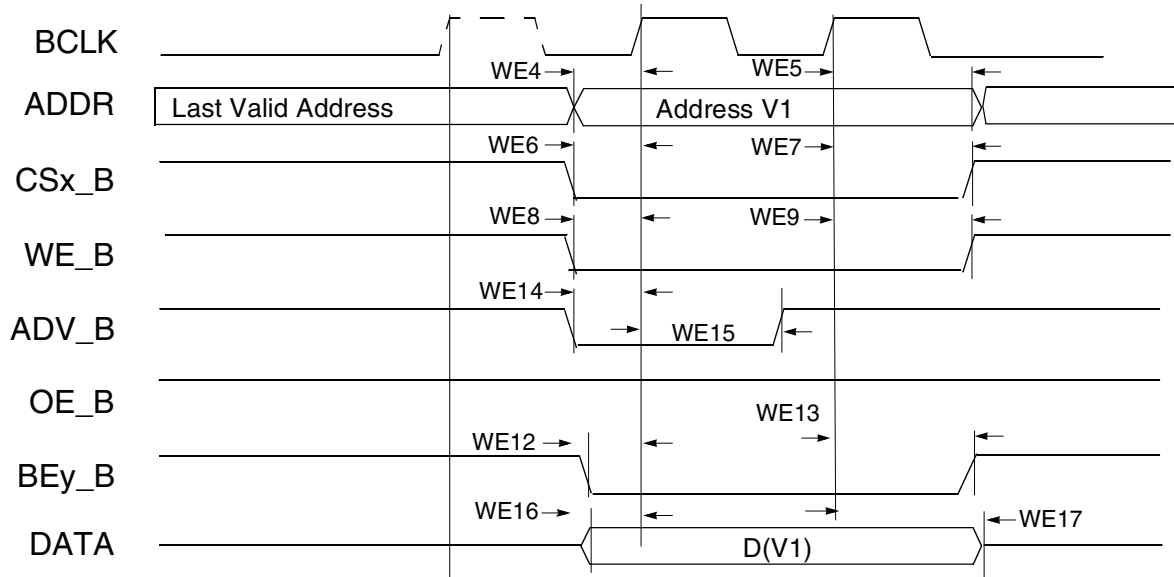


Figure 15. Synchronous Memory, Write Access, WSC=1, WBEA=0 and WADVN=0

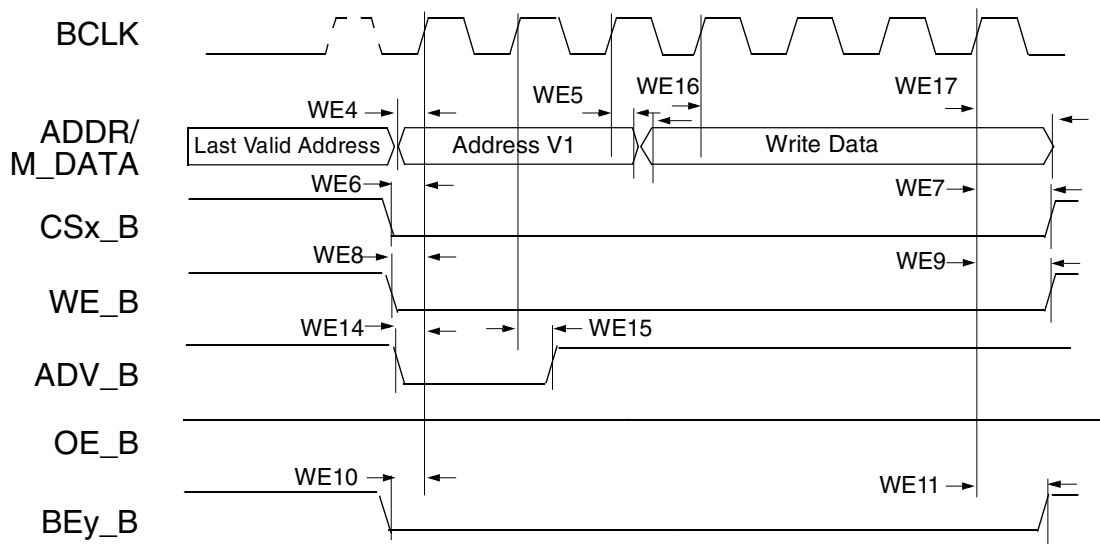


Figure 16. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

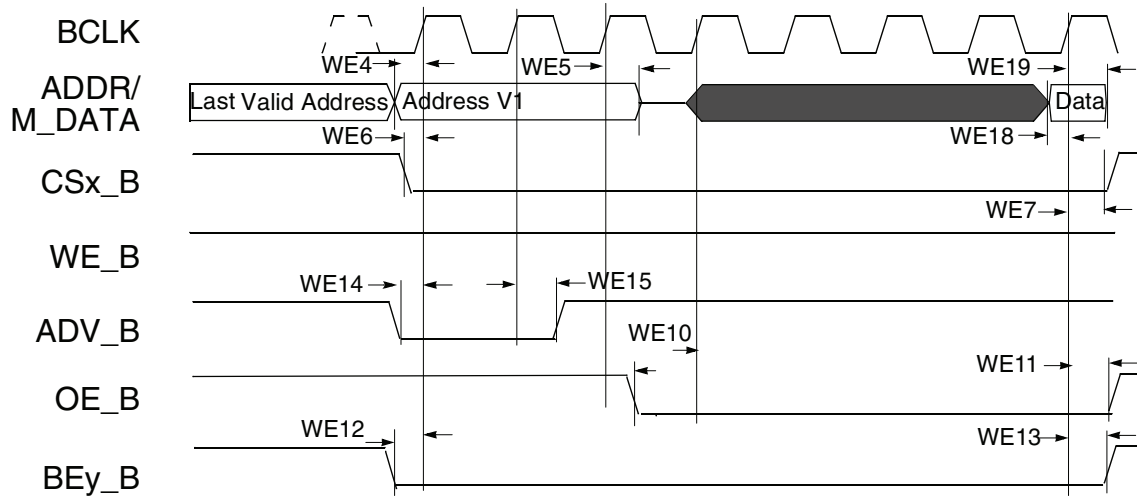


Figure 17. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, OEA=0

4.9.3.5 General EIM Timing-Asynchronous Mode

Figure 18 through Figure 22, and Table 44 help you determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK EIM accesses with corresponding EIM bit fields and the timing parameters mentioned above.

Asynchronous read & write access length in cycles may vary from what is shown in Figure 18 through Figure 21 as RWSC, OEN & CSN is configured differently. See the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* for the EIM programming model.

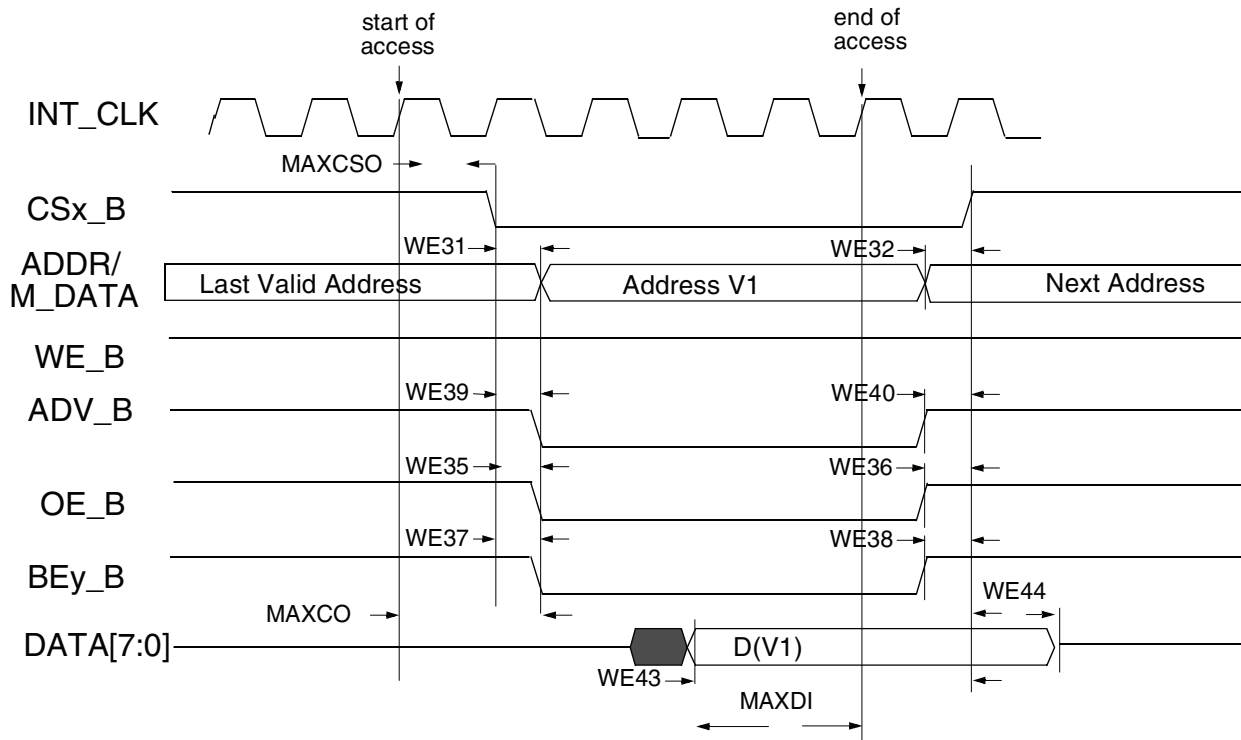


Figure 18. Asynchronous Memory Read Access (RWSC = 5)

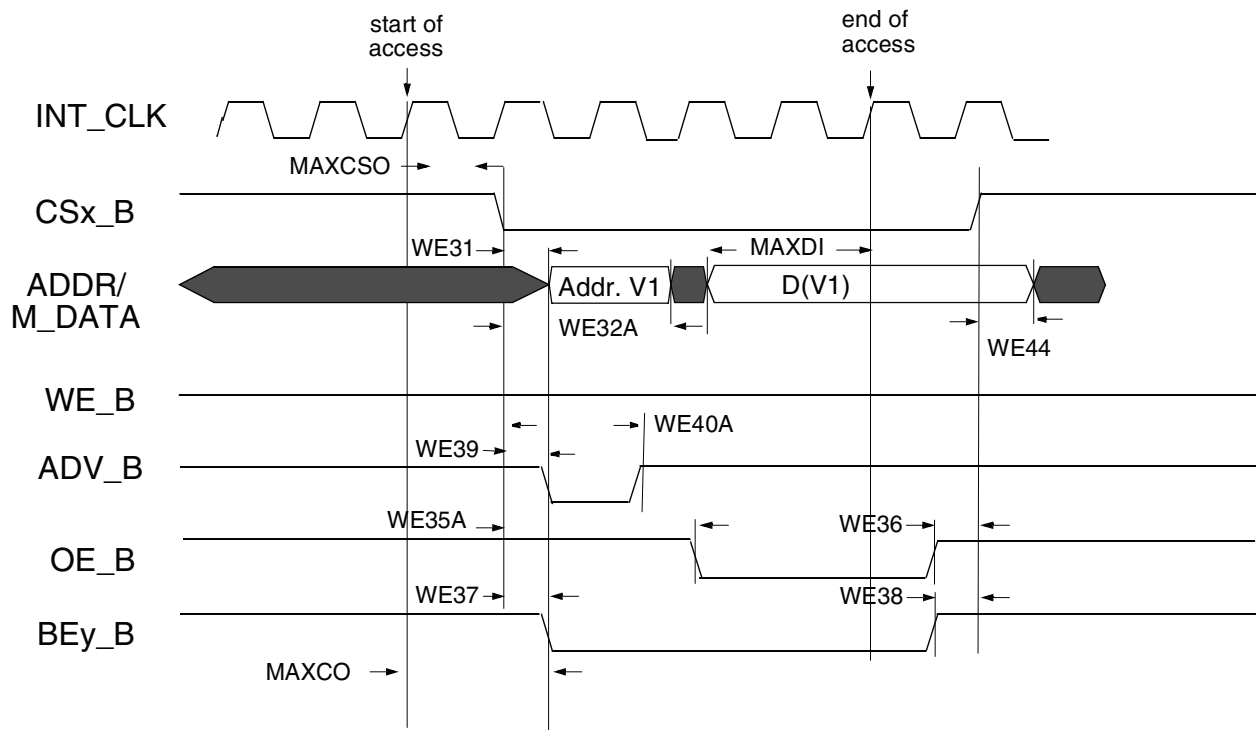


Figure 19. Asynchronous A/D Muxed Read Access (RWSC = 5)

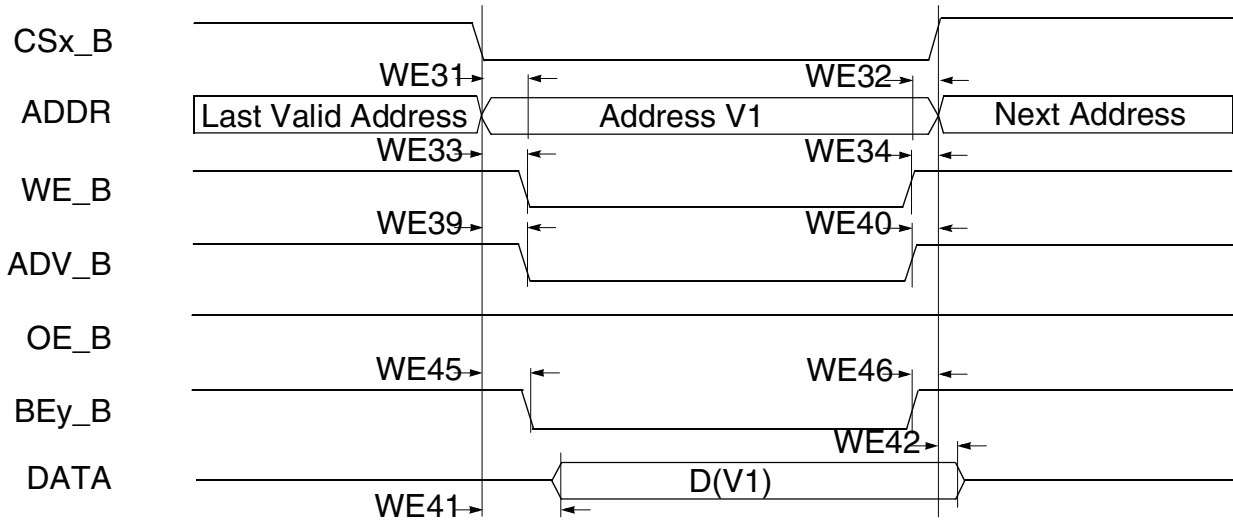


Figure 20. Asynchronous Memory Write Access

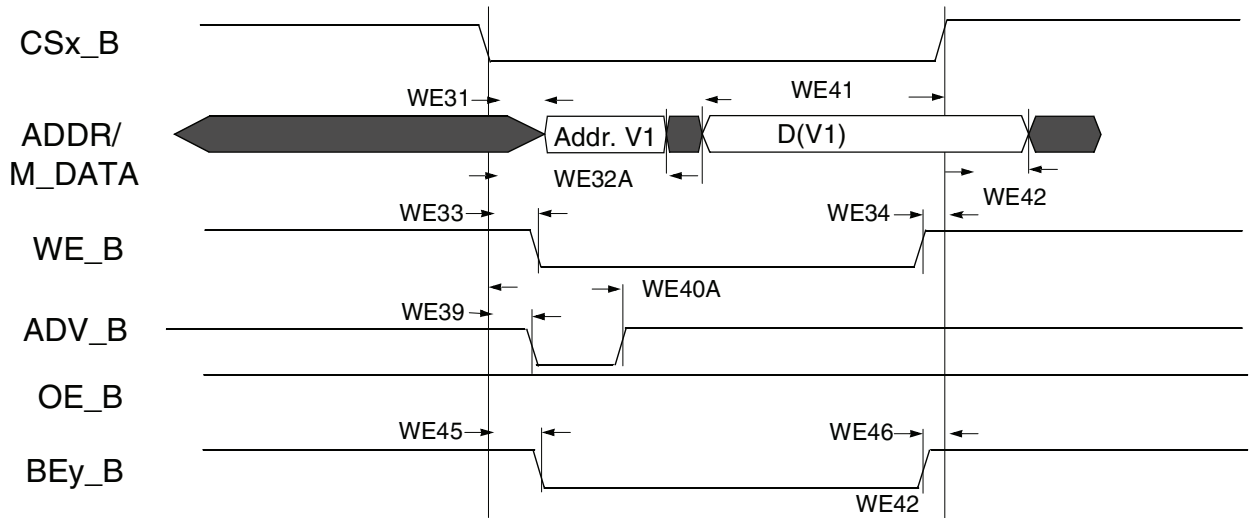


Figure 21. Asynchronous A/D Muxed Write Access

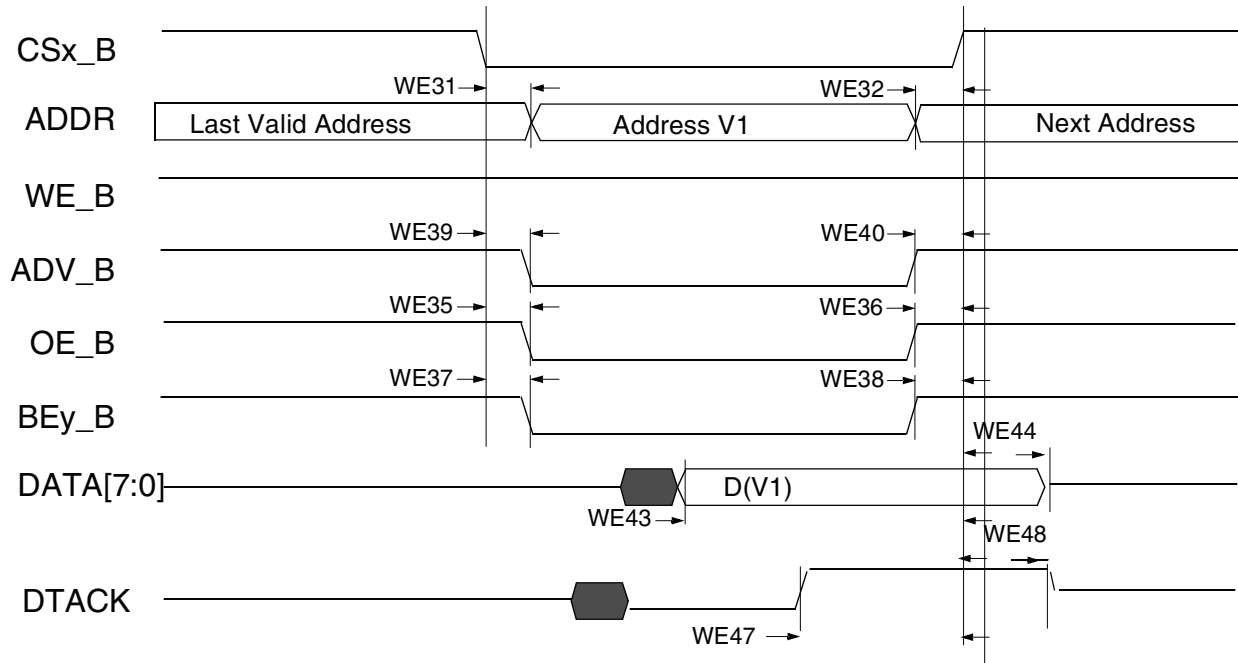


Figure 22. DTACK Read Access (DAP=0)

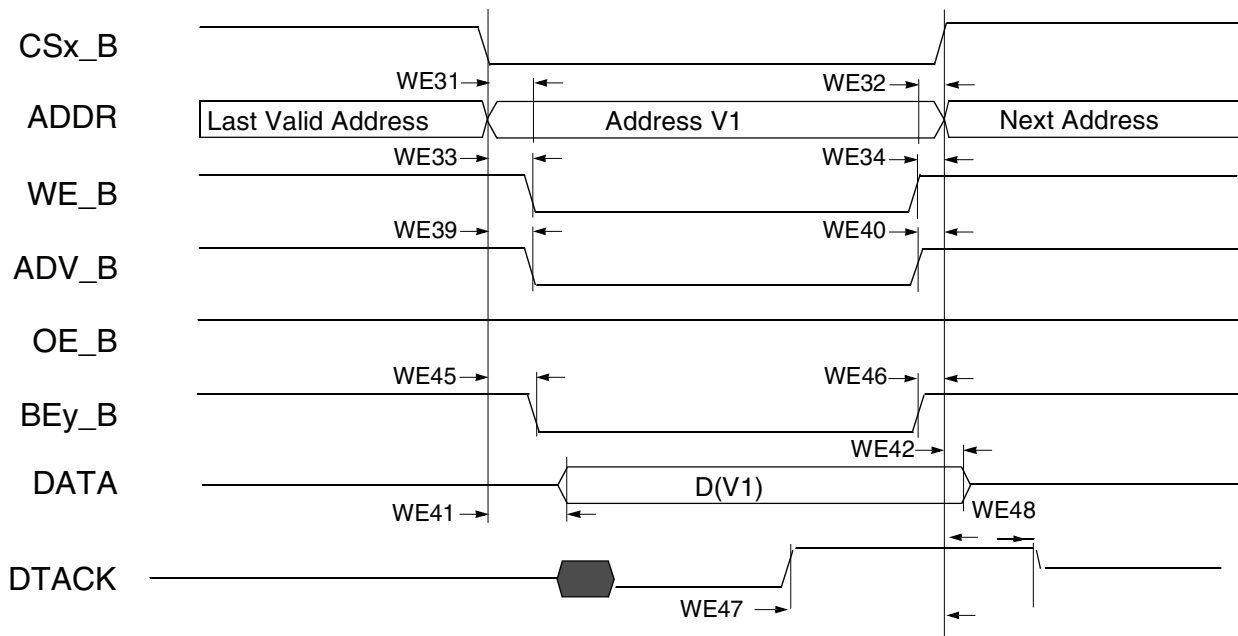


Figure 23. DTACK Write Access (DAP=0)

Electrical Characteristics

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters ¹	Min	Max (If 132 MHz is supported by SoC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA ²	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN ³	—	3 - CSN	ns
WE32A(muxed A/D)	CSx_B valid to Address Invalid	t ⁴ + WE4 - WE7 + (ADV ⁵ + ADVA ⁶ + 1 - CSA)	-3 + (ADV ⁵ + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - WCSA)	—	3 + (WEA - WCSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - WCSN)	—	3 - (WEN - WCSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - RCSA)	—	3 + (OEA - RCSA)	ns
WE35A(muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	-3 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	3 + (OEA + RADVN + RADVA + ADH + 1 - RCSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - RCSN)	—	3 - (OEN - RCSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - RCSA)	—	3 + (RBEA - RCSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - RCSN)	—	3 - (RBEN - RCSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADV _L is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A(muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADV ⁵ + ADVA + 1 - CSA)	-3 + (ADV ⁵ + ADVA + 1 - CSA)	3 + (ADV ⁵ + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A(muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADV ⁵ + WADVA + ADH + 1 - WCSA)	—	3 + (WADV ⁵ + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCSO	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

Table 44. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters ¹	Min	Max (If 132 MHz is supported by SoC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - WCSA)	—	3 + (WBEA - WCSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - WCSN)	—	-3 + (WBEN - WCSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization	10	—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

¹ For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.

² In this table, CSA means WCSA when write operation or RCSA when read operation.

³ In this table, CSN means WCSN when write operation or RCSN when read operation.

⁴ t is axi_clk cycle time.

⁵ In this table, ADVN means WADV when write operation or RADVN when read operation.

⁶ In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4 DDR SDRAM Specific Parameters (DDR3/DDR3L and LPDDR2)

4.9.4.1 DDR3/DDR3L Parameters

Figure 24 shows the basic timing parameters. The timing parameters for this diagram appear in Table 45.

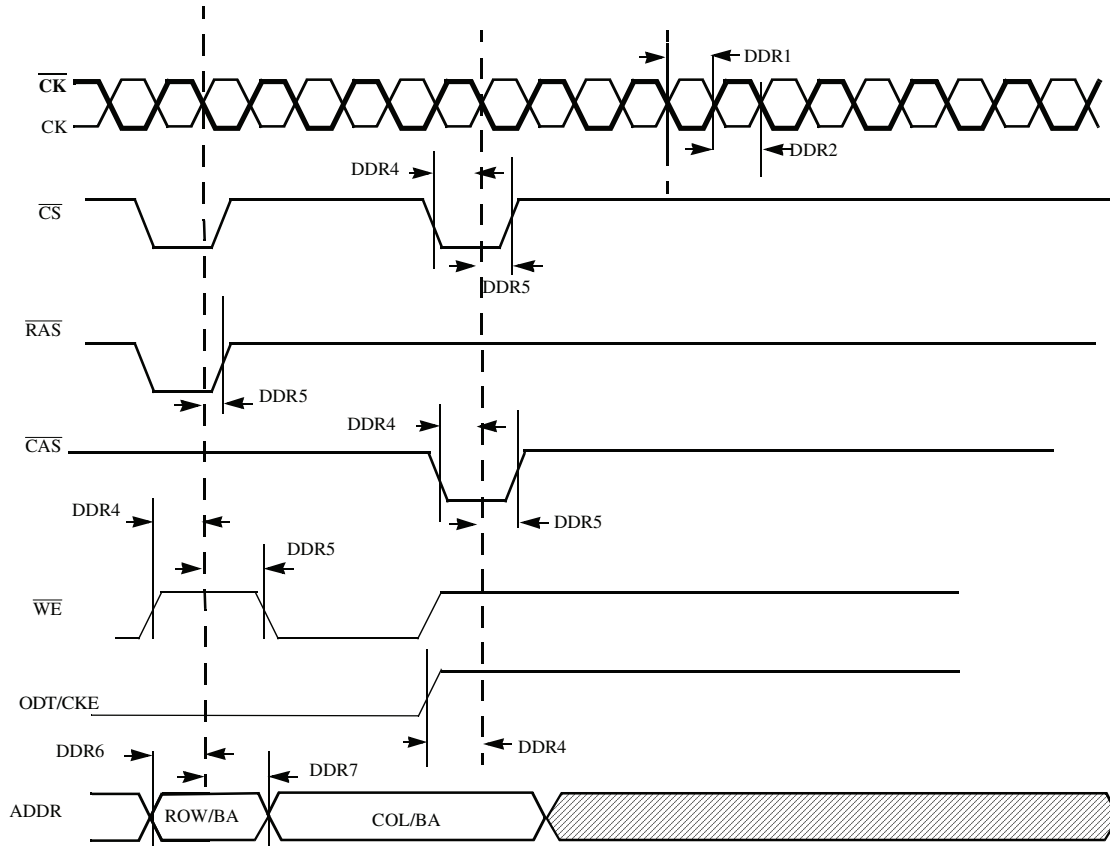


Figure 24. DDR3 Command and Address Timing Parameters

Table 45. DDR3/DDR3L Timing Parameter Table

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tck
DDR2	CK clock low-level width	tCL	0.47	0.53	tck
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	800	—	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	580	—	ps
DDR6	Address output setup time	tIS	800	—	ps
DDR7	Address output hold time	tIH	580	—	ps

- ¹ All measurements are in reference to Vref level.
- ² Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 25 shows the DDR3/DDR3L write timing parameters. The timing parameters for this diagram appear in Table 46.

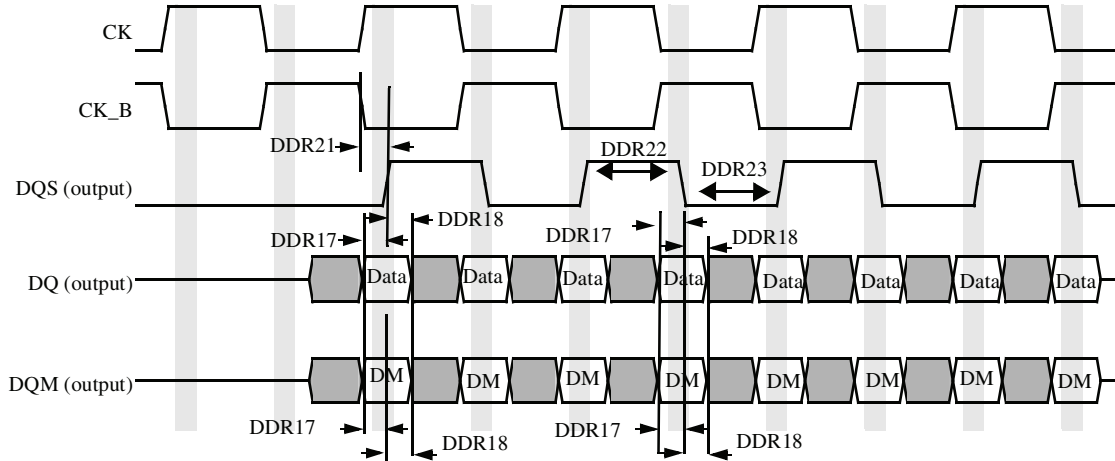


Figure 25. DDR3/DDR3L Write Cycle

Table 46. DDR3/DDR3L Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	420	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	345	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR23	DQS low level width	tDQSL	0.45	0.55	tCK

- ¹ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.
- ² All measurements are in reference to Vref level.
- ³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Electrical Characteristics

Figure 26 shows the read DDR3/DDR3L timing parameters. The timing parameters for this diagram appear in Table 47.

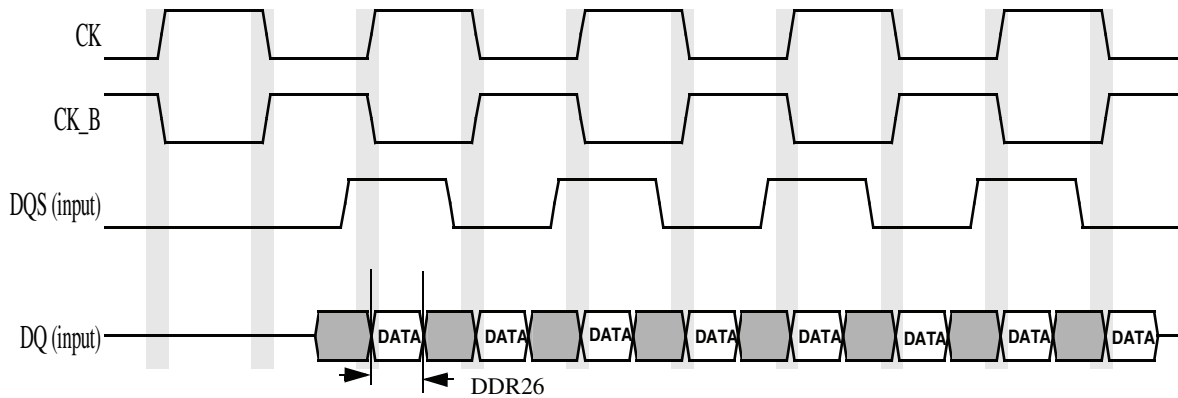


Figure 26. DDR3/DDR3L Read Cycle

Table 47. DDR3/DDR3L Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	—	450	—	ps

- ¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.
- ² All measurements are in reference to Vref level.
- ³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.9.4.2 LPDDR2 Parameters

Figure 27 shows the basic timing parameters. The timing parameters for this diagram appear in Table 48.

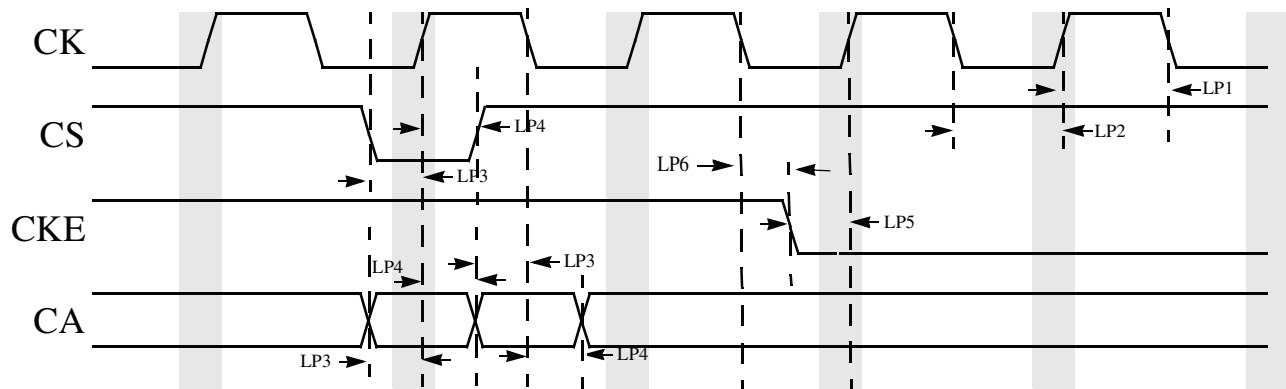


Figure 27. LPDDR2 Command and Address Timing Parameters

Table 48. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	tck
LP2	SDRAM clock low-level width	tCL	0.45	0.55	tck
LP3	CA, CS setup time	tIS	380	—	ps
LP4	CA, CS hold time	tIH	380	—	ps
LP5	CKE setup time	tISCKE	770	—	tck
LP6	CKE hold time	tIHCKE	770	—	tck

¹ All measurements are in reference to Vref level.

² Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Electrical Characteristics

Figure 28 shows the write timing parameters. The timing parameters for this diagram appear in Table 49.

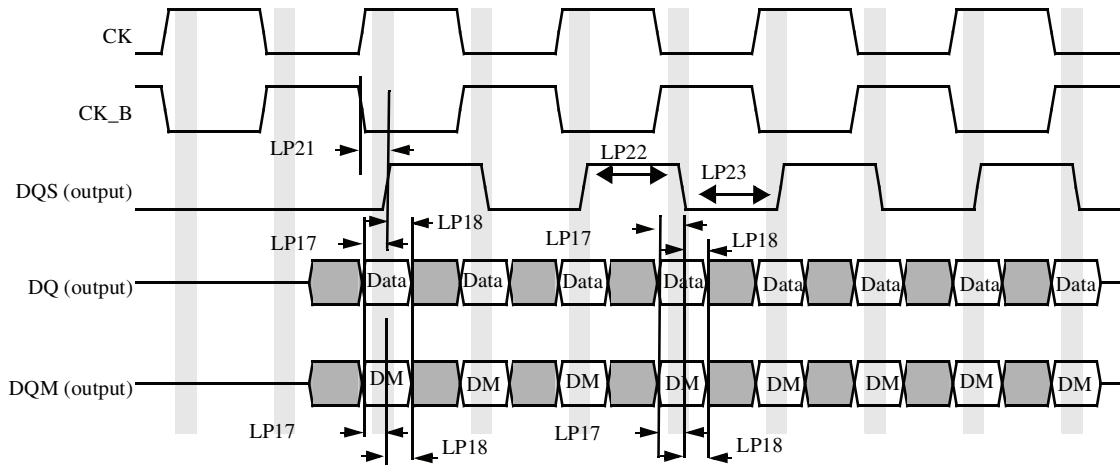


Figure 28. LPDDR2 Write Cycle

Table 49. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	t _{DS}	375	—	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	t _{DH}	375	—	ps
LP21	DQS latching rising transitions to associated clock edges	t _{DQSS}	-0.25	+0.25	tCK
LP22	DQS high level width	t _{DQSH}	0.4	-	tCK
LP23	DQS low level width	t _{DQSL}	0.4	-	tCK

- ¹ To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.
- ² All measurements are in reference to V_{ref} level.
- ³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

Figure 29 shows the read timing parameters. The timing parameters for this diagram appear in Table 50.

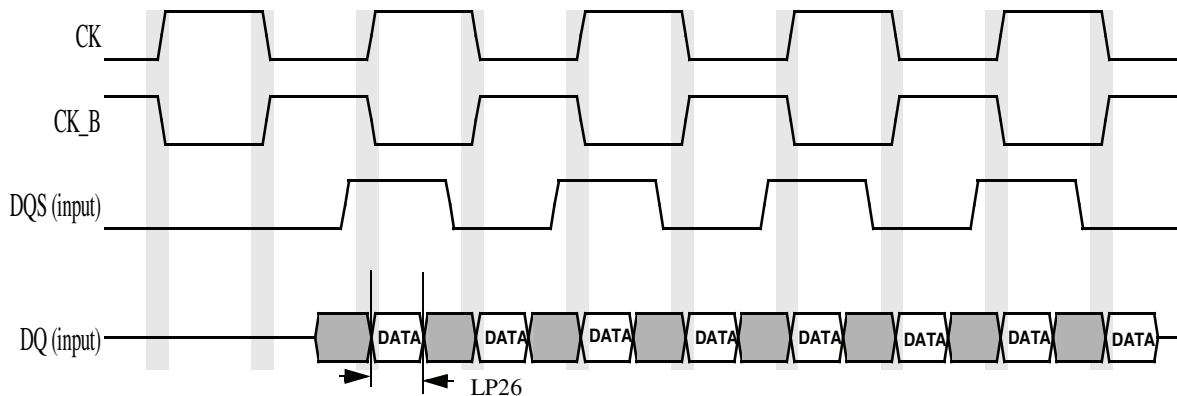


Figure 29. LPDDR2 Read Cycle

Table 50. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	—	270	—	ps

¹ To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

² All measurements are in reference to Vref level.

³ Measurements were done using balanced load and 25 Ω resistor from outputs to VDD_REF.

4.10 General-Purpose Media Interface (GPMI) Timing

The i.MX 6Solo/6DualLite GPMI controller is a flexible interface NAND Flash controller with 8-bit data width, up to 200 MB/s I/O speed and individual chip select.

It supports Asynchronous timing mode, Source Synchronous timing mode and Samsung Toggle timing mode separately described in the following subsections.

4.10.1 Asynchronous Mode AC Timing (ONFI 1.0 Compatible)

Asynchronous mode AC timings are provided as multiplications of the clock cycle and fixed delay. The maximum I/O speed of GPMI in asynchronous mode is about 50 MB/s. Figure 30 through Figure 33 depicts the relative timing between GPMI signals at the module level for different operations under asynchronous mode. Table 51 describes the timing parameters (NF1–NF17) that are shown in the figures.

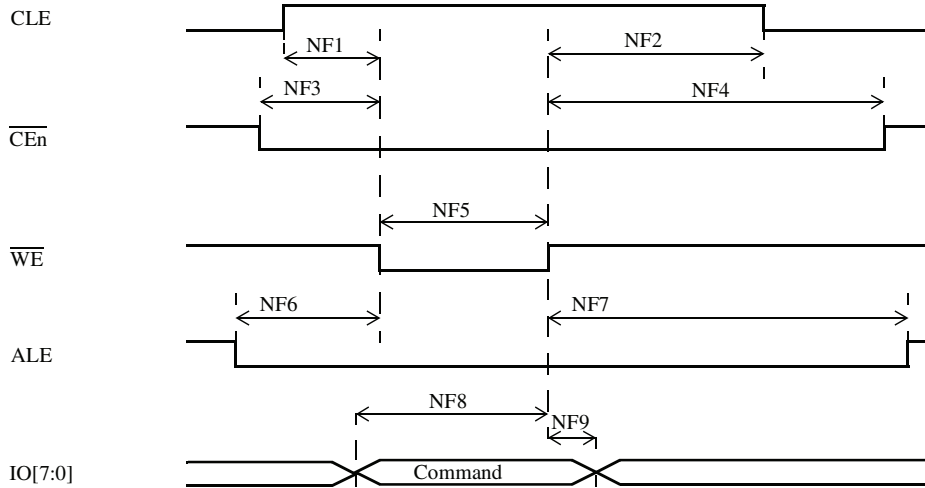


Figure 30. Command Latch Cycle Timing Diagram

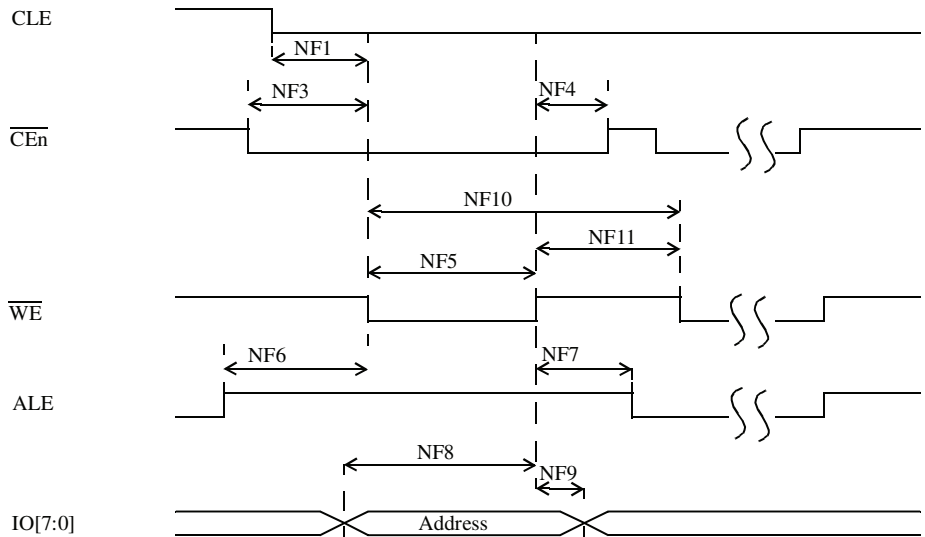


Figure 31. Address Latch Cycle Timing Diagram

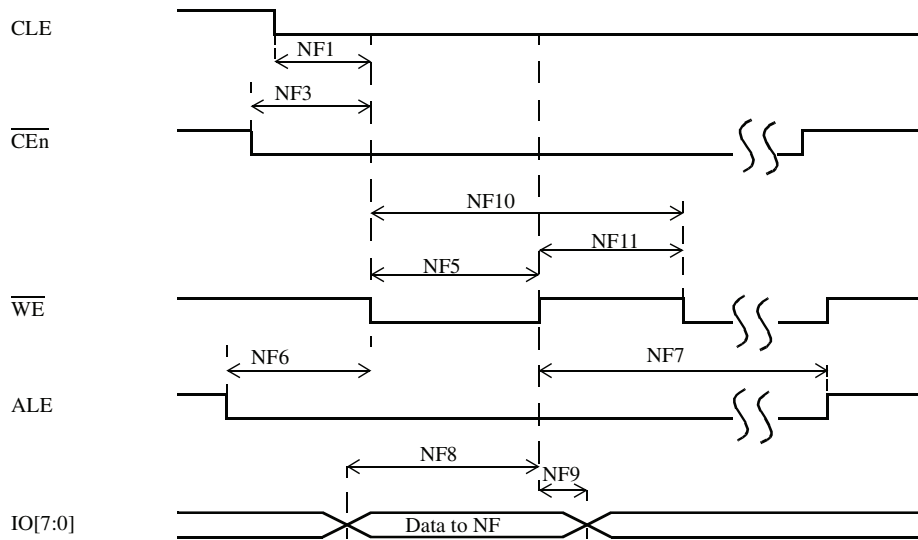


Figure 32. Write Data Latch Cycle Timing Diagram

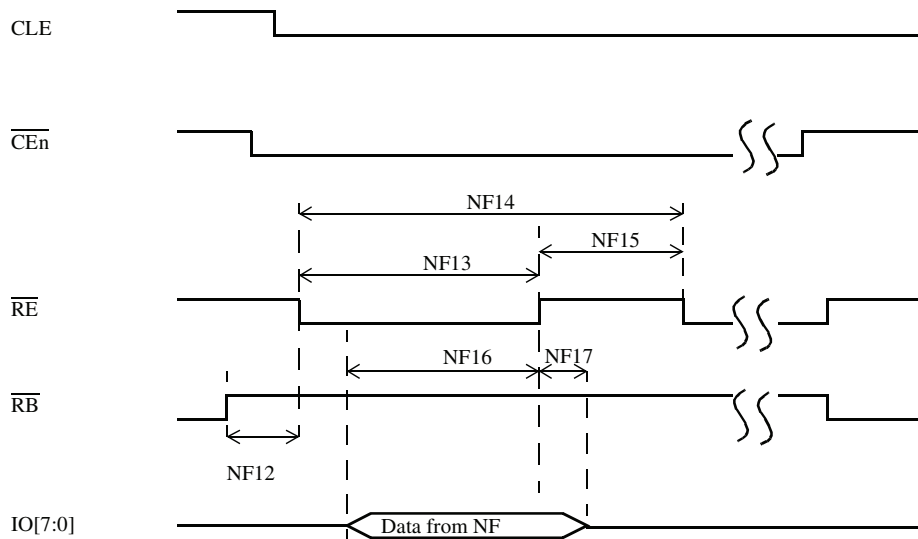


Figure 33. Read Data Latch Cycle Timing Diagram

Table 51. Asynchronous Mode Timing Parameters¹

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock ≈ 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF1	CLE setup time	tCLS	(AS+1) x T	—	10	—	ns
NF2	CLE hold time	tCLH	(DH+1) x T	—	20	—	ns
NF3	$\overline{\text{CEn}}$ setup time	tCS	(AS+1) x T	—	10	—	ns
NF4	$\overline{\text{CE}}$ hold time	tCH	(DH+1) x T	—	20	—	ns

Table 51. Asynchronous Mode Timing Parameters¹ (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Example Timing for GPMI Clock \approx 100 MHz T = 10 ns		Unit
			Min.	Max.	Min.	Max.	
NF5	\overline{WE} pulse width	tWP	DS x T		10		ns
NF6	ALE setup time	tALS	(AS+1) x T	—	10	—	ns
NF7	ALE hold time	tALH	(DH+1) x T	—	20	—	ns
NF8	Data setup time	tDS	DS x T	—	10	—	ns
NF9	Data hold time	tDH	DH x T	—	10	—	ns
NF10	Write cycle time	tWC	(DS+DH) x T		20		ns
NF11	\overline{WE} hold time	tWH	DH x T		10		ns
NF12	Ready to \overline{RE} low	tRR	(AS+1) x T	—	10	—	ns
NF13	\overline{RE} pulse width	tRP	DS x T	—	10	—	ns
NF14	READ cycle time	tRC	(DS+DH) x T	—	20	—	ns
NF15	\overline{RE} high hold time	tREH	DH x T		10	—	ns
NF16	Data setup on read	tDSR	N/A		10	—	ns
NF17	Data hold on read	tDHR	N/A		10	—	ns

¹ GPMI's Async Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING0_ADDRESS_SETUP, HW_GPMI_TIMING0_DATA_SETUP, and HW_GPMI_TIMING0_DATA_HOLD. This AC timing depends on these registers' settings. In the above table, we use AS/DS/DH to represent each of these settings.

2) AS minimum value could be 0, while DS/DH minimum value is 1.

3) T represents for the GPMI clock period.

In EDO mode (Figure 33), NF16/NF17 are different from the definition in non-EDO mode (Figure 32). They are called tREA/tRHOH (RE# access time/RE# HIGH to output hold). The typical value for them are 16 ns (max for tREA)/15 ns (min for tRHOH) at 50 MB/s EDO mode. In EDO mode, GPMI will sample IO[7:0] at rising edge of delayed RE provided by an internal DPLL. The delay value can be controlled by GPMI_CTRL1.RDN_DELAY (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). The typical value of this control register is 0x8 at 50 MT/s EDO mode. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 34 to Figure 36 show the write and read timing of Source Synchronous Mode.

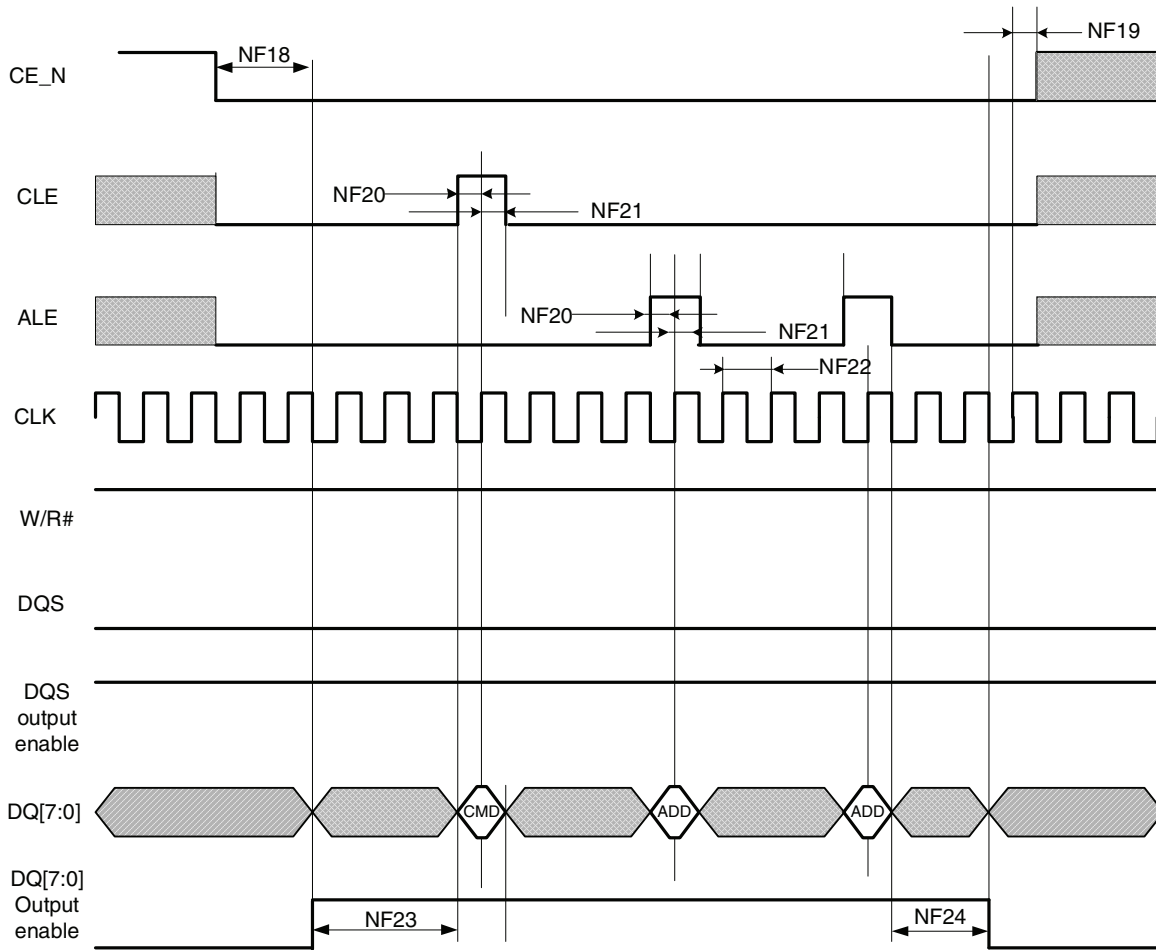


Figure 34. Source Synchronous Mode Command and Address Timing Diagram

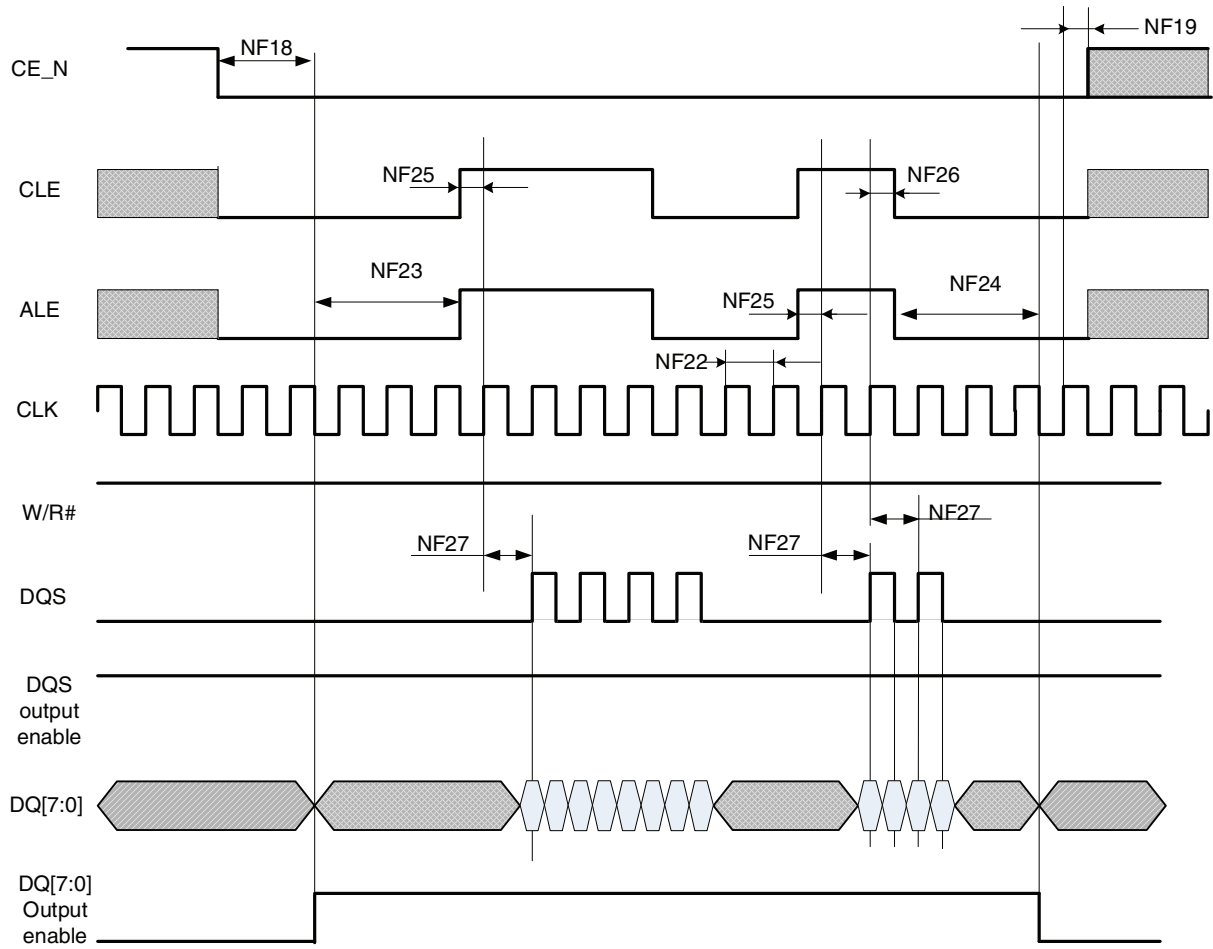


Figure 35. Source Synchronous Mode Data Write Timing Diagram

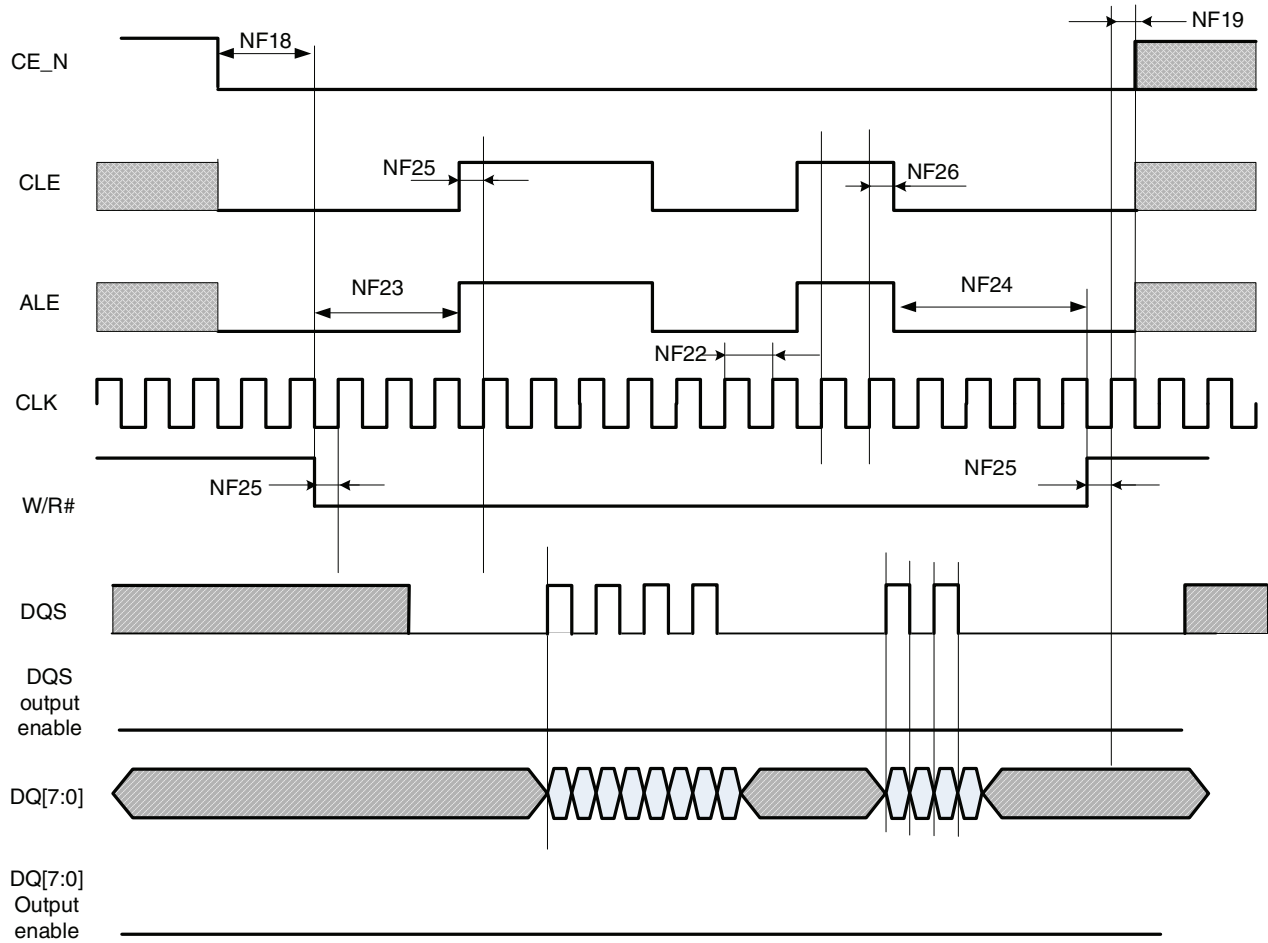


Figure 36. Source Synchronous Mode Data Read Timing Diagram

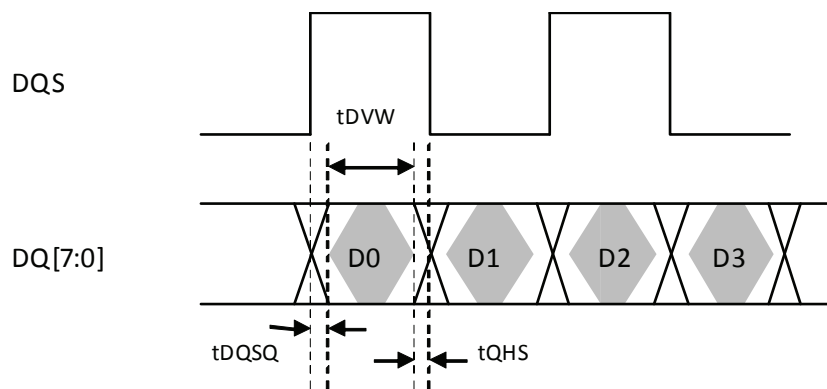


Figure 37. DQS/DQ Read Valid Window

Table 52. Source Synchronous Mode Timing Parameters¹

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	5	--	ns
NF23	preamble delay	tPRE	PRE_DELAY x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALs	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns
NF27	Data input to first DQS latching transition	tDQSS	tCK	—	ns

¹ GPMI's Sync Mode output timing could be controlled by module's internal registers, say HW_GPMI_TIMING2_CE_DELAY, HW_GPMI_TIMING2_PRE_DELAY, and HW_GPMI_TIMING2_POST_DELAY. This AC timing depends on these registers' settings. In the above table, we use CE_DELAY/PRE_DELAY/POST_DELAY to represent each of these settings.

For DDR Source sync mode, [Figure 37](#) shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 0.85ns (max) and 1ns (max) for tQHS at 200MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which can be provided by an internal DPLL. The delay value can be controlled by GPMI register GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET(see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value of this register is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.10.3 Samsung Toggle Mode AC Timing

4.10.3.1 Command and Address Timing

NOTE

Samsung Toggle Mode command and address timing is the same as ONFI 1.0 compatible Async mode AC timing. See [Section 4.10.1, “Asynchronous Mode AC Timing \(ONFI 1.0 Compatible\),”](#) for details.

4.10.3.2 Read and Write Timing

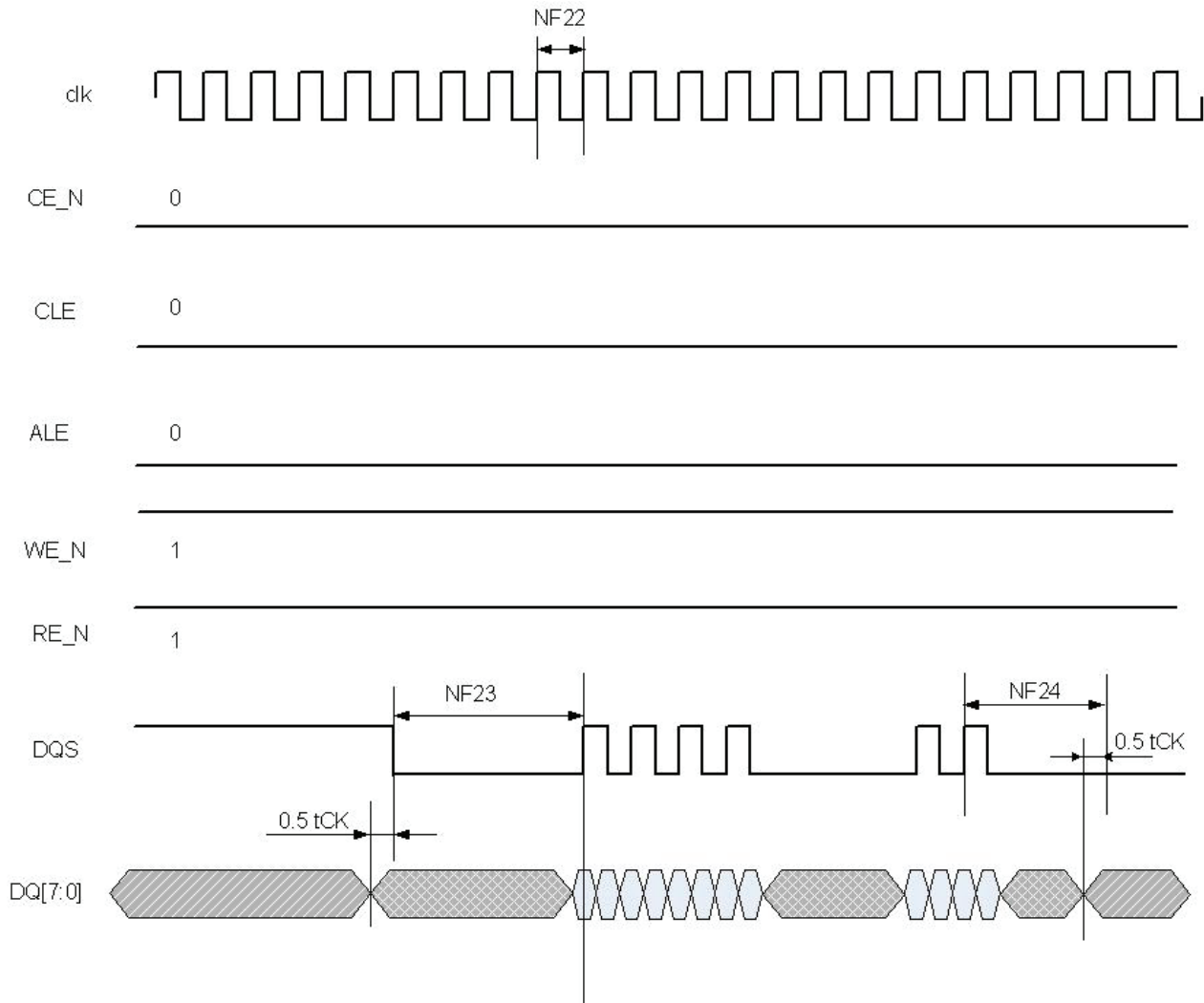


Figure 38. Samsung Toggle Mode Data Write Timing

Electrical Characteristics

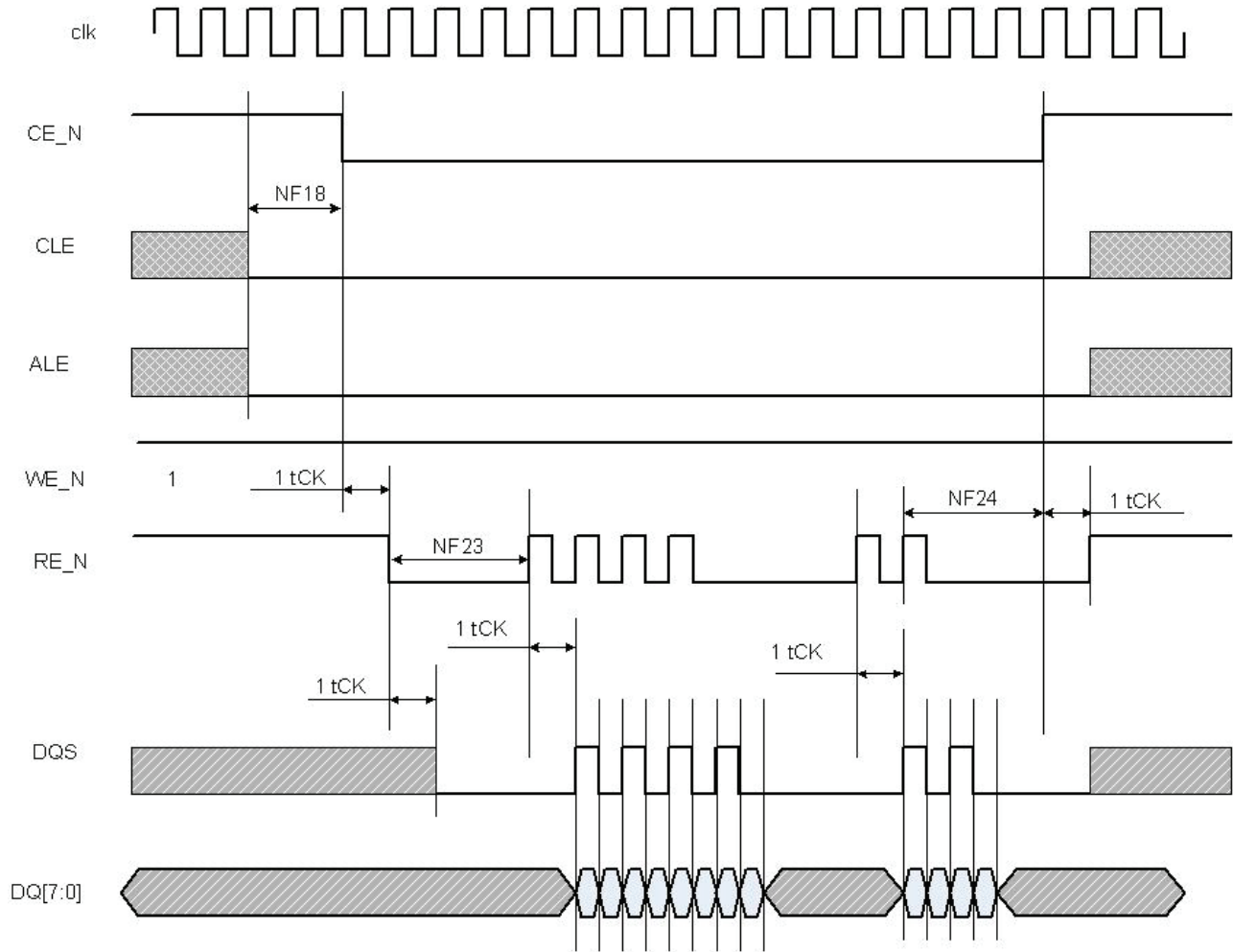


Figure 39. Samsung Toggle Mode Data Read Timing

Table 53. Samsung Toggle Mode Timing Parameters

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF18	CE# access time	tCE	CE_DELAY x tCK	—	ns
NF19	CE# hold time	tCH	0.5 x tCK	—	ns
NF20	Command/address DQ setup time	tCAS	0.5 x tCK	—	ns
NF21	Command/address DQ hold time	tCAH	0.5 x tCK	—	ns
NF22	clock period	tCK	7.5	--	ns

Table 53. Samsung Toggle Mode Timing Parameters (continued)

ID	Parameter	Symbol	Timing T = GPMI Clock Cycle		Unit
			Min.	Max.	
NF23	preamble delay	tPRE	(PRE_DELAY+1) x tCK	—	ns
NF24	postamble delay	tPOST	POST_DELAY x tCK	—	ns
NF25	CLE and ALE setup time	tCALS	0.5 x tCK	—	ns
NF26	CLE and ALE hold time	tCALH	0.5 x tCK	—	ns

For DDR Toggle mode, [Figure 37](#) shows the timing diagram of DQS/DQ read valid window. The typical value of tDQSQ is 1.4 ns(max) and 1.4 ns (max) for tQHS at 133 MB/s. GPMI will sample DQ[7:0] at both rising and falling edge of an delayed DQS signal, which is provided by an internal DPLL. The delay value of this register can be controlled by GPMI register

GPMI_READ_DDR_DLL_CTRL.SLV_DLY_TARGET (see the GPMI chapter of the i.MX 6Solo/6DualLite reference manual). Generally, the typical delay value is equal to 0x7 which means 1/4 clock cycle delay expected. But if the board delay is big enough and cannot be ignored, the delay value should be made larger to compensate the board delay.

4.11 External Peripheral Interface Parameters

The following subsections provide information on external peripheral interfaces.

4.11.1 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio, and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is governed by the SSI module. For more information, see the respective SSI electrical specifications found within this document.

4.11.2 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI blocks. The ECSPI have separate timing parameters for master and slave modes.

4.11.2.1 ECSPI Master Mode Timing

Figure 40 depicts the timing of ECSPI in master mode. Table 54 lists the ECSPI master mode timing characteristics.

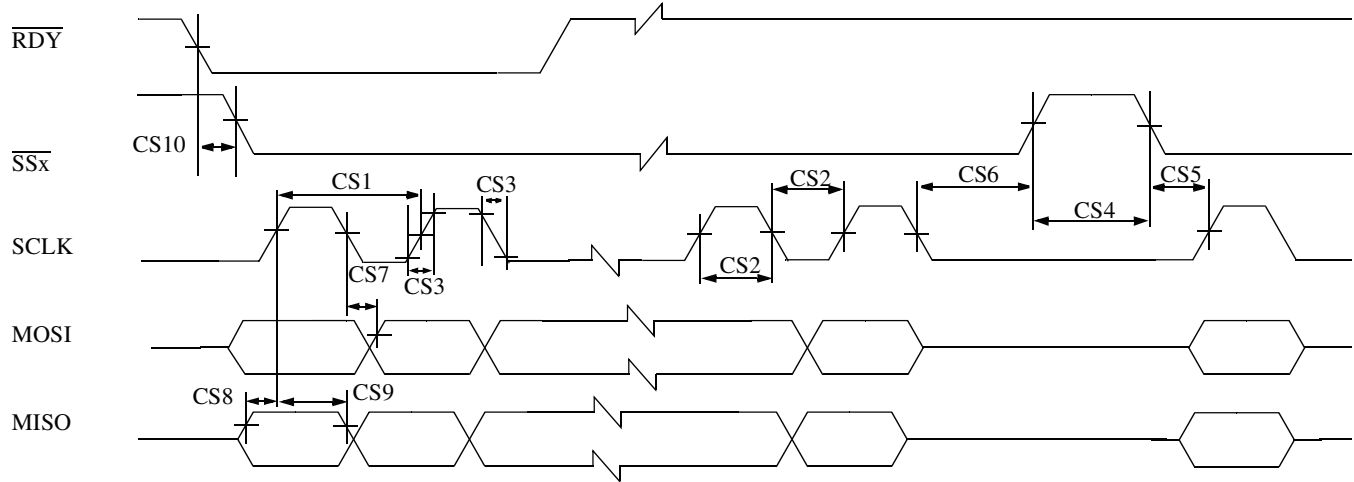


Figure 40. ECSPI Master Mode Timing Diagram

Table 54. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time–Read SCLK Cycle Time–Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time–Read SCLK High or Low Time–Write	t_{sw}	21.5 7	—	ns
CS3	SCLK Rise or Fall ¹	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	Half SCLK period - 4	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	Half SCLK period - 2	—	ns
CS7	MOSI Propagation Delay ($C_{LOAD} = 20\text{ pF}$)	t_{PDmosi}	-1	1	ns
CS8	MISO Setup Time	t_{Smiso}	18	—	ns
CS9	MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	RDY to SSx Time ²	t_{SDRY}	5	—	ns

¹ See specific I/O AC parameters Section 4.7, “I/O AC Parameters.”

² SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.11.2.2 ECSPi Slave Mode Timing

Figure 41 depicts the timing of ECSPi in slave mode. Table 55 lists the ECSPi slave mode timing characteristics.

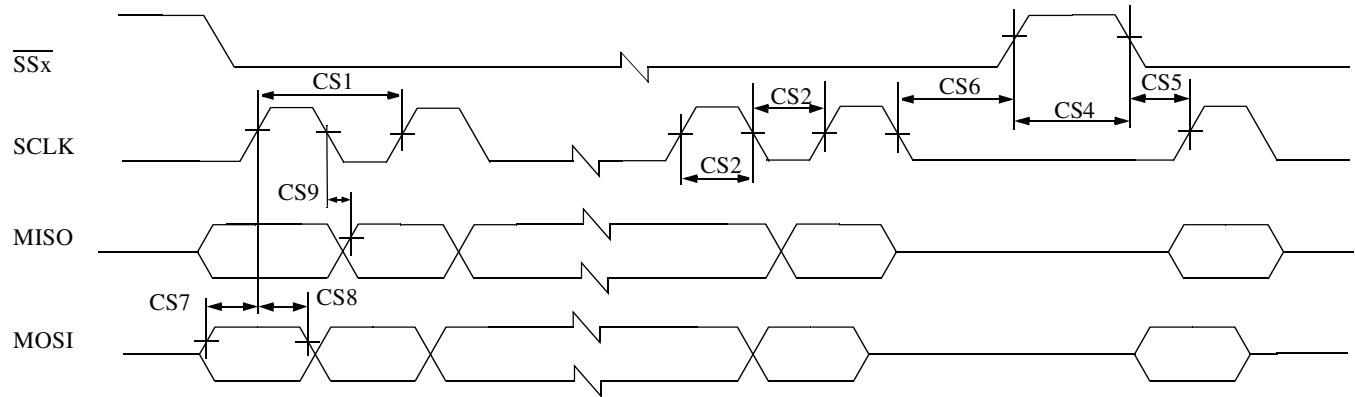


Figure 41. ECSPi Slave Mode Timing Diagram

Table 55. ECSPi Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time—Read SCLK Cycle Time—Write	t_{clk}	43 15	—	ns
CS2	SCLK High or Low Time—Read SCLK High or Low Time—Write	t_{sw}	21.5 7	—	ns
CS4	SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	MISO Propagation Delay ($C_{LOAD} = 20 \text{ pF}$)	t_{PDmiso}	4	19	ns

4.11.3 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. Table 56 shows the interface timing values. The number field in the table refers to timing signals found in Figure 42 and Figure 43.

Table 56. Enhanced Serial Audio Interface (ESAI) Timing

No.	Characteristics ^{1,2}	Symbol	Expression ²	Min	Max	Condition ³	Unit
62	Clock cycle ⁴	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	30.0 30.0	— —	i ck i ck	ns
63	Clock high period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
64	Clock low period: • For internal clock • For external clock	— —	$2 \times T_C - 9.0$ $2 \times T_C$	6 15	— —	— —	ns
65	SCKR rising edge to FSR out (bl) high	— —	— —	— —	17.0 7.0	x ck i ck a	ns
66	SCKR rising edge to FSR out (bl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
67	SCKR rising edge to FSR out (wr) high ⁵	— —	— —	— —	19.0 9.0	x ck i ck a	ns
68	SCKR rising edge to FSR out (wr) low ⁵	— —	— —	— —	19.0 9.0	x ck i ck a	ns
69	SCKR rising edge to FSR out (wl) high	— —	— —	— —	16.0 6.0	x ck i ck a	ns
70	SCKR rising edge to FSR out (wl) low	— —	— —	— —	17.0 7.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) falling edge	— —	— —	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR falling edge	— —	— —	3.5 9.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR falling edge ⁵	— —	— —	2.0 12.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR falling edge	— —	— —	2.0 12.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR falling edge	— —	— —	2.5 8.5	— —	x ck i ck a	ns
78	SCKT rising edge to FST out (bl) high	— —	— —	— —	18.0 8.0	x ck i ck	ns
79	SCKT rising edge to FST out (bl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
80	SCKT rising edge to FST out (wr) high ⁵	— —	— —	— —	20.0 10.0	x ck i ck	ns

Table 56. Enhanced Serial Audio Interface (ESAI) Timing (continued)

No.	Characteristics ^{1,2}	Symbol	Expression ²	Min	Max	Condition ³	Unit
81	SCKT rising edge to FST out (wr) low ⁵	— —	— —	— —	22.0 12.0	x ck i ck	ns
82	SCKT rising edge to FST out (wl) high	— —	— —	— —	19.0 9.0	x ck i ck	ns
83	SCKT rising edge to FST out (wl) low	— —	— —	— —	20.0 10.0	x ck i ck	ns
84	SCKT rising edge to data out enable from high impedance	— —	— —	— —	22.0 17.0	x ck i ck	ns
86	SCKT rising edge to data out valid	— —	— —	— —	18.0 13.0	x ck i ck	ns
87	SCKT rising edge to data out high impedance ^{6,7}	— —	— —	— —	21.0 16.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT falling edge ⁵	— —	— —	2.0 18.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT falling edge	— —	— —	2.0 18.0	— —	x ck i ck	ns
91	FST input hold time after SCKT falling edge	— —	— —	4.0 5.0	— —	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	$2 \times T_C$	15	—	—	ns
96	HCKT input rising edge to SCKT output	—	—	—	18.0	—	ns
97	HCKR input rising edge to SCKR output	—	—	—	18.0	—	ns

- ¹ i ck = internal clock
x ck = external clock
i ck a = internal clock, asynchronous mode
(asynchronous implies that SCKT and SCKR are two different clocks)
i ck s = internal clock, synchronous mode
(synchronous implies that SCKT and SCKR are the same clock)

- ² bl = bit length
wl = word length
wr = word length relative

- ³ SCKT(SCKT pin) = transmit clock
SCKR(SCKR pin) = receive clock
FST(FST pin) = transmit frame sync
FSR(FSR pin) = receive frame sync
HCKT(HCKT pin) = transmit high frequency clock
HCKR(HCKR pin) = receive high frequency clock

- ⁴ For the internal clock, the external clock cycle is defined by l_{cy}c and the ESAI control register.

- ⁵ The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but it spreads from one serial clock before the first bit clock (like the bit length frame sync signal), until the second-to-last bit clock of the first word in the frame.

- ⁶ Periodically sampled and not 100% tested.

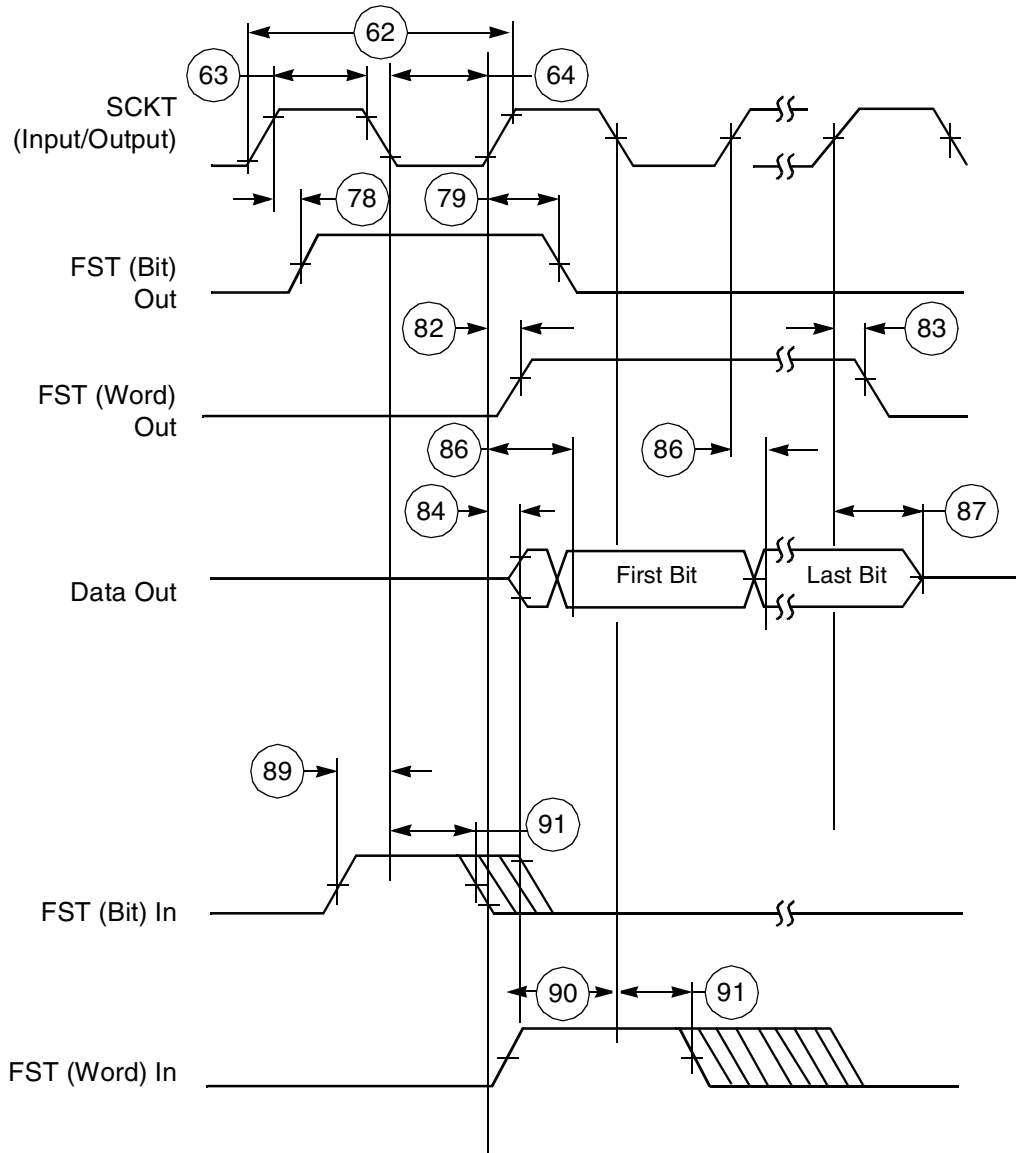


Figure 42. ESAI Transmitter Timing

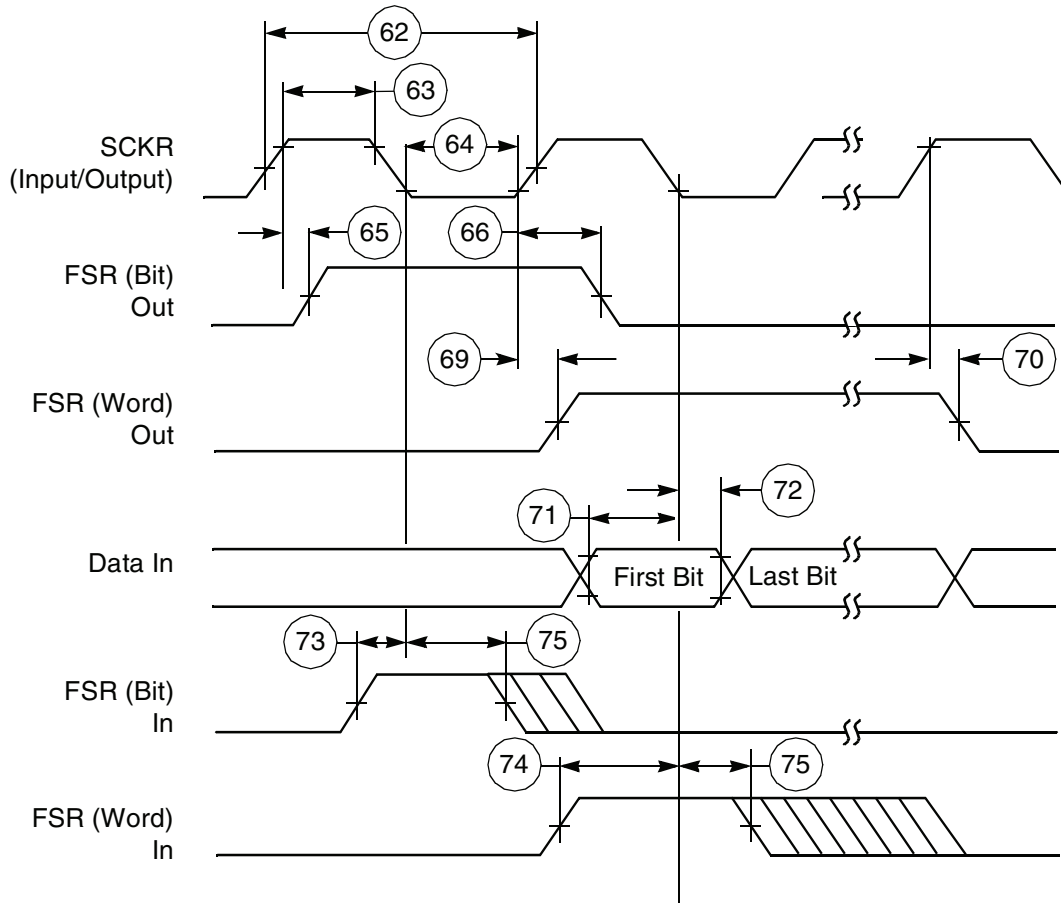


Figure 43. ESAI Receiver Timing

4.11.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4 (Dual Data Rate) timing and SDR104/50(SD3.0) timing.

4.11.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing

Figure 44 depicts the timing of SD/eMMC4.3, and Table 57 lists the SD/eMMC4.3 timing characteristics.

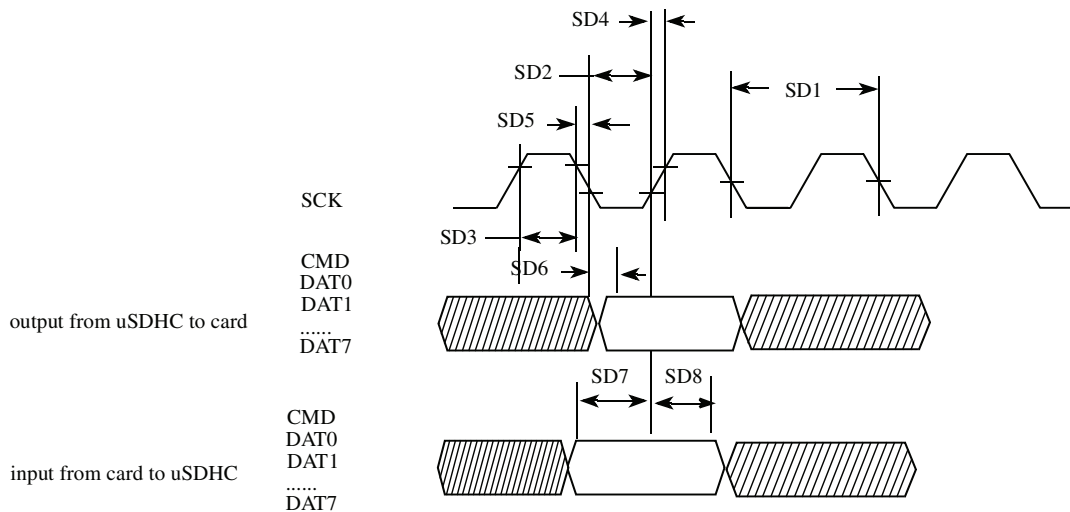


Figure 44. SD/eMMC4.3 Timing

Table 57. SD/eMMC4.3 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}^1	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}^2	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}^3	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns

Table 57. SD/eMMC4.3 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input/Card Outputs CMD, DAT (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time ⁴	t_{IH}	5.6	—	ns

¹ In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

² In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

³ In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

⁴To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.11.4.2 eMMC4.4 (Dual Data Rate) AC Timing

Figure 45 depicts the timing of eMMC4.4. Table 58 lists the eMMC4.4 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

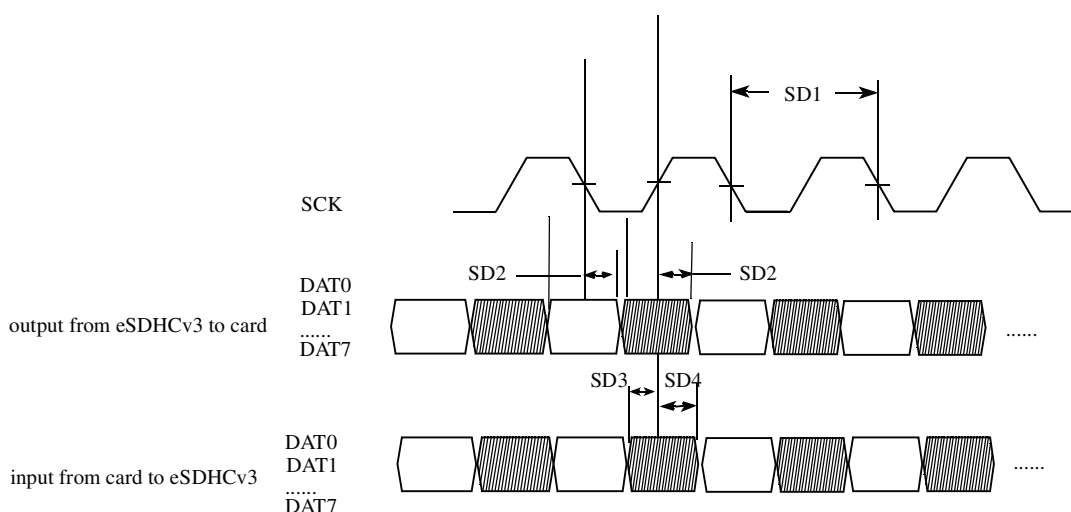


Figure 45. eMMC4.4 Timing

Table 58. eMMC4.4 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (EMMC4.4 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs CMD, DAT (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns

Table 58. eMMC4.4 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

4.11.4.3 SDR50/SDR104 AC Timing

Figure 46 depicts the timing of SDR50/SDR104, and Table 59 lists the SDR50/SDR104 timing characteristics.

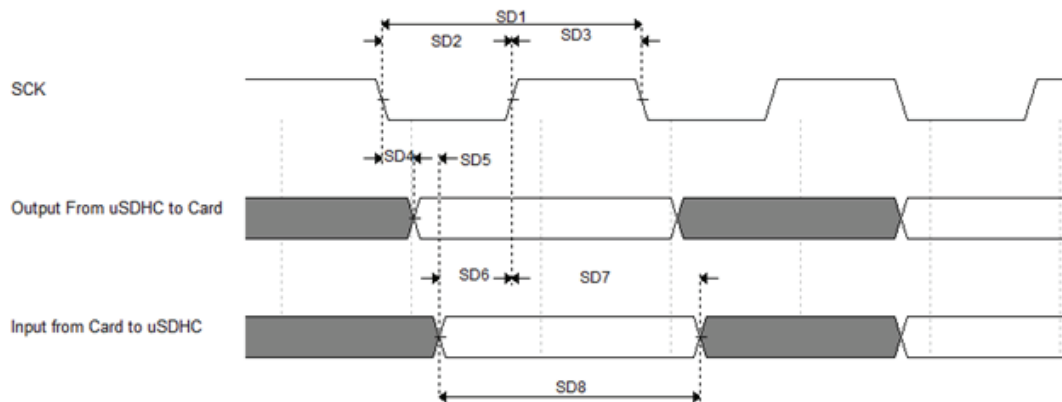


Figure 46. SDR50/SDR104 Timing

Table 59. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.3 \cdot t_{CLK}$	$0.7 \cdot t_{CLK}$	ns
SD2	Clock High Time	t_{CH}	$0.3 \cdot t_{CLK}$	$0.7 \cdot t_{CLK}$	ns
uSDHC Output/Card Inputs CMD, DAT in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs CMD, DAT in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs CMD, DAT in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns

Table 59. SDR50/SDR104 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs CMD, DAT in SDR104 (Reference to CLK)¹					
SD8	Card Output Data Window	t_{ODW}	$0.5 \cdot t_{CLK}$	—	ns

¹Data window in SDR100 mode is variable.

4.11.4.4 Bus Operation Condition for 3.3 V and 1.8 V Signaling

Signaling level of SD/eMMC4.3 and eMMC4.4 modes is 3.3 V. Signaling level of SDR104/SDR50 mode is 1.8 V. The DC parameters for the NVCC_SD1, NVCC_SD2 and NVCC_SD3 supplies are identical to those shown in Table 24, "GPIO DC Parameters," on page 38.

4.11.5 Ethernet Controller (ENET) AC Electrical Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.11.5.1 ENET MII Mode Timing

This subsection describes MII receive, transmit, asynchronous inputs, and serial management signal timings.

4.11.5.1.1 MII Receive Signal Timing (ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER, and ENET_RX_CLK)

The receiver functions correctly up to an ENET_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_RX_CLK frequency.

Electrical Characteristics

Figure 47 shows MII receive signal timings. Table 60 describes the timing parameters (M1–M4) shown in the figure.

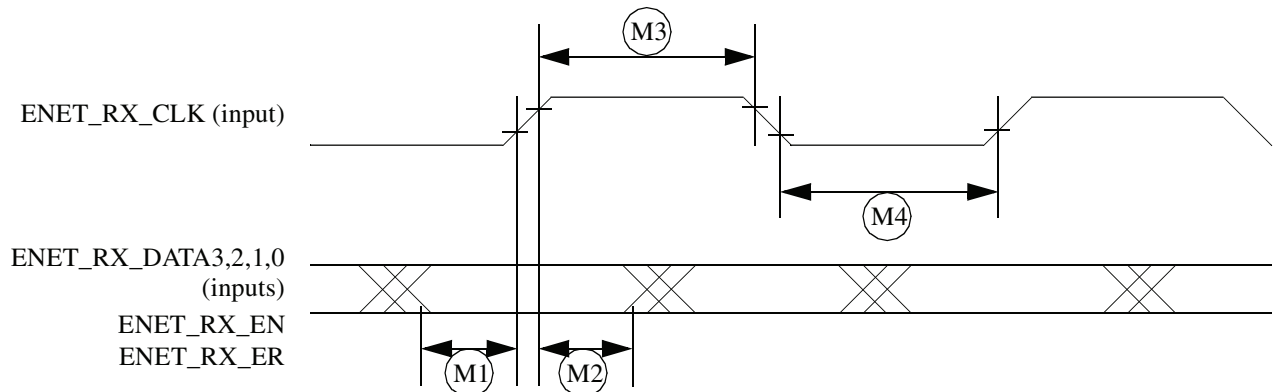


Figure 47. MII Receive Signal Timing Diagram

Table 60. MII Receive Signal Timing

ID	Characteristic ¹	Min.	Max.	Unit
M1	ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER to ENET_RX_CLK setup	5	—	ns
M2	ENET_RX_CLK to ENET_RX_DATA3,2,1,0, ENET_RX_EN, ENET_RX_ER hold	5	—	ns
M3	ENET_RX_CLK pulse width high	35%	65%	ENET_RX_CLK period
M4	ENET_RX_CLK pulse width low	35%	65%	ENET_RX_CLK period

¹ ENET_RX_EN, ENET_RX_CLK, and ENET0_RXD0 have the same timing in 10 Mbps 7-wire interface mode.

4.11.5.1.2 MII Transmit Signal Timing (ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER, and ENET_TX_CLK)

The transmitter functions correctly up to an ENET_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. Additionally, the processor clock frequency must exceed twice the ENET_TX_CLK frequency.

Figure 48 shows MII transmit signal timings. Table 61 describes the timing parameters (M5–M8) shown in the figure.

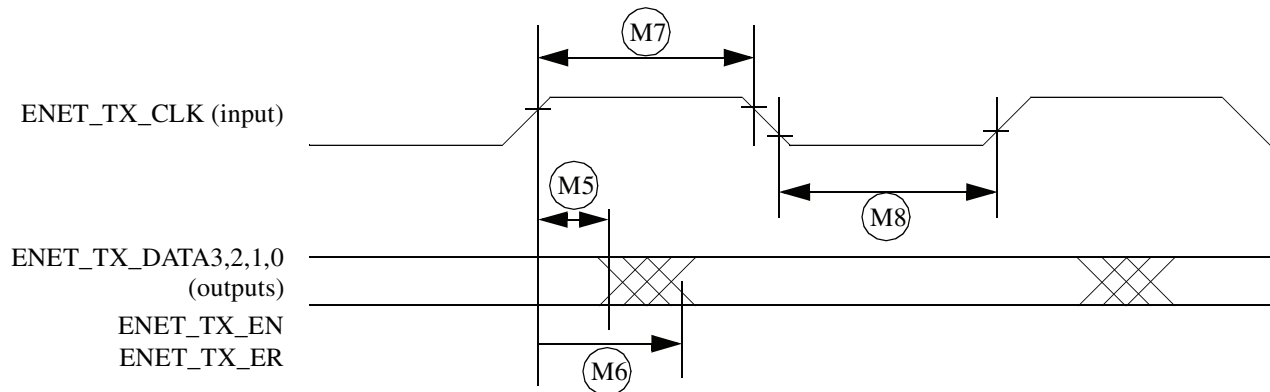


Figure 48. MII Transmit Signal Timing Diagram

Table 61. MII Transmit Signal Timing

ID	Characteristic ¹	Min.	Max.	Unit
M5	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER invalid	5	—	ns
M6	ENET_TX_CLK to ENET_TX_DATA3,2,1,0, ENET_TX_EN, ENET_TX_ER valid	—	20	ns
M7	ENET_TX_CLK pulse width high	35%	65%	ENET_TX_CLK period
M8	ENET_TX_CLK pulse width low	35%	65%	ENET_TX_CLK period

¹ ENET_TX_EN, ENET_TX_CLK, and ENET0_TXD0 have the same timing in 10-Mbps 7-wire interface mode.

4.11.5.1.3 MII Asynchronous Inputs Signal Timing (ENET_CRS and ENET_COL)

Figure 49 shows MII asynchronous input timings. Table 62 describes the timing parameter (M9) shown in the figure.

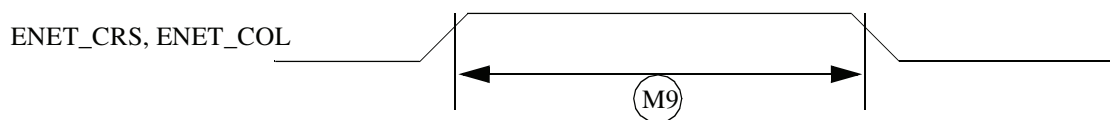


Figure 49. MII Async Inputs Timing Diagram

Table 62. MII Asynchronous Inputs Signal Timing

ID	Characteristic	Min.	Max.	Unit
M9 ¹	ENET_CRS to ENET_COL minimum pulse width	1.5	—	ENET_TX_CLK period

¹ ENET_COL has the same timing in 10-Mbit 7-wire interface mode.

4.11.5.1.4 MII Serial Management Channel Timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification. However the ENET can function correctly with a maximum MDC frequency of 15 MHz.

Figure 50 shows MII asynchronous input timings. Table 63 describes the timing parameters (M10–M15) shown in the figure.

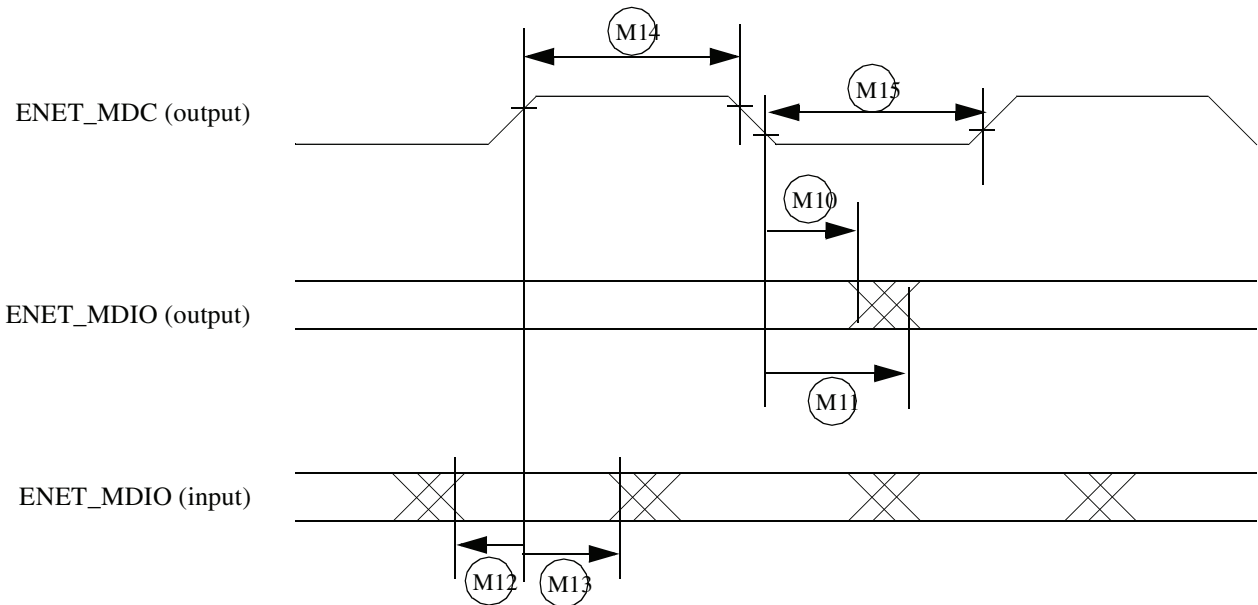


Figure 50. MII Serial Management Channel Timing Diagram

Table 63. MII Serial Management Channel Timing

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	0	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	5	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	18	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

4.11.5.2 RMII Mode Timing

In RMII mode, ENET_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock. ENET_RX_EN is used as the CRS_DV in RMII. Other signals under RMII mode include ENET_TX_EN, ENET0_TXD[1:0], ENET0_RXD[1:0] and ENET_RX_ER.

Figure 51 shows RMI mode timings. Table 64 describes the timing parameters (M16–M21) shown in the figure.

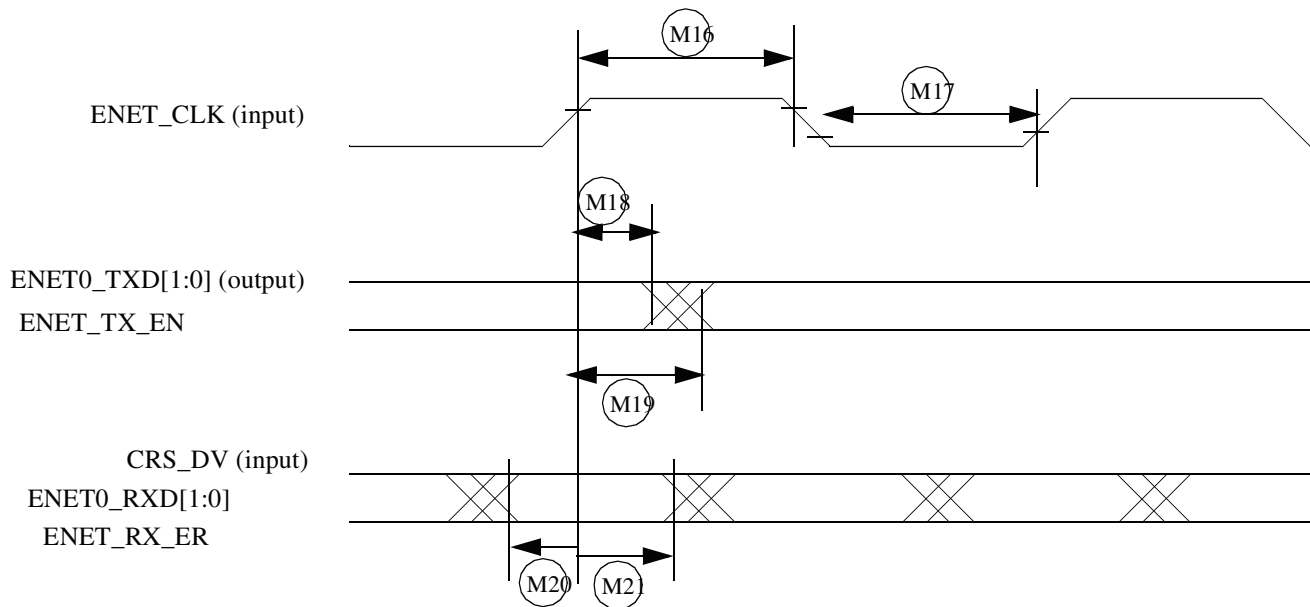


Figure 51. RMI Mode Signal Timing Diagram

Table 64. RMI Signal Timing

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	ENET_CLK period
M17	ENET_CLK pulse width low	35%	65%	ENET_CLK period
M18	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	4	—	ns
M19	ENET_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	15	ns
M20	ENET0_RXD[1:0], CRS_DV(ENET_RX_EN), ENET_RX_ER to ENET_CLK setup	4	—	ns
M21	ENET_CLK to ENET0_RXD[1:0], ENET_RX_EN, ENET_RX_ER hold	2	—	ns

4.11.5.3 RGMII Signal Switching Specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 65. RGMII Signal Switching Specifications¹

Symbol	Description	Min.	Max.	Unit
T_{cyc}^2	Clock cycle duration	7.2	8.8	ns
T_{skewT}^3	Data to clock output skew at transmitter	-100	900	ps

Table 65. RGMII Signal Switching Specifications¹ (continued)

Symbol	Description	Min.	Max.	Unit
T_{skewR}^3	Data to clock input skew at receiver	1	2.6	ps
Duty_G ⁴	Duty cycle for Gigabit	45	55	%
Duty_T ⁴	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

¹ The timings assume the following configuration:

DDR_SEL = (11)b

DSE (drive-strength) = (111)b

² For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns \pm 40 ns and 40 ns \pm 4 ns respectively.

³ For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

⁴ Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{cyc} of the lowest speed transitioned between.

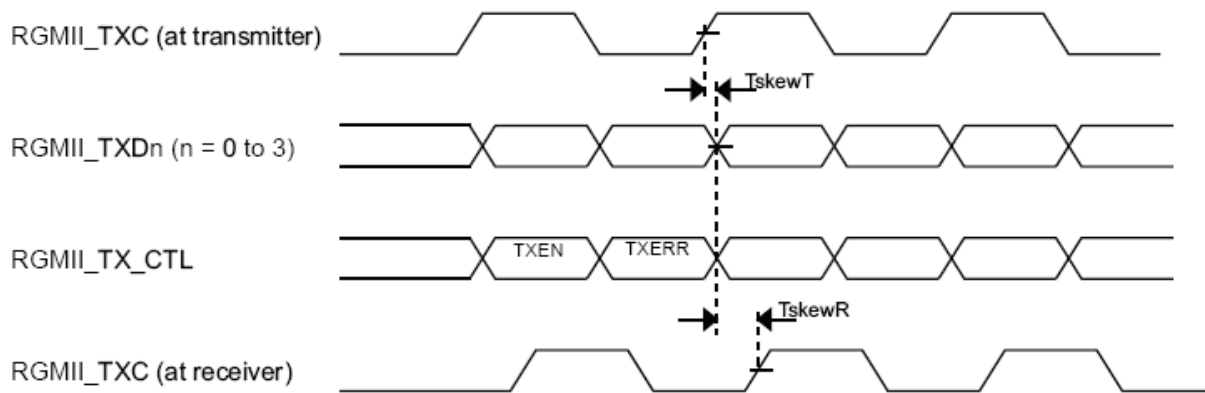


Figure 52. RGMII Transmit Signal Timing Diagram Original

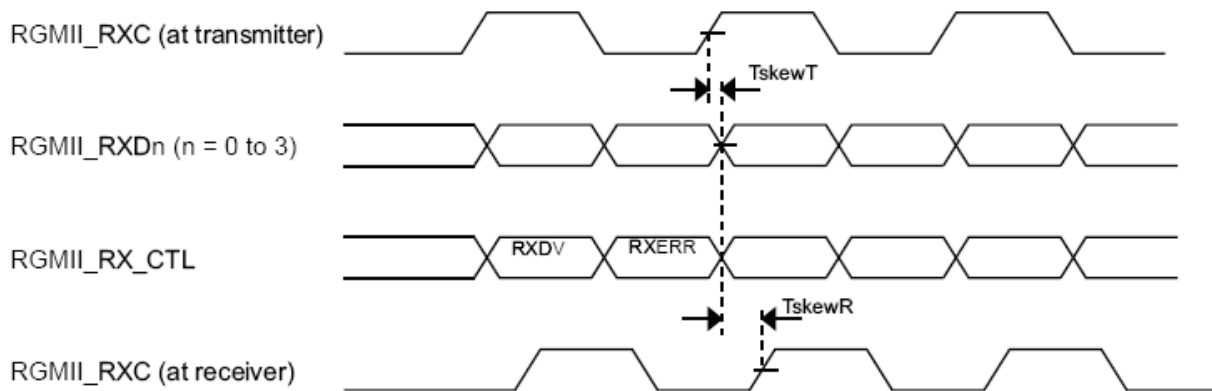


Figure 53. RGMII Receive Signal Timing Diagram Original

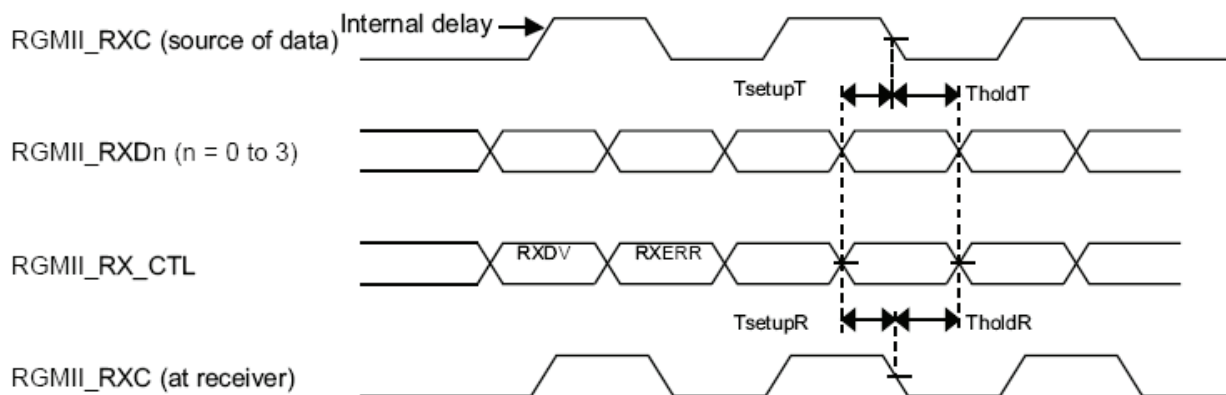


Figure 54. RGMII Receive Signal Timing Diagram with Internal Delay

4.11.6 Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The processor has two CAN modules available for systems design. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* to see which pins expose Tx and Rx pins; these ports are named TXCAN and RXCAN, respectively.

4.11.7 HDMI Module Timing Parameters

4.11.7.1 Latencies and Timing Information

Power-up time (time between TX_PWRON assertion and TX_READY assertion) for the HDMI 3D Tx PHY while operating with the slowest input reference clock supported (13.5 MHz) is 3.35 ms.

Electrical Characteristics

Power-up time for the HDMI 3D Tx PHY while operating with the fastest input reference clock supported (340 MHz) is 133 μ s.

4.11.7.2 Electrical Characteristics

The table below provides electrical characteristics for the HDMI 3D Tx PHY. The following three figures illustrate various definitions and measurement conditions specified in the table below.

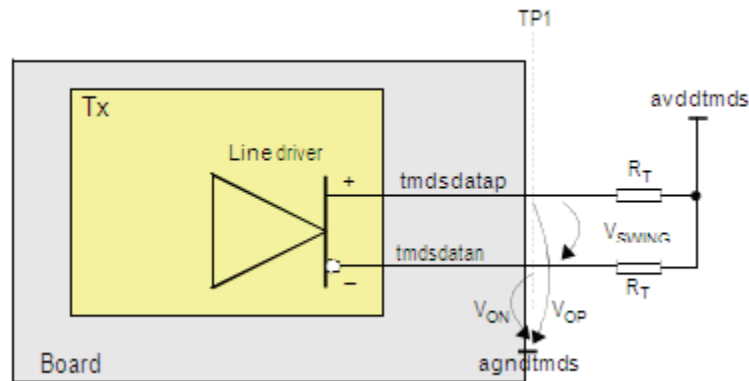


Figure 55. Driver Measuring Conditions

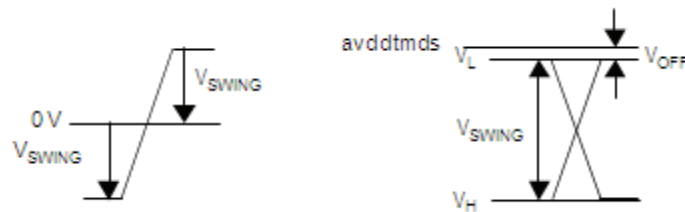


Figure 56. Driver Definitions

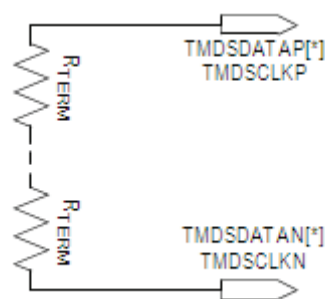


Figure 57. Source Termination

Table 66. Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating conditions for HDMI						
avddtmds	Termination supply voltage	-	3.15	3.3	3.45	V
R_T	Termination resistance	-	45	50	55	Ω
TMDS drivers DC specifications						
V_{OFF}	Single-ended standby voltage	$R_T = 50 \Omega$	$avddtmds \pm 10 \text{ mV}$			mV
V_{SWING}	Single-ended output swing voltage	For measurement conditions and definitions, see the first two figures above. Compliance point TP1 as defined in the HDMI specification, version 1.3a, section 4.2.4.	400	-	600	mV
V_H	Single-ended output high voltage For definition, see the second figure above	If attached sink supports TMDSCCLK < or = 165 MHz	$avddtmds \pm 10 \text{ mV}$			mV
		If attached sink supports TMDSCCLK > 165 MHz	$avddtmds - 200 \text{ mV}$	-	$avddtmds + 10 \text{ mV}$	mV
V_L	Single-ended output low voltage For definition, see the second figure above	If attached sink supports TMDSCCLK < or = 165 MHz	$avddtmds - 600 \text{ mV}$	-	$avddtmds - 400 \text{ mV}$	mV
		If attached sink supports TMDSCCLK > 165 MHz	$avddtmds - 700 \text{ mV}$	-	$avddtmds - 400 \text{ mV}$	mV
R_{TERM}	Differential source termination load (inside HDMI 3D Tx PHY) Although the HDMI 3D Tx PHY includes differential source termination, the user-defined value is set for each single line (for illustration, see the third figure above). Note: R_{TERM} can also be configured to be open and not present on TMDS channels.	-	50	-	200	Ω
Hot plug detect specifications						
HPD^{VH}	Hot plug detect high range	-	2.0	-	5.3	V
$V_{HPD_{VL}}$	Hot plug detect low range	-	0	-	0.8	V
HPD_Z	Hot plug detect input impedance	-	10	-	-	k Ω
HPD_t	Hot plug detect time delay	-	-	-	100	μs

4.11.8 Switching Characteristics

Table 67 describes switching characteristics for the HDMI 3D Tx PHY. Figure 58 to Figure 62 illustrate various parameters specified in table.

NOTE

All dynamic parameters related to the TMDS line drivers' performance imply the use of assembly guidelines.

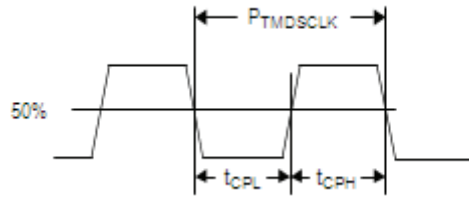


Figure 58. TMDS Clock Signal Definitions

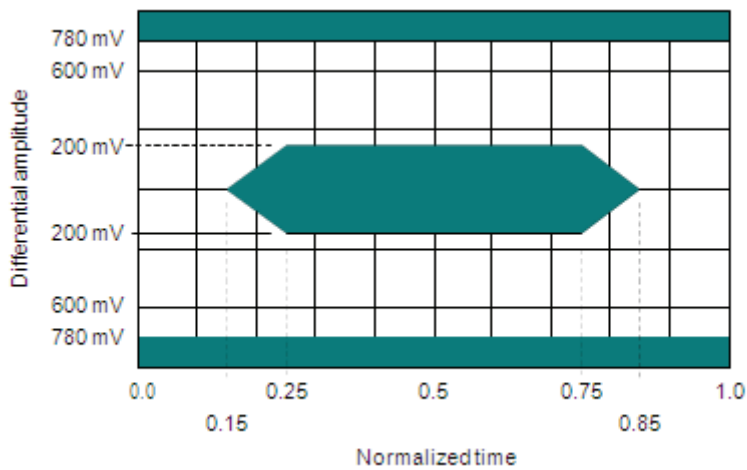


Figure 59. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

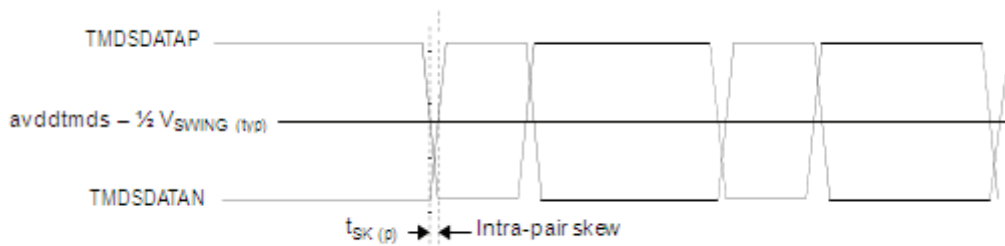


Figure 60. Intra-Pair Skew Definition

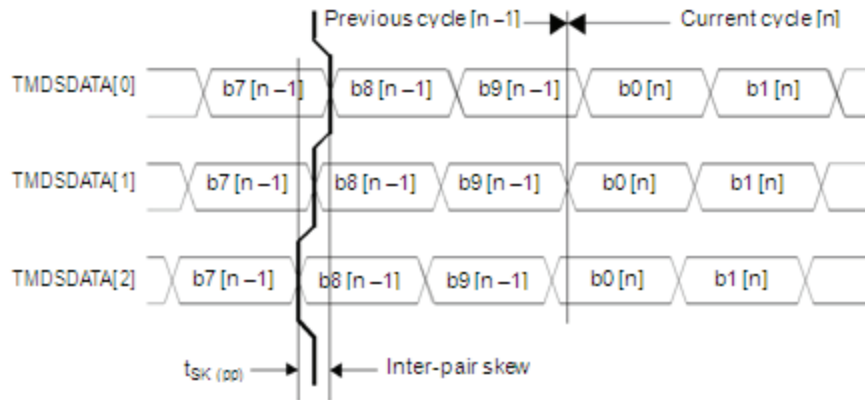


Figure 61. Inter-Pair Skew Definition

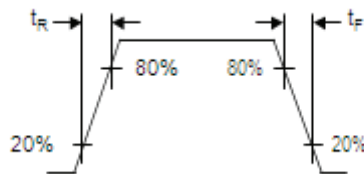


Figure 62. TMDS Output Signals Rise and Fall Time Definition

Table 67. Switching Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
TMDS Drivers Specifications						
—	Maximum serial data rate	—	—	—	3.4	Gbps
$F_{TMDSCLK}^F$	TMDSCLK frequency	On TMDSCLKP/N outputs	25	—	340	MHz
$P_{TMDSCLK}^P$	TMDSCLK period	RL = 50 Ω See Figure 58.	2.94	—	40	ns
t_{CDC}^t	TMDSCLK duty cycle	$t_{CDC} = t_{CPH} / P_{TMDSCLK}$ RL = 50 Ω See Figure 58.	40	50	60	%
t_{CPH}^t	TMDSCLK high time	RL = 50 Ω See Figure 58.	4	5	6	UI ¹
t_{CPL}^t	TMDSCLK low time	RL = 50 Ω See Figure 58.	4	5	6	UI ¹
—	TMDSCLK jitter ²	RL = 50 Ω	—	—	0.25	UI ¹
$t_{SK(p)}^t$	Intra-pair (pulse) skew	RL = 50 Ω See Figure 60.	—	—	0.15	UI ¹

Table 67. Switching Characteristics (continued)

$t_{SK(pp)}$	Inter-pair skew	$R_L = 50 \Omega$ See Figure 61.	—	—	1	UI ¹
t_R	Differential output signal rise time	20–80% $R_L = 50 \Omega$ See Figure 62.	75	—	0.4 UI	ps
t_F	Differential output signal fall time	20–80% $R_L = 50 \Omega$ See Figure 62.	75	—	0.4 UI	ps
—	Differential signal overshoot	Referred to $2x V_{SWING}$	—	—	15	%
—	Differential signal undershoot	Referred to $2x V_{SWING}$	—	—	25	%

¹ UI means TMD5 clock unit.

² Relative to ideal recovery clock, as specified in the HDMI specification, version 1.4a, section 4.2.3.

4.11.9 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 63 depicts the timing of I²C module, and Table 68 lists the I²C module timing characteristics.

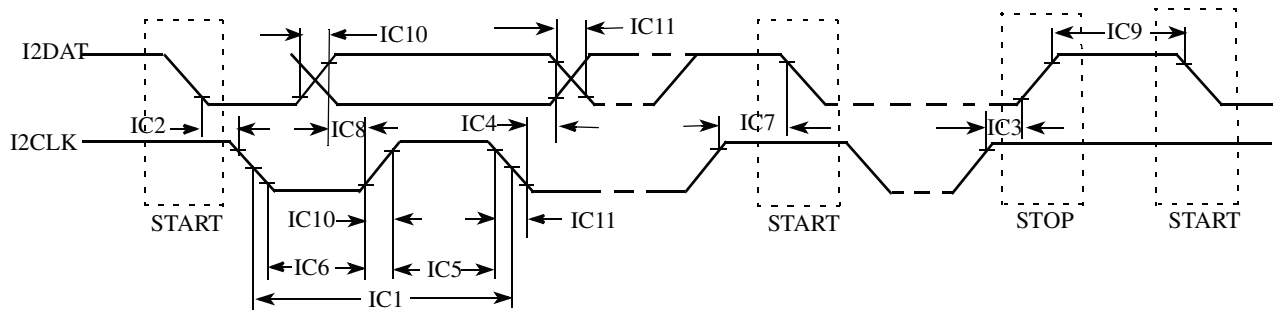


Figure 63. I²C Bus Timing

Table 68. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	μs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	μs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	μs
IC4	Data hold time	0 ¹	3.45 ²	0 ¹	0.9 ²	μs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	μs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	μs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	μs

Table 68. I²C Module Timing Parameters (continued)

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC8	Data set-up time	250	—	100 ³	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	μs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b^4$	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b^4$	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

¹ A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

² The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal.

³ A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line $\text{max_rise_time (IC9)} + \text{data_setup_time (IC7)} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the I2CLK line is released.

⁴ C_b = total capacitance of one bus line in pF.

4.11.10 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and other related functions.
- Synchronization and control capabilities, such as avoidance of tearing artifacts.

4.11.10.1 IPU Sensor Interface Signal Mapping

The IPU supports a number of sensor input formats. Table 69 defines the mapping of the Sensor Interface Pins used for various supported interface formats.

Table 69. Camera Input Signal Cross Reference, Format, and Bits Per Cycle

Signal Name ¹	RGB565 8 bits 2 cycles	RGB565 ² 8 bits 3 cycles	RGB666 ³ 8 bits 3 cycles	RGB888 8 bits 3 cycles	YCbCr ⁴ 8 bits 2 cycles	RGB565 ⁵ 16 bits 2 cycles	YCbCr ⁶ 16 bits 1 cycle	YCbCr ⁷ 16 bits 1 cycle	YCbCr ⁸ 20 bits 1 cycle
CSIx_DAT0	—	—	—	—	—	—	—	0	C[0]
CSIx_DAT1	—	—	—	—	—	—	—	0	C[1]
CSIx_DAT2	—	—	—	—	—	—	—	C[0]	C[2]
CSIx_DAT3	—	—	—	—	—	—	—	C[1]	C[3]
CSIx_DAT4	—	—	—	—	—	B[0]	C[0]	C[2]	C[4]
CSIx_DAT5	—	—	—	—	—	B[1]	C[1]	C[3]	C[5]
CSIx_DAT6	—	—	—	—	—	B[2]	C[2]	C[4]	C[6]
CSIx_DAT7	—	—	—	—	—	B[3]	C[3]	C[5]	C[7]
CSIx_DAT8	—	—	—	—	—	B[4]	C[4]	C[6]	C[8]
CSIx_DAT9	—	—	—	—	—	G[0]	C[5]	C[7]	C[9]
CSIx_DAT10	—	—	—	—	—	G[1]	C[6]	0	Y[0]
CSIx_DAT11	—	—	—	—	—	G[2]	C[7]	0	Y[1]
CSIx_DAT12	B[0], G[3]	R[2],G[4],B[2]	R/G/B[4]	R/G/B[0]	Y/C[0]	G[3]	Y[0]	Y[0]	Y[2]
CSIx_DAT13	B[1], G[4]	R[3],G[5],B[3]	R/G/B[5]	R/G/B[1]	Y/C[1]	G[4]	Y[1]	Y[1]	Y[3]
CSIx_DAT14	B[2], G[5]	R[4],G[0],B[4]	R/G/B[0]	R/G/B[2]	Y/C[2]	G[5]	Y[2]	Y[2]	Y[4]
CSIx_DAT15	B[3], R[0]	R[0],G[1],B[0]	R/G/B[1]	R/G/B[3]	Y/C[3]	R[0]	Y[3]	Y[3]	Y[5]
CSIx_DAT16	B[4], R[1]	R[1],G[2],B[1]	R/G/B[2]	R/G/B[4]	Y/C[4]	R[1]	Y[4]	Y[4]	Y[6]
CSIx_DAT17	G[0], R[2]	R[2],G[3],B[2]	R/G/B[3]	R/G/B[5]	Y/C[5]	R[2]	Y[5]	Y[5]	Y[7]
CSIx_DAT18	G[1], R[3]	R[3],G[4],B[3]	R/G/B[4]	R/G/B[6]	Y/C[6]	R[3]	Y[6]	Y[6]	Y[8]
CSIx_DAT19	G[2], R[4]	R[4],G[5],B[4]	R/G/B[5]	R/G/B[7]	Y/C[7]	R[4]	Y[7]	Y[7]	Y[9]

¹ CSIx stands for CSI1 or CSI2

² The MSB bits are duplicated on LSB bits implementing color extension

³ The two MSB bits are duplicated on LSB bits implementing color extension

⁴ YCbCr, 8 bits—Supported within the BT.656 protocol (sync embedded within the data stream).

⁵ RGB 16 bits— Supported in two ways: (1) As a “generic data” input, with no on-the-fly processing; (2) With on-the-fly processing, but only under some restrictions on the control protocol.

⁶ YCbCr 16 bits— Supported as a “generic-data” input, with no on-the-fly processing.

⁷ YCbCr 16 bits— Supported as a sub-case of the YCbCr, 20 bits, under the same conditions (BT.1120 protocol).

⁸ YCbCr, 20 bits, supported only within the BT.1120 protocol (syncs embedded within the data stream).

4.11.10.2 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.11.10.2.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.11.10.2.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See [Figure 64](#).

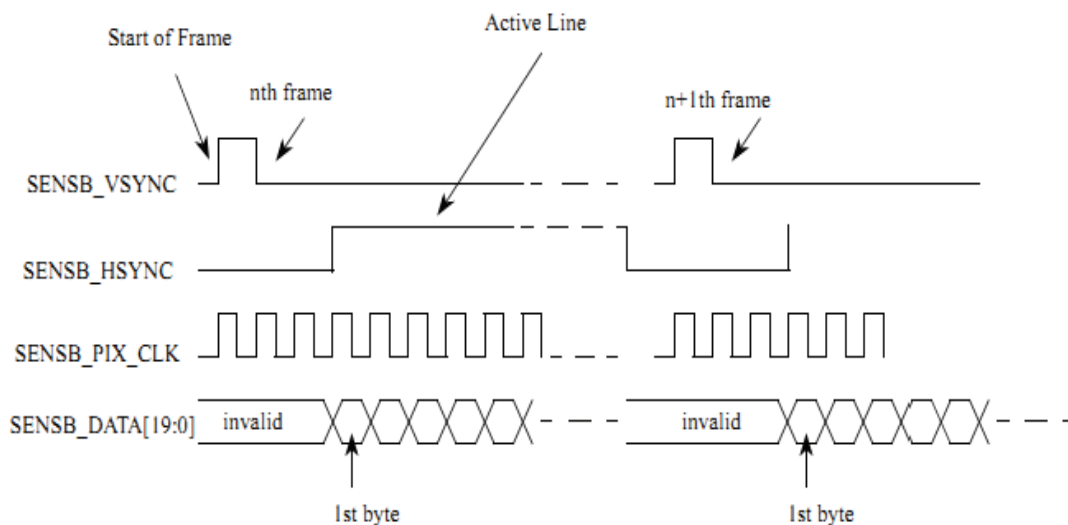


Figure 64. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.11.10.2.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.11.10.2.2, “Gated Clock Mode,”) except for the SENS_B_HSYNC signal, which is not used (see Figure 65). All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENS_B_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

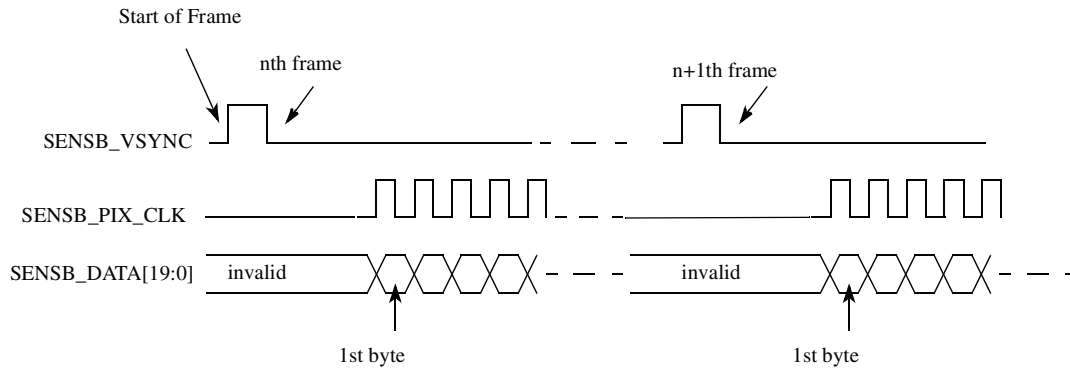


Figure 65. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 65 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENS_B_VSYNC; active-high/low SENS_B_HSYNC; and rising/falling-edge triggered SENS_B_PIX_CLK.

4.11.10.3 Electrical Characteristics

Figure 66 depicts the sensor interface timing. SENSB_MCLK signal described here is not generated by the IPU. Table 70 lists the sensor interface timing characteristics.

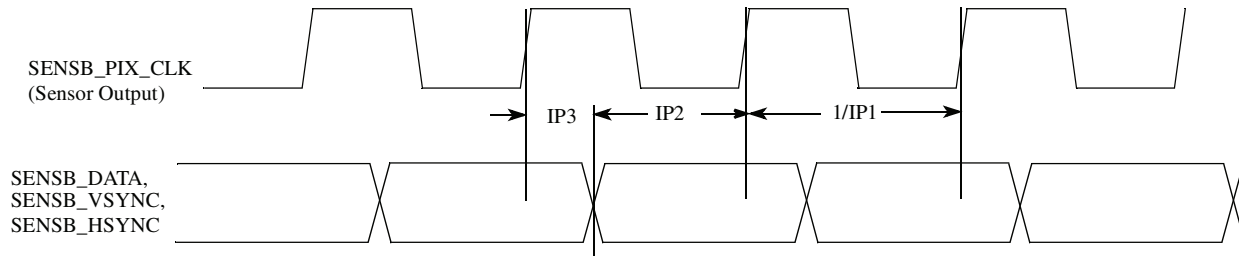


Figure 66. Sensor Interface Timing Diagram

Table 70. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	180	MHz
IP2	Data and control setup time	Tsu	2	—	ns
IP3	Data and control holdup time	Thd	1	—	ns

4.11.10.4 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 71 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 71. Video Signal Cross-Reference

i.MX 6Solo/6DualLite	LCD							Comment ¹
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit Y/Cb ²	16-bit Y/Cb	20-bit Y/Cb	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	<p>The restrictions are as follows:</p> <ul style="list-style-type: none"> • There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. • The bit order is expressed in each of the bit groups, for example, B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	

Table 71. Video Signal Cross-Reference (continued)

i.MX 6Solo/6DualLite	LCD							Comment ¹
Port Name (x=0, 1)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						
		16-bit RGB	18-bit RGB	24 Bit RGB	8-bit YCrCb ²	16-bit YCrCb	20-bit YCrCb	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—
Dlx_DISP_CLK	PixCLK							—
Dlx_PIN1	—							May be required for anti-tearing
Dlx_PIN2	HSYNC							—
Dlx_PIN3	VSYNC							VSYNC out
Dlx_PIN4	—							Additional frame/row synchronous signals with programmable timing
Dlx_PIN5	—							
Dlx_PIN6	—							
Dlx_PIN7	—							
Dlx_PIN8	—							
Dlx_D0_CS	—							—
Dlx_D1_CS	—							Alternate mode of PWM output for contrast or brightness control
Dlx_PIN11	—							—
Dlx_PIN12	—							—
Dlx_PIN13	—							Register select signal
Dlx_PIN14	—							Optional RS2
Dlx_PIN15	DRDY/DV							Data validation/blank, data enable
Dlx_PIN16	—							Additional data synchronous signals with programmable features/timing
Dlx_PIN17	Q							

¹ Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

² This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

NOTE

Table 71 provides information for both the Disp0 and Disp1 ports. However, Disp1 port has reduced pinout depending on IOMUXC configuration and therefore may not support all the above configurations. See the IOMUXC table for details.

4.11.10.5 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordingly.

4.11.10.5.1 Synchronous Controls

The synchronous control changes its value as a function of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The `ipp_disp_clk` is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The `ipp_pin_1–ipp_pin_7` are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (such as, HSYNC/VSYCN) calculation. The internal event (local start point) is synchronized with internal `DI_CLK`. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half `DI_CLK` resolution. A full description of the counters system can be found in the IPU chapter of the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

4.11.10.5.2 Asynchronous Controls

The asynchronous control is a data-oriented signal that changes its value with an output data according to additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The `ipp_d0_cs` and `ipp_d1_cs` pins are dedicated to provide chip select signals to two displays.
- The `ipp_pin_11–ipp_pin_17` are general purpose asynchronous pins, that can be used to provide WR, RD, RS or any other data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half `DI_CLK` resolution.

4.11.10.6 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.11.10.6.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization
- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on the base of an internally generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point. The data bus of the synchronous interface is output direction only.

4.11.10.6.2 LCD Interface Functional Description

Figure 67 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure, signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock is used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC.)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC.)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off. (DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

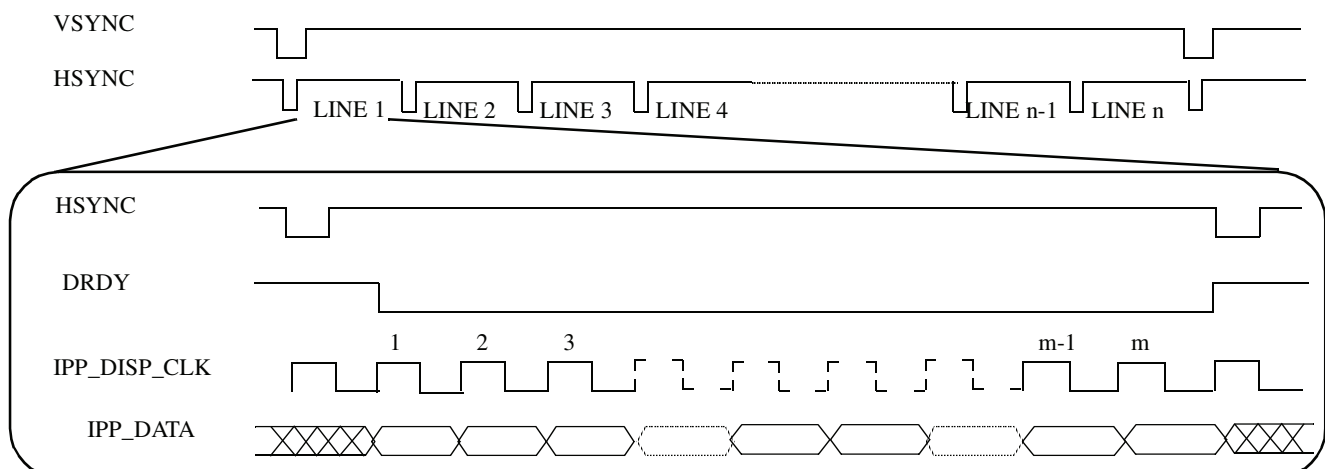


Figure 67. Interface Timing Diagram for TFT (Active Matrix) Panels

4.11.10.6.3 TFT Panel Sync Pulse Timing Diagrams

Figure 68 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All the parameters shown in the figure are programmable. All controls are started by corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

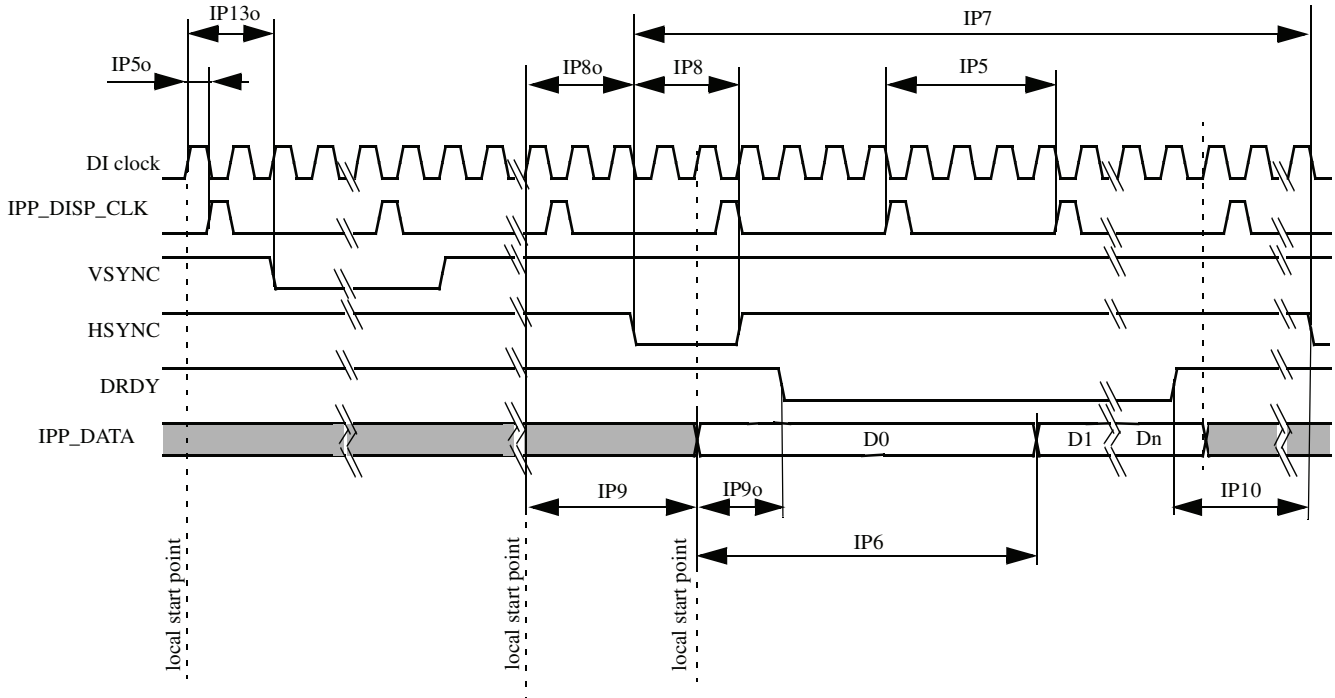


Figure 68. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 69 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

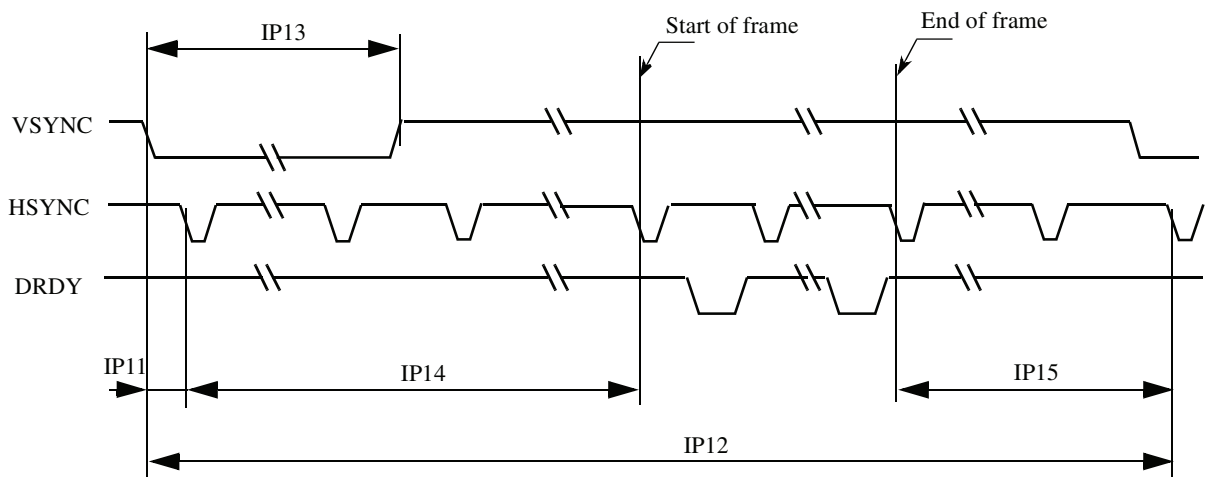


Figure 69. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 72 shows timing characteristics of signals presented in Figure 68 and Figure 69.

Table 72. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	(¹)	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to n components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter ² .	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—width of a horizontal blanking before a first active data in a line (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line (in interface clocks) FW—width of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking. The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line. The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	Width of second Vertical blanking interval in line. The FH should be built by suitable DI's counter.	ns

Table 72. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET—offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution). Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution). The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET—offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution). The DRDY_OFFSET should be built by suitable DI's counter.	ns

¹ Display interface clock period immediate value.

$$T_{dicp} = \begin{cases} T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk} \left(\text{floor} \left[\frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \right] + 0.5 \pm 0.5 \right), & \text{for fractional } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK.

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}_{dicp} = T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

² DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is:

$$\text{Accuracy} = (0.5 \times T_{diclk}) \pm 0.62\text{ns}$$

The maximal accuracy of UP/DOWN edge of IPP_DATA is:

$$\text{Accuracy} = T_{\text{diclk}} \pm 0.62\text{ns}$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed through the registers.

Figure 70 depicts the synchronous display interface timing for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set through the Register. Table 73 lists the synchronous display interface timing characteristics.

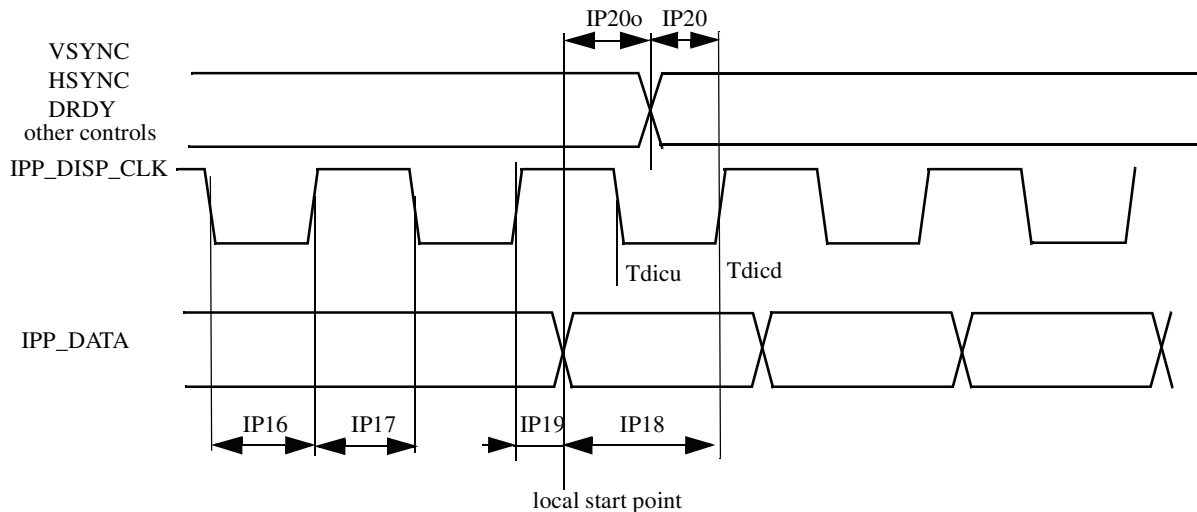


Figure 70. Synchronous Display Interface Timing Diagram—Access Level

Table 73. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ ¹	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu-1.24	Tdicd ² -Tdicu ³	Tdicd-Tdicu+1.24	ns
IP17	Display interface clock high time	Tckh	Tdicp-Tdicd+Tdicu-1.24	Tdicp-Tdicd+Tdicu	Tdicp-Tdicd+Tdicu+1.2	ns
IP18	Data setup time	Tdsu	Tdicd-1.24	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp-Tdicd-1.24	Tdicp-Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu-1.24	Tocsu	Tocsu+1.24	ns
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd-1.24-Tocsu%Tdicp	Tdicu	—	ns

¹The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

² Display interface clock down time

$$T_{\text{dicd}} = \frac{1}{2} \left(T_{\text{diclk}} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_DOWN}}{\text{DI_CLK_PERIOD}} \right] \right)$$

Electrical Characteristics

³ Display interface clock up time where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

$$T_{dicu} = \frac{1}{2} \left(T_{diclk} \times \text{ceil} \left[\frac{2 \times \text{DISP_CLK_UP}}{\text{DI_CLK_PERIOD}} \right] \right)$$

4.11.11 LVDS Display Bridge (LDB) Module Parameters

The LVDS interface complies with TIA/EIA 644-A standard. For more details, see TIA/EIA STANDARD 644-A, “Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits”.

Table 74. LVDS Display Bridge (LDB) Electrical Specification

Parameter	Symbol	Test Condition	Min	Max	Units
Differential Voltage Output Voltage	V _{OD}	100 Ω Differential load	250	450	mV
Output Voltage High	V _{oh}	100 Ω differential load (0 V Diff—Output High Voltage static)	1.25	1.6	mV
Output Voltage Low	V _{ol}	100 Ω differential load (0 V Diff—Output Low Voltage static)	0.9	1.25	mV
Offset Static Voltage	V _{OS}	Two 49.9 Ω resistors in series between N-P terminal, with output in either Zero or One state, the voltage measured between the 2 resistors.	1.15	1.375	V
VOS Differential	V _{OSDIFF}	Difference in V _{OS} between a One and a Zero state	-50	50	mV
Output short circuited to GND	ISA ISB	With the output common shorted to GND	-24	24	mA
VT Full Load Test	VTLoad	100 Ω Differential load with a 3.74 kΩ load between GND and IO Supply Voltage	247	454	mV

4.11.12 MIPI D-PHY Timing Parameters

This section describes MIPI D-PHY electrical specifications, compliant with MIPI CSI-2 version 1.0, D-PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes) and MIPI DSI Version 1.01, and D-PHY specification Rev. 1.0 (and also DPI version 2.0, DBI version 2.0, DSC version 1.0a at protocol layer) (for MIPI display port x2 lanes).

4.11.12.1 Electrical and Timing Information

Table 75. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
Input DC Specifications - Apply to CLKP/N and DATAP/N inputs						
V _I	Input signal voltage range	Transient voltage range is limited from -300 mV to 1600 mV	-50	—	1350	mV

Table 75. Electrical and Timing Information (continued)

V_{LEAK}	Input leakage current	$V_{GNDSH(min)} = V_I = V_{GNDSH(max)} + V_{OH(absmax)}$ Lane module in LP Receive Mode	-10	—	10	mA
V_{GNDSH}	Ground Shift		-50	—	50	mV
$V_{OH(absmax)}$	Maximum transient output voltage level		—	—	1.45	V
$t_{voh(absmax)}$	Maximum transient time above $V_{OH(absmax)}$		—	—	20	ns
HS Line Drivers DC Specifications						
$ V_{OD} $	HS Transmit Differential output voltage magnitude	$80 \Omega \leq RL < = 125 \Omega$	140	200	270	mV
$\Delta V_{OD} $	Change in Differential output voltage magnitude between logic states	$80 \Omega \leq RL < = 125 \Omega$			10	mV
V_{CMTX}	Steady-state common-mode output voltage.	$80 \Omega \leq RL < = 125 \Omega$	150	200	250	mV
$\Delta V_{CMTX(1,0)}$	Changes in steady-state common-mode output voltage between logic states	$80 \Omega \leq RL < = 125 \Omega$			5	mV
V_{OHHS}	HS output high voltage	$80 \Omega \leq RL < = 125 \Omega$			360	mV
Z_{OS}	Single-ended output impedance.		40	50	62.5	Ω
ΔZ_{OS}	Single-ended output impedance mismatch.				10	%
LP Line Drivers DC Specifications						
V_{OL}	Output low-level SE voltage		-50		50	mV
V_{OH}	Output high-level SE voltage		1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance.		110			Ω
$\Delta Z_{OLP(01-10)}$	Single-ended output impedance mismatch driving opposite level				20	%
$\Delta Z_{OLP(0-11)}$	Single-ended output impedance mismatch driving same level				5	%
HS Line Receiver DC Specifications						
V_{IDTH}	Differential input high voltage threshold				70	mV

Table 75. Electrical and Timing Information (continued)

V_{IDTL}	Differential input low voltage threshold		-70			mV
V_{IHHS}	Single ended input high voltage				460	mV
V_{ILHS}	Single ended input low voltage		-40			mV
V_{CMRXDC}	Input common mode voltage		70		330	mV
Z_{ID}	Differential input impedance		80		125	Ω
LP Line Receiver DC Specifications						
V_{IL}	Input low voltage				550	mV
V_{IH}	Input high voltage		920			mV
V_{HYST}	Input hysteresis		25			mV
Contention Line Receiver DC Specifications						
V_{ILF}	Input low fault threshold		200		450	mV

4.11.12.2 MIPI D-PHY Signaling Levels

The signal levels are different for differential HS mode and single-ended LP mode. Figure 71 shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

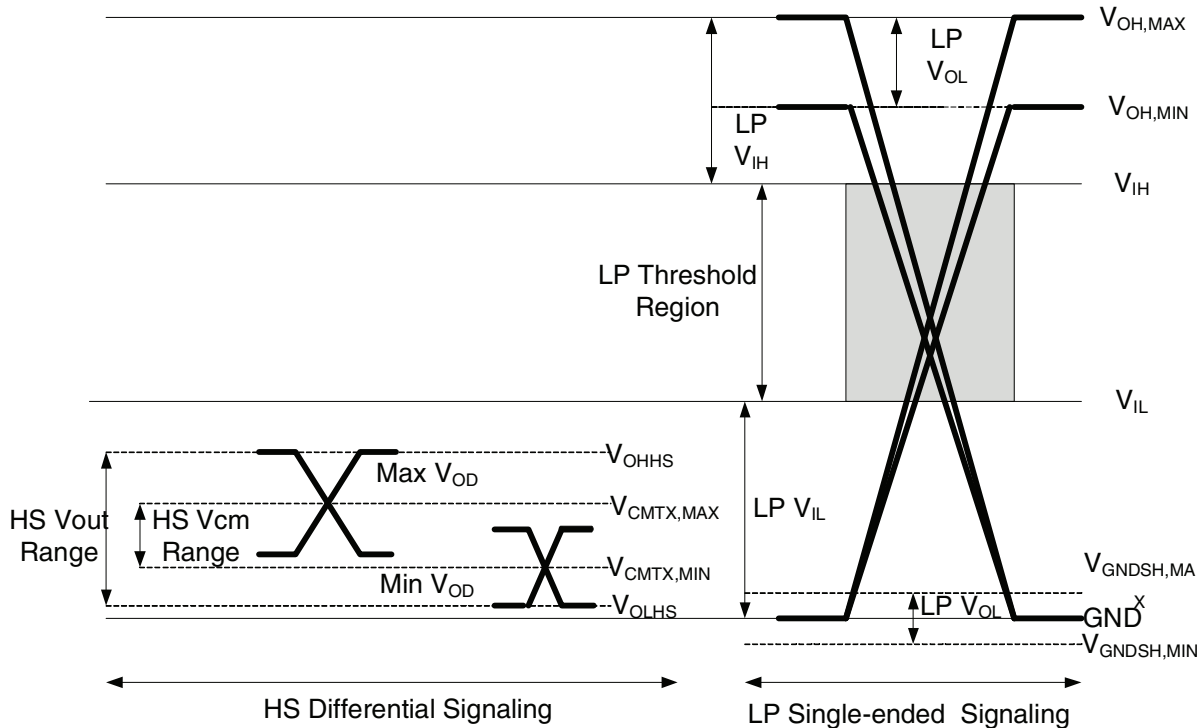


Figure 71. D-PHY Signaling Levels

4.11.12.3 MIPI HS Line Driver Characteristics

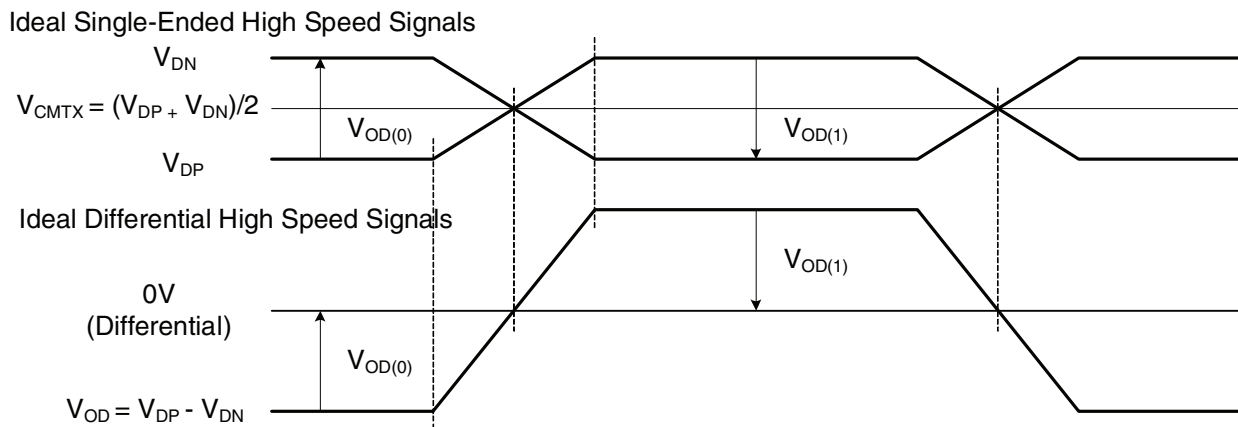


Figure 72. Ideal Single-ended and Resulting Differential HS Signals

4.11.12.4 Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

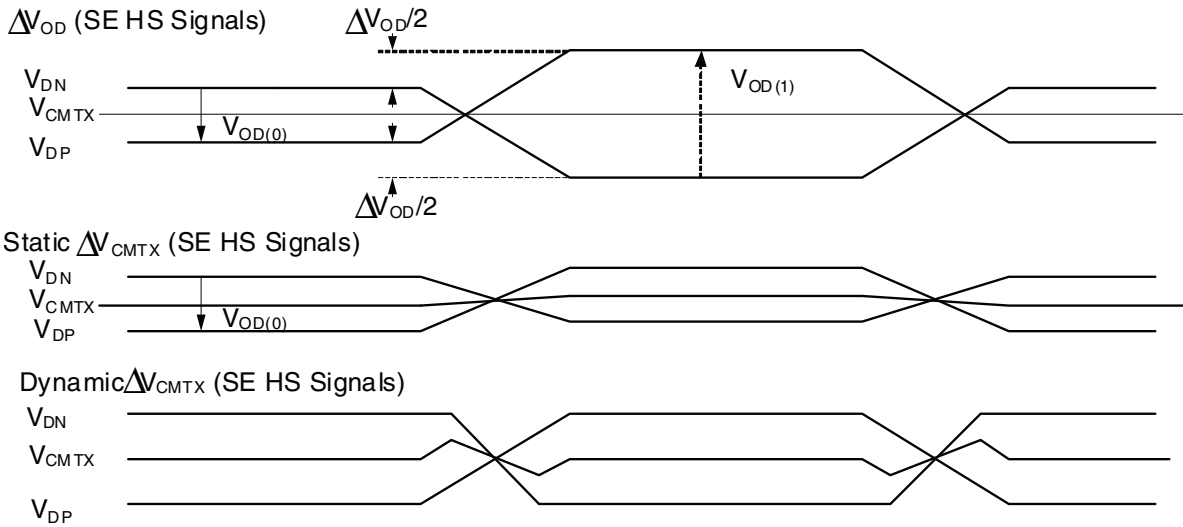


Figure 73. Possible ΔV_{CMTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

4.11.12.5 MIPI D-PHY Switching Characteristics

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
HS Line Drivers AC Specifications						
—	Maximum serial data rate (forward direction)	On DATAP/N outputs. 80 Ω ≤ RL ≤ 125 Ω	80	—	1000	Mbps
F _{DDRCLK}	DDR CLK frequency	On DATAP/N outputs.	40	—	500	MHz
P _{DDRCLK}	DDR CLK period	80 Ω ≤ RL ≤ 125 Ω	2	—	25	ns
t _{CDC}	DDR CLK duty cycle	t _{CDC} = t _{CPH} / P _{DDRCLK}	—	50	—	%
t _{CPH}	DDR CLK high time		—	1	—	UI
t _{CPL}	DDR CLK low time		—	1	—	UI
—	DDR CLK / DATA Jitter		—	75	—	ps pk-pk
t _{SKEW[PN]}	Intra-Pair (Pulse) skew			0.075		UI
t _{SKEW[TX]}	Data to Clock Skew		0.350		0.650	UI
t _{SETUP[RX]}	Data to Clock Receiver Setup time		0.15			UI
t _{HOLD[RX]}	Clock to Data Receiver Hold time		0.15			UI
t _r	Differential output signal rise time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
t _f	Differential output signal fall time	20% to 80%, RL = 50 Ω	150		0.3UI	ps
ΔV _{CMTX(HF)}	Common level variation above 450 MHz	80 Ω ≤ RL ≤ 125 Ω			15	mV _{rms}

Table 76. Electrical and Timing Information

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	Unit
$\Delta V_{CMTX(LF)}$	Common level variation between 50 MHz and 450 MHz.	$80 \Omega \leq R_L < 125 \Omega$			25	mV _p
LP Line Drivers AC Specifications						
t_{rip}, t_{flp}	Single ended output rise/fall time	15% to 85%, $C_L < 70$ pF			25	ns
t_{reo}		30% to 85%, $C_L < 70$ pF			35	ns
$\delta V / \delta t_{SR}$	Signal slew rate	15% to 85%, $C_L < 70$ pF			120	mV/ns
C_L	Load capacitance		0		70	pF
HS Line Receiver AC Specifications						
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz				200	mVpp
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 MHz and 450 MHz.		-50		50	mVpp
C_{CM}	Common mode termination				60	pF
LP Line Receiver AC Specifications						
e_{SPIKE}	Input pulse rejection				300	Vps
T_{MIN}	Minimum pulse response		50			ns
V_{INT}	Pk-to-Pk interference voltage				400	mV
f_{INT}	Interference frequency		450			MHz
Model Parameters used for Driver Load switching performance evaluation						
C_{PAD}	Equivalent Single ended I/O PAD capacitance.				1	pF
C_{PIN}	Equivalent Single ended Package + PCB capacitance.				2	pF
L_S	Equivalent wire bond series inductance				1.5	nH
R_S	Equivalent wire bond series resistance				0.15	Ω
R_L	Load resistance		80	100	125	Ω

4.11.12.6 High-Speed Clock Timing

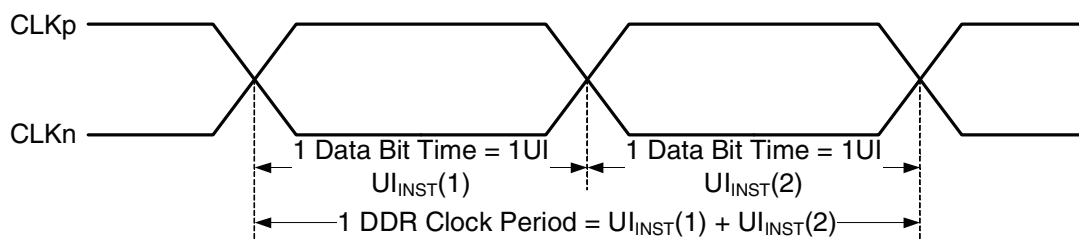


Figure 74. DDR Clock Definition

4.11.12.7 Forward High-Speed Data Transmission Timing

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 75:

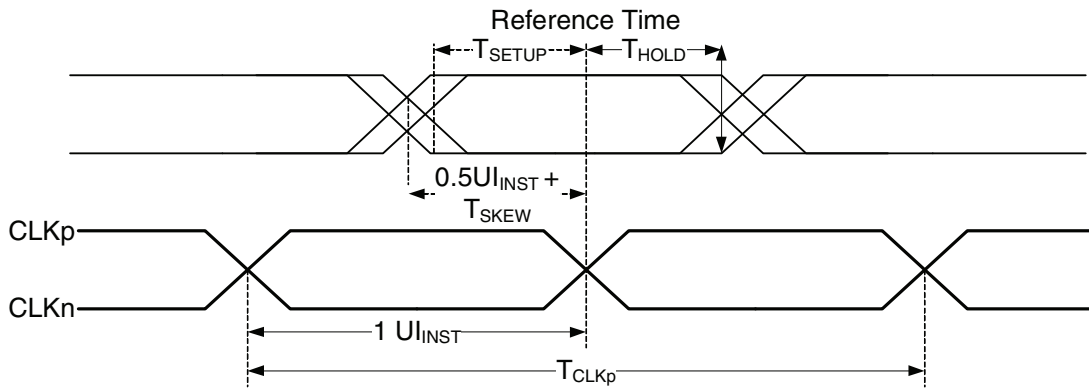


Figure 75. Data to Clock Timing Definitions

4.11.12.8 Reverse High-Speed Data Transmission Timing

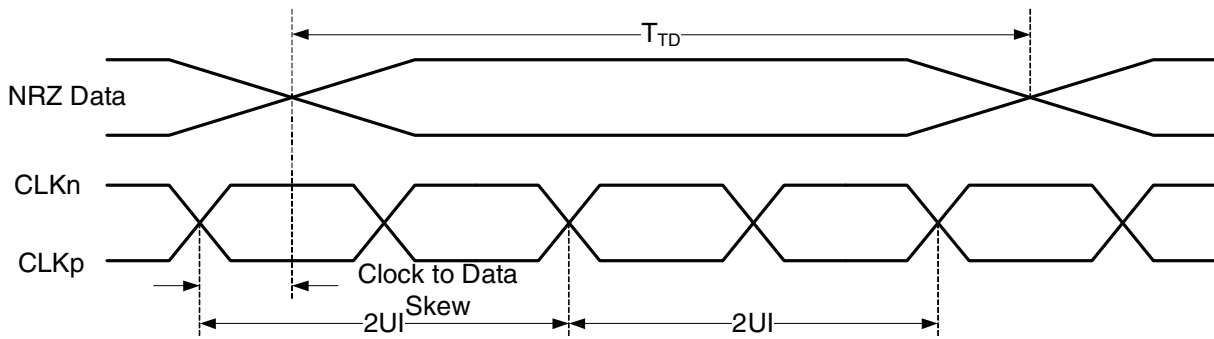


Figure 76. Reverse High-Speed Data Transmission Timing at Slave Side

4.11.12.9 Low-Power Receiver Timing

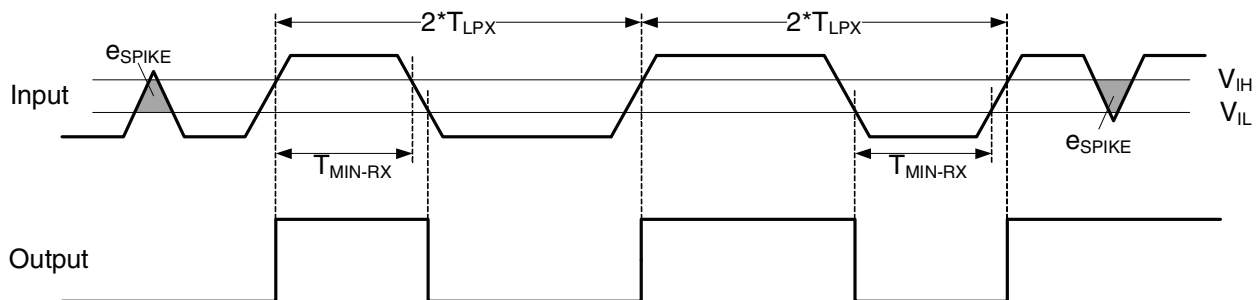


Figure 77. Input Glitch Rejection of Low-Power Receivers

4.11.13 HSI Host Controller Timing Parameters

This section describes the timing parameters of the HSI Host Controller which are compliant with High-speed Synchronous Serial Interface (HSI) Physical Layer specification version 1.01.

4.11.13.1 Synchronous Data Flow

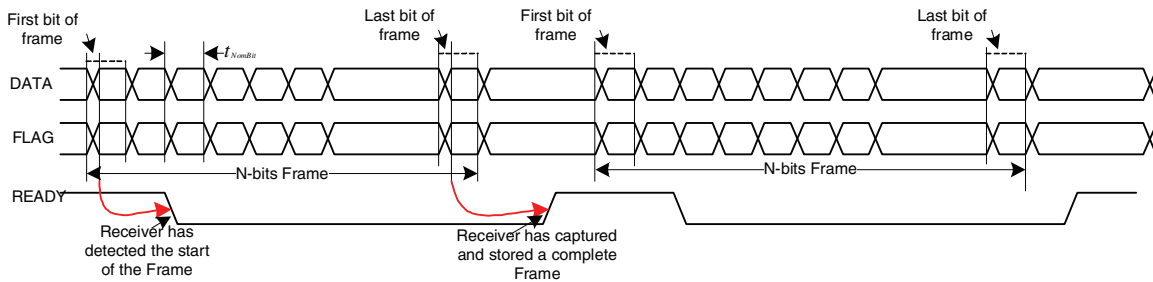


Figure 78. Synchronized Data Flow READY Signal Timing (Frame and Stream Transmission)

4.11.13.2 Pipelined Data Flow

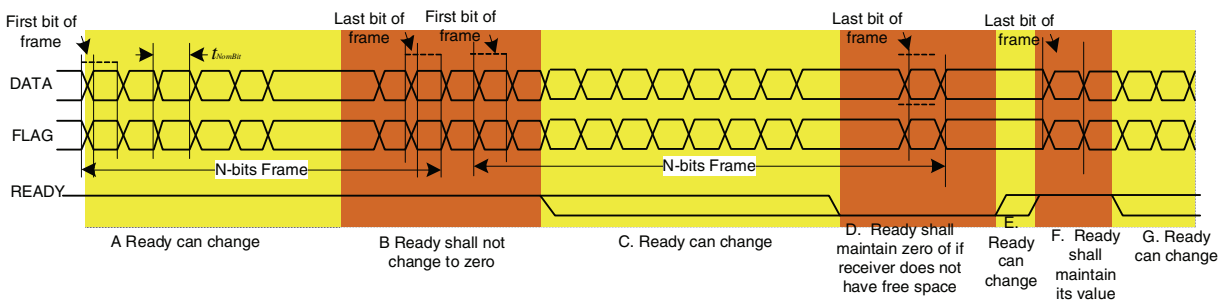


Figure 79. Pipelined Data Flow Ready Signal Timing (Frame Transmission Mode)

4.11.13.3 Receiver Real-Time Data Flow

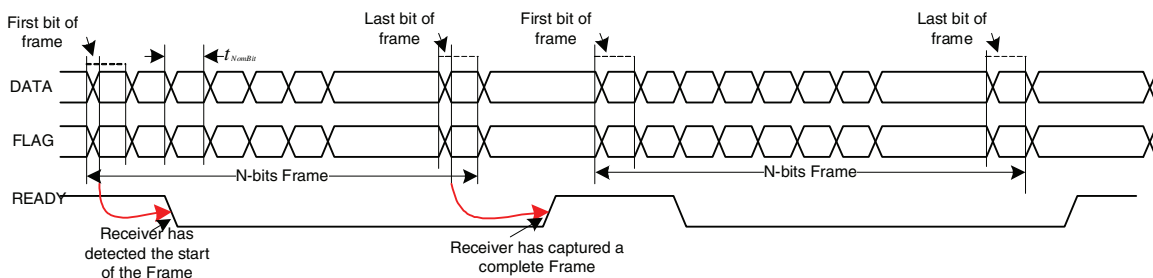


Figure 80. Receiver Real-Time Data Flow READY Signal Timing

4.11.13.4 Synchronized Data Flow Transmission with Wake

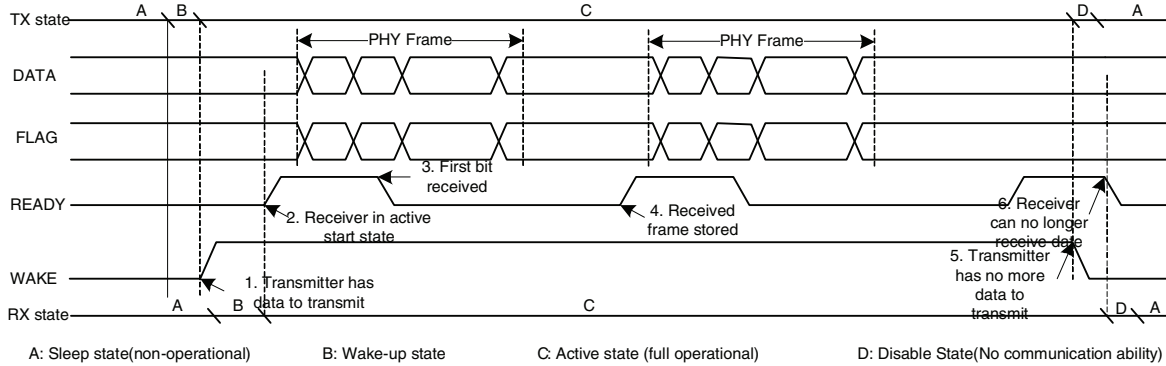


Figure 81. Synchronized Data Flow Transmission with WAKE

4.11.13.5 Stream Transmission Mode Frame Transfer

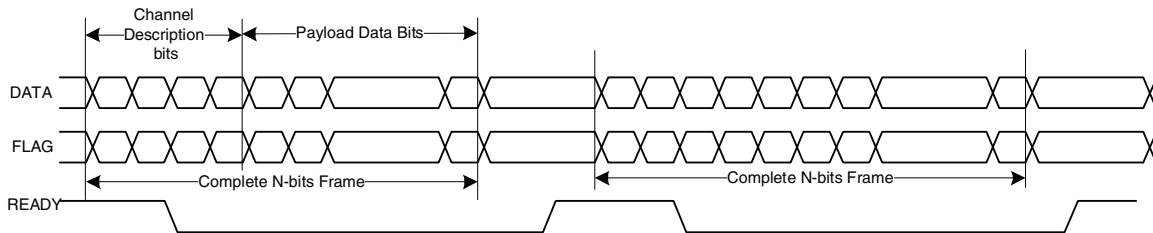


Figure 82. Stream Transmission Mode Frame Transfer (Synchronized Data Flow)

4.11.13.6 Frame Transmission Mode (Synchronized Data Flow)

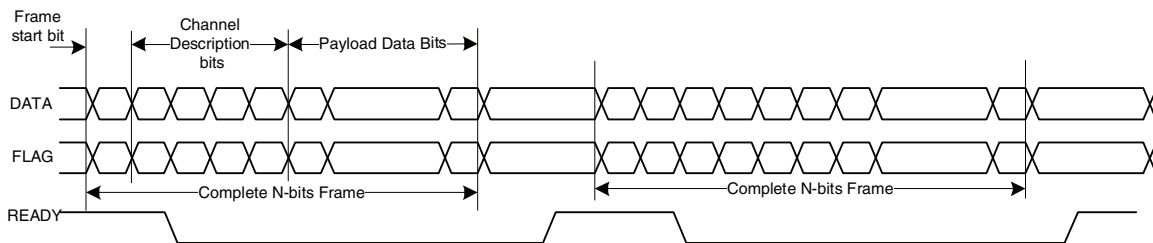


Figure 83. Frame Transmission Mode Transfer of Two Frames (Synchronized Data Flow)

4.11.13.7 Frame Transmission Mode (Pipelined Data Flow)

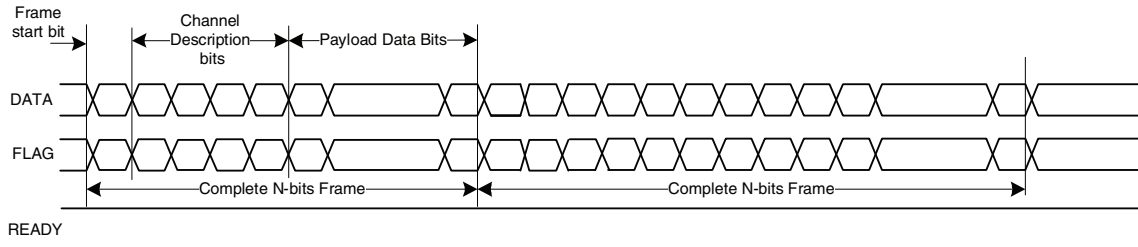


Figure 84. Frame Transmission Mode Transfer of Two Frames (Pipelined Data Flow)

4.11.13.8 DATA and FLAG Signal Timing Requirement for a 15 pF Load

Table 77. DATA and FLAG Timing

Parameter	Description	1 Mbit/s	100 Mbit/s	200 Mbit/s
$t_{Bit, nom}$	Nominal bit time	1000 ns	10.0 ns	5.00 ns
$t_{Rise, min}$ and $t_{Fall, min}$	Minimum allowed rise and fall time	2.00 ns	2.00 ns	1.00 ns
$t_{TxToRxSkew, maxfq}$	Maximum skew between transmitter and receiver package pins	50.0 ns	0.5.0 ns	0.25 ns
$t_{EageSepTx, min}$	Minimum allowed separation of signal transitions at transmitter package pins, including all timing defects, for example, jitter and skew, inside the transmitter.	400 ns	4.00 ns	2.00 ns
$t_{EageSepRx, min}$	Minimum separation of signal transitions, measured at the receiver package pins, including all timing defects, for example, jitter and skew, inside the receiver.	350 ns	3.5 ns	1.75 ns

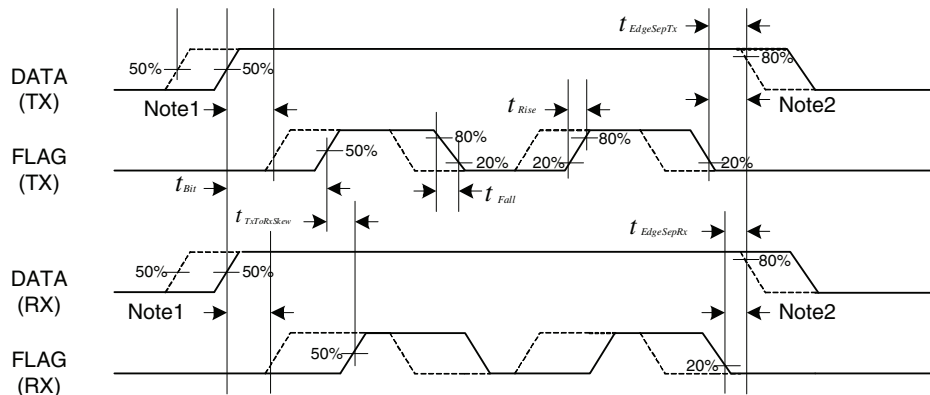


Figure 85. DATA and FLAG Signal Timing

Note:

- ¹ This case shows that the DATA signal has slowed down more compared to the FLAG signal
- ² This case shows that the FLAG signal has slowed down more compared to the DATA signal.

4.11.14 MediaLB (MLB) Characteristics

4.11.14.1 MediaLB (MLB) DC Characteristics

Table 78 lists the MediaLB 3-pin interface electrical characteristics.

Table 78. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note ¹	1.8	—	V
Low level output threshold	V_{OL}	$I_{OL} = 6 \text{ mA}$	—	0.4	V
High level output threshold	V_{OH}	$I_{OH} = -6 \text{ mA}$	2.0	—	V
Input leakage current	I_L	$0 < V_{in} < V_{DD}$	—	± 10	μA

¹ Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

Table 79 lists the MediaLB 6-pin interface electrical characteristics.

Table 79. MediaLB 6-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Driver Characteristics					
Differential output voltage (steady-state): $ V_{O+} - V_{O-} $	V_{OD}	See Note ¹	300	500	mV
Difference in differential output voltage between (high/low) steady-states: $ V_{OD, high} - V_{OD, low} $	ΔV_{OD}	—	-50	50	mV
Common-mode output voltage: $(V_{O+} + V_{O-}) / 2$	V_{OCM}	—	1.0	1.5	V
Difference in common-mode output between (high/low) steady-states: $ V_{OCM, high} - V_{OCM, low} $	ΔV_{OCM}	—	-50	50	mV
Variations on common-mode output during a logic state transitions	V_{CMV}	See Note ²	—	150	mVpp
Short circuit current	$ I_{OS} $	See Note ³	—	43	mA
Differential output impedance	Z_O	—	1.6	—	k Ω
Receiver Characteristics					

Table 79. MediaLB 6-Pin Interface Electrical DC Specifications (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Differential clock input: • logic low steady-state • logic high steady-state • hysteresis	V_{ILC} V_{IHC} V_{HSC}	See Note ⁴	50 -25	-50 25	mV mV mV
Differential signal/data input: • logic low steady-state • logic high steady-state	V_{ILS} V_{IHS}	—	50	-50	mV mV
Signal-ended input voltage (steady-state): • MLBSP, MLBDP • MLBSN, MLBDN	V_{IN+} V_{IN-}	—	0.5 0.5	2.0 2.0	V V

¹ The signal-ended output voltage of a driver is defined as V_{O+} on MLBCP, MLBSP, and MLBDP. The signal-ended output voltage of a driver is defined as V_{O-} on MLBCN, MLBSN, and MLBDN.

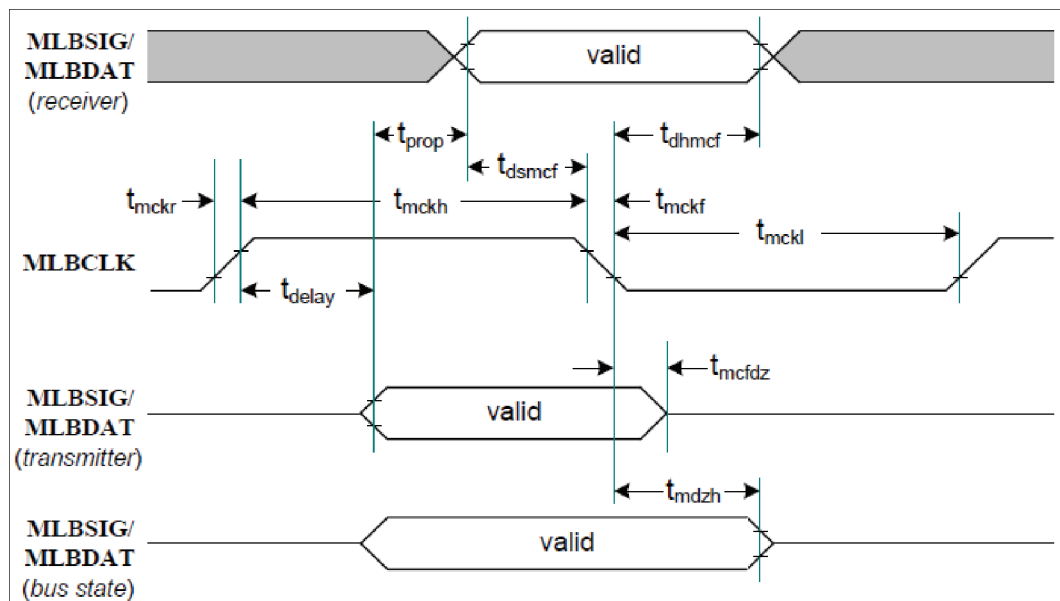
² Variations in the common-mode voltage can occur between logic states (for example, during state transitions) as a result of differences in the transition rate of V_{O+} and V_{O-} .

³ Short circuit current is applicable when V_{O+} and V_{O-} are shorted together and/or shorted to ground.

⁴ The logic state of the receiver is undefined when $-50 \text{ mV} < V_{ID} < 50 \text{ mV}$.

4.11.14.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module. Figure 86 show the timing of MediaLB 3-pin interface, and Table 80 and Table 81 lists the MediaLB 3-pin interface timing characteristics.

**Figure 86. MediaLB 3-Pin Timing**

Ground = 0.0 V; Load Capacitance = 60 pF; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 80. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency ¹	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz 512xFs at 50.0 kHz
MLBCLK rise time	t_{mckr}	—	3	ns	V_{IL} TO V_{IH}
MLBCLK fall time	t_{mckf}	—	3	ns	V_{IH} TO V_{IL}
MLBCLK low time ²	t_{mckl}	30 14	—	ns	256xFs 512xFs
MLBCLK high time	t_{mckh}	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input valid to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mdzh}	—	ns	—
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	4	—	ns	—
MLBSIG/MLBDAT output valid from transition of MLBCLK (low to high)	t_{delay}		10	ns	—

¹ The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.

² MLBCLK low/high time includes the pulse width variation.

³ The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; load capacitance = 40 pF; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed in Table 81; unless otherwise noted.

Table 81. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency ¹	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLBCLK rise time	t_{mckr}	—	1	ns	V_{IL} TO V_{IH}
MLBCLK fall time	t_{mckf}	—	1	ns	V_{IH} TO V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	—
MLBSIG/MLBDAT receiver input valid to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mdzh}	—	ns	—

Table 81. MLB 1024 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
MLBSIG/MLBDAT output high impedance from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	—
MLBSIG/MLBDAT output valid from transition of MLBCLK (low to high)	t_{delay}	—	7	ns	—

¹ The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.

² MLBCLK low/high time includes the pulse width variation.

³ The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for t_{mdzh} . Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 82 lists the MediaLB 6-pin interface timing characteristics, and Figure 87 shows the MLB 6-pin delay, setup, and hold times.

Table 82. MLB 6-Pin Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
Cycle-to-cycle system jitter	t_{jitter}	—	600	ps	—
Transmitter MLBSP/N (MLBDP/N) output valid from transition of MLBCP/N (low-to-high) ¹	t_{delay}	0.6	1.3	ns	
Disable turnaround time from transition of MLBCP/N (low-to-high)	t_{phz}	0.6	3.5	ns	
Enable turnaround time from transition of MLBCP/N (low-to-high)	t_{plz}	0.6	5.6	ns	
MLBSP/N (MLBDP/N) valid to transition of MLBCP/N (low-to-high)	t_{su}	0.05	—	ns	
MLBSP/N (MLBDP/N) hold from transition of MLBCP/N (low-to-high) ²	t_{hd}	0.6			

¹ t_{delay} , t_{phz} , t_{plz} , t_{su} , and t_{hd} may also be referenced from a low-to-high transition of the recovered clock for 2:1 and 4:1 recovered-to-external clock ratios.

² The transmitting device must ensure valid data on MLBSP/N (MLBDP/N) for at least $t_{hd(min)}$ following the rising edge of MLBCP/N; receivers must latch MLBSP/N (MLBDP/N) data within $t_{hd(min)}$ of the rising edge of MLBCP/N.

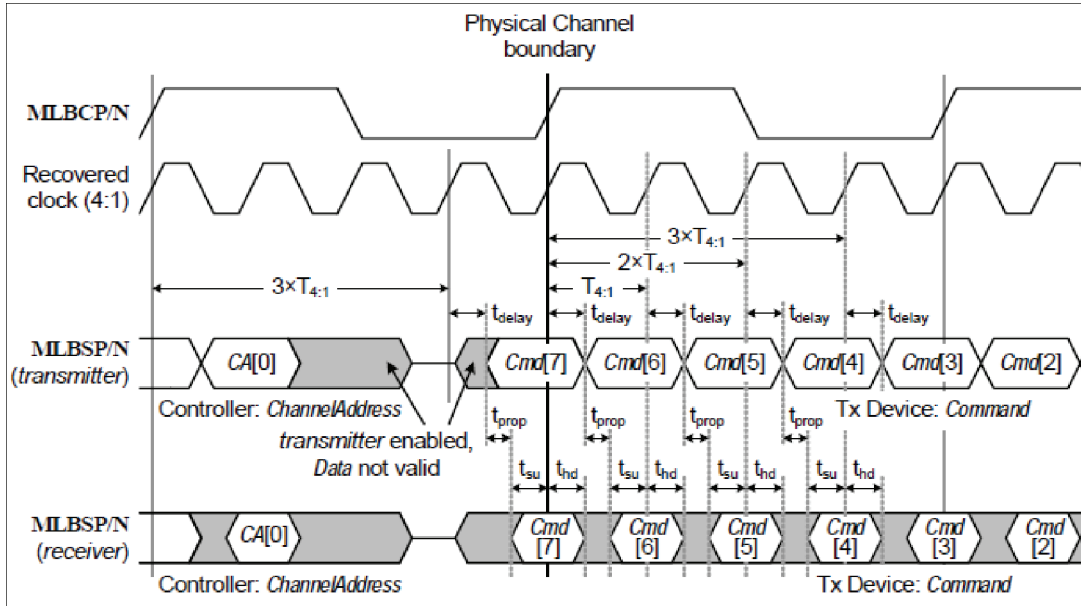


Figure 87. MLB 6-Pin Delay, Setup, and Hold Times

4.11.15 PCIe PHY Parameters

The PCIe interface complies with PCIe specification Gen2 x1 lane and supports the PCI Express 1.1/2.0 standard.

4.11.15.1 PCIE_REXT Reference Resistor Connection

The impedance calibration process requires connection of reference resistor 200 Ω. 1% precision resistor on PCIE_REXT pads to ground. It is used for termination impedance calibration.

4.11.16 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 88 depicts the timing of the PWM, and Table 83 lists the PWM timing parameters.

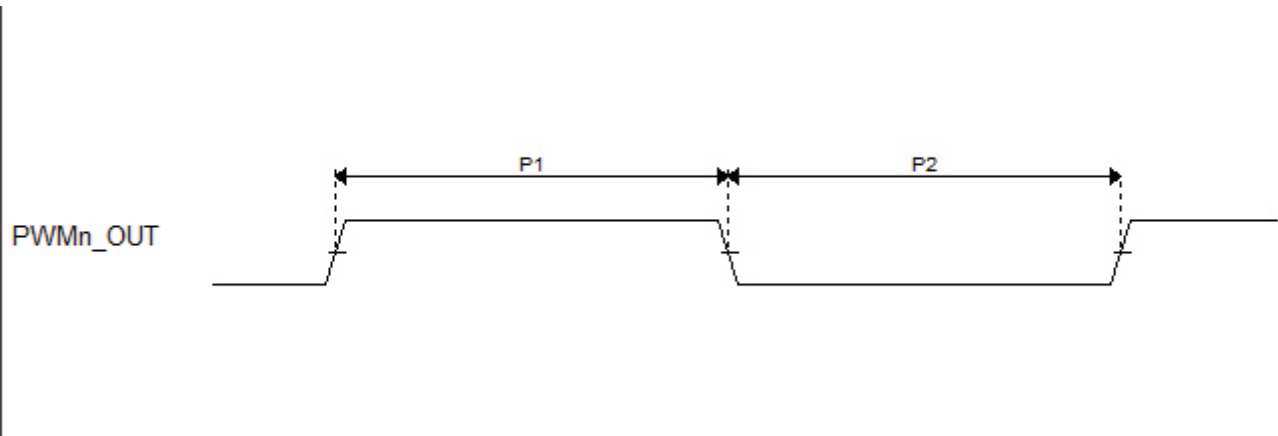


Figure 88. PWM Timing

Table 83. PWM Output Timing Parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	ipg_clk	MHz
P1	PWM output pulse width high	15		ns
P2	PWM output pulse width low	15		ns

4.11.17 SCAN JTAG Controller (SJC) Timing Parameters

Figure 89 depicts the SJC test clock input timing. Figure 90 depicts the SJC boundary scan timing. Figure 91 depicts the SJC test access port. Signal parameters are listed in Table 84.

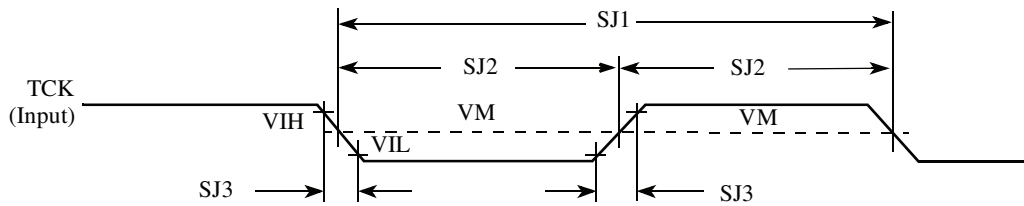


Figure 89. Test Clock Input Timing Diagram

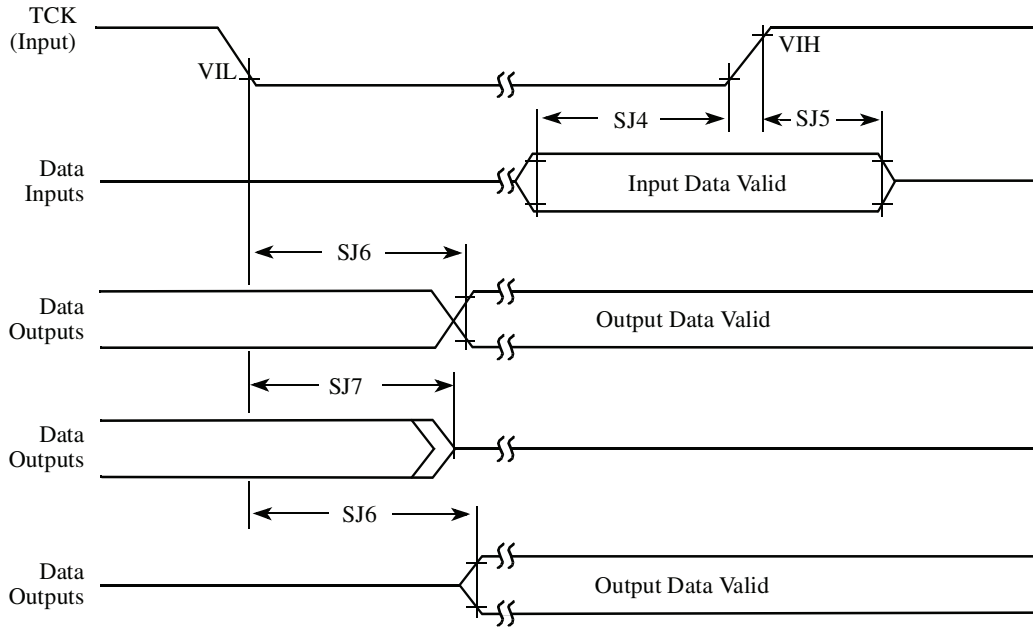


Figure 90. Boundary Scan (JTAG) Timing Diagram

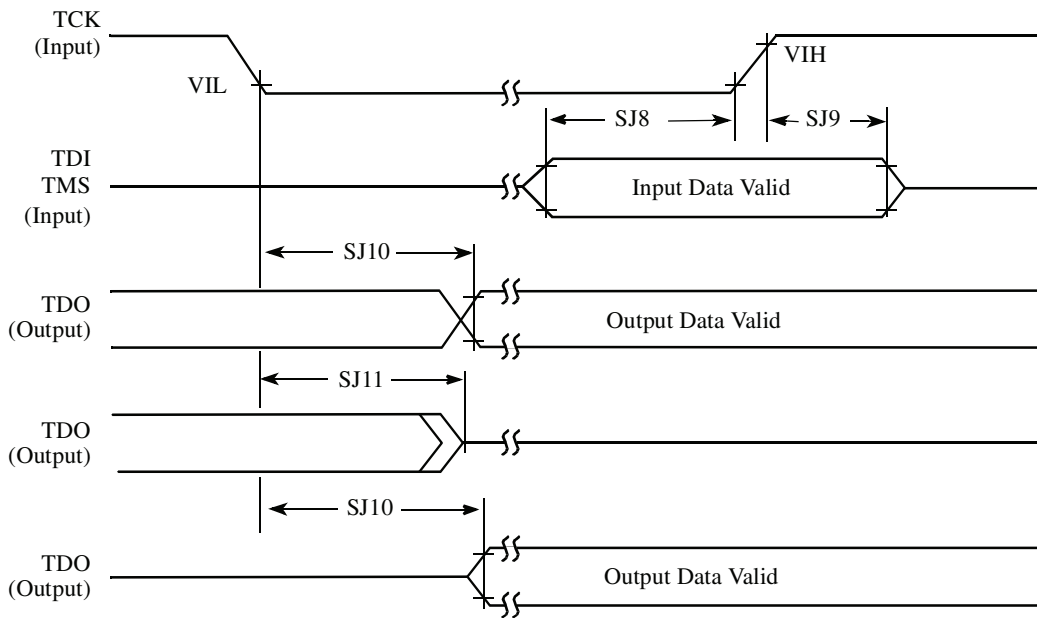


Figure 91. Test Access Port Timing Diagram

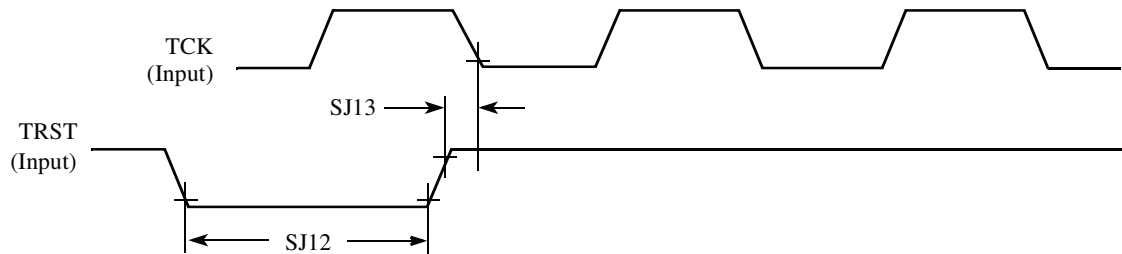
Figure 92. $\overline{\text{TRST}}$ Timing Diagram

Table 84. JTAG Timing

ID	Parameter ^{1,2}	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \cdot T_{DC})^1$	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M^2	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

¹ T_{DC} = target frequency of SJC² V_M = mid-point voltage

4.11.18 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 85 and Figure 93 and Figure 94 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 85. SPDIF Timing Parameters

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIFOUT output (Load = 50pf)	—	—	1.5	ns
• Skew	—	—	24.2	
• Transition rising	—	—	31.3	
SPDIFOUT1 output (Load = 30pf)	—	—	1.5	ns
• Skew	—	—	13.6	
• Transition falling	—	—	18.0	
Modulating Rx clock (SRCK) period	srckp	40.0	—	ns
SRCK high period	srckph	16.0	—	ns
SRCK low period	srckpl	16.0	—	ns
Modulating Tx clock (STCLK) period	stclkp	40.0	—	ns
STCLK high period	stclkph	16.0	—	ns
STCLK low period	stclkpl	16.0	—	ns

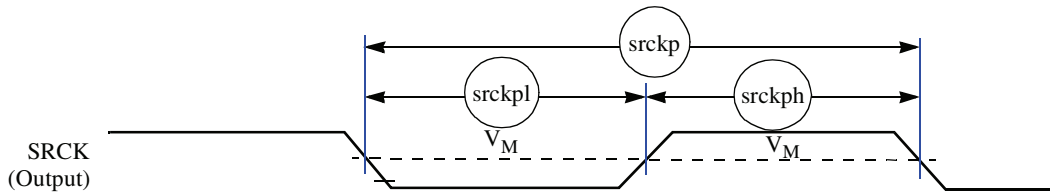


Figure 93. SRCK Timing Diagram

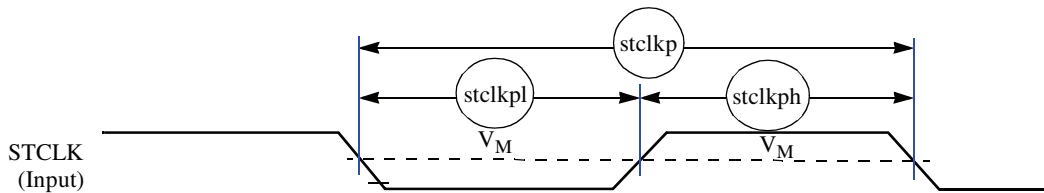


Figure 94. STCLK Timing Diagram

4.11.19 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces are summarized in [Table 86](#).

Table 86. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External— AUD3 I/O
AUDMUX port 4	AUD4	External— EIM or CSPI1 I/O through IOMUXC
AUDMUX port 5	AUD5	External— EIM or SD1 I/O through IOMUXC
AUDMUX port 6	AUD6	External— EIM or DISP2 through IOMUXC
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables see Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)* are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as RGMII_TXC.

4.11.19.1 SSI Transmitter Timing with Internal Clock

Figure 95 depicts the SSI transmitter internal clock timing and Table 87 lists the timing parameters for the SSI transmitter internal clock.

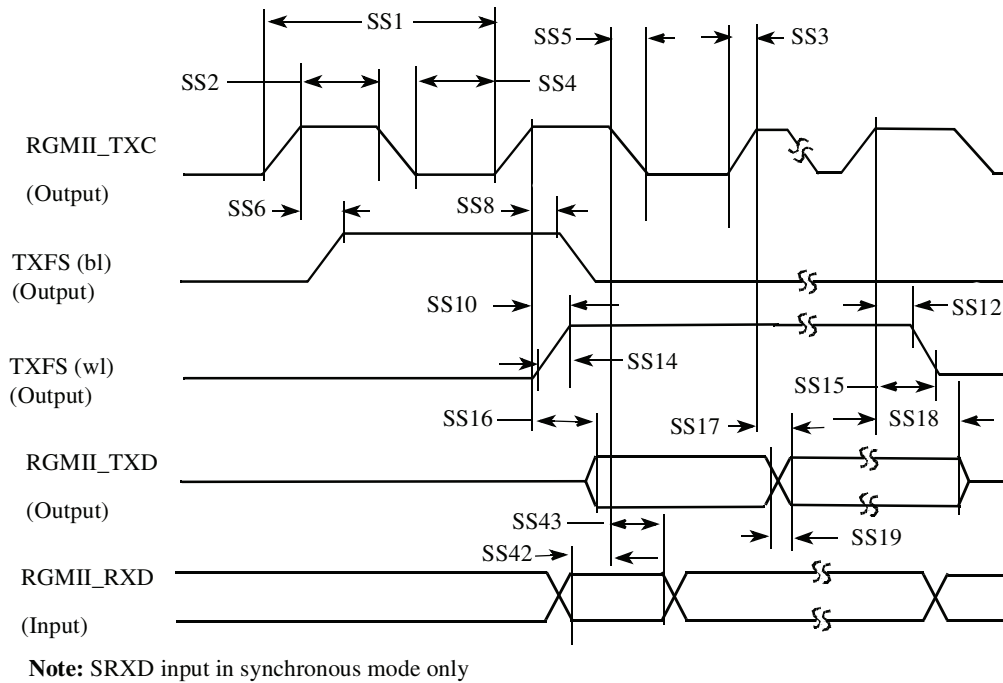


Figure 95. SSI Transmitter Internal Clock Timing Diagram

Table 87. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns

Table 87. SSI Transmitter Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	10.0	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.2 SSI Receiver Timing with Internal Clock

Figure 96 depicts the SSI receiver internal clock timing and Table 88 lists the timing parameters for the receiver timing with the internal clock.

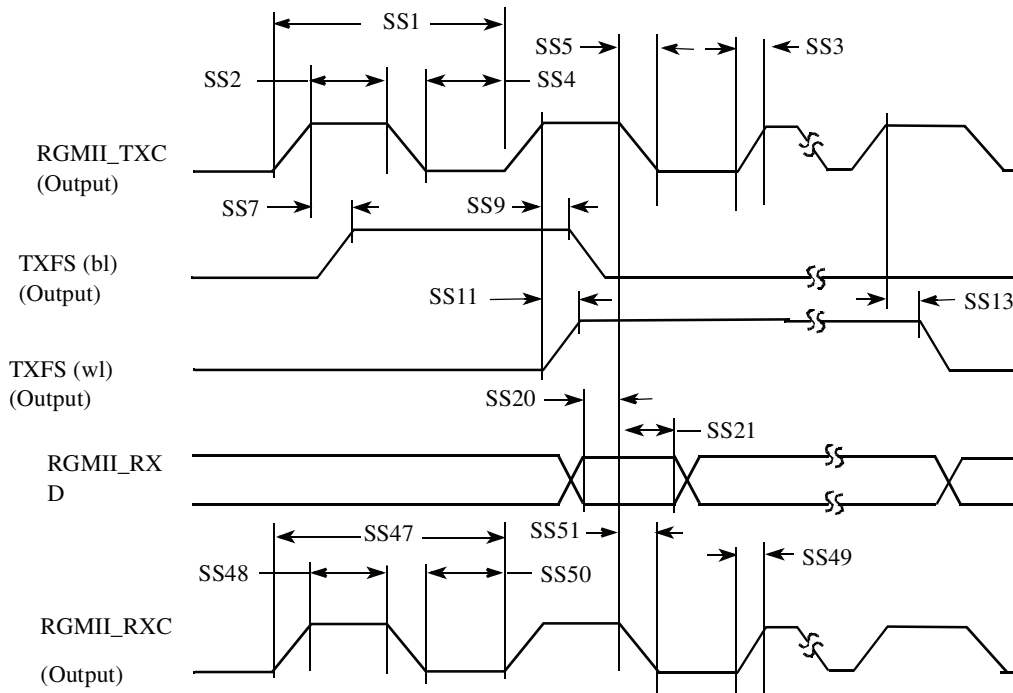


Figure 96. SSI Receiver Internal Clock Timing Diagram

Table 88. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	10.0	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns
Oversampling Clock Operation				

Table 88. SSI Receiver Timing with Internal Clock (continued)

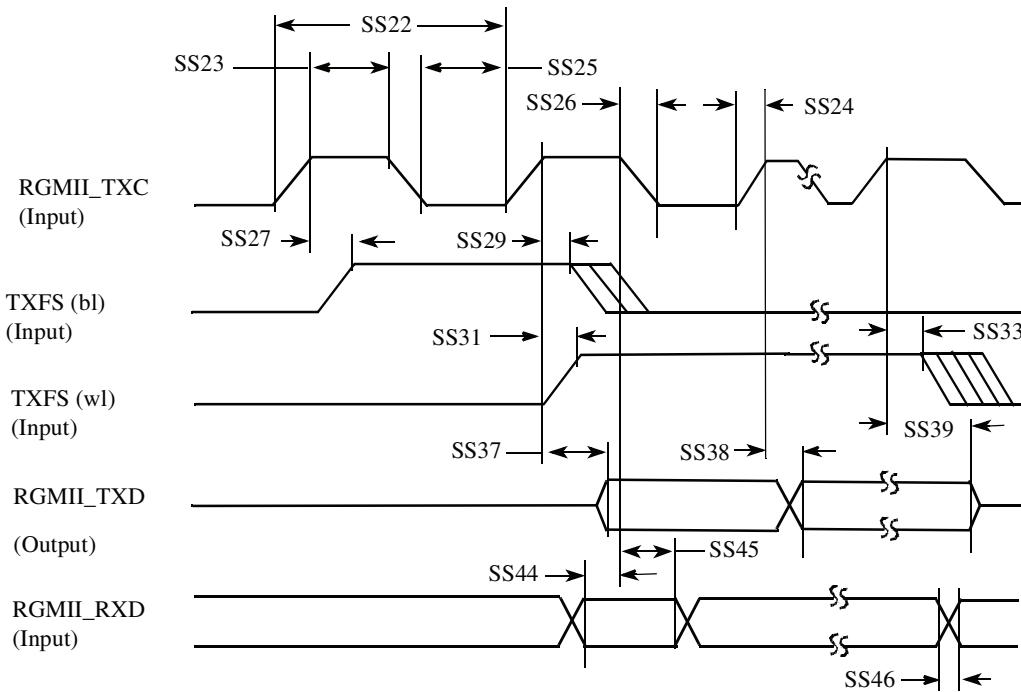
ID	Parameter	Min	Max	Unit
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.3 SSI Transmitter Timing with External Clock

Figure 97 depicts the SSI transmitter external clock timing and Table 89 lists the timing parameters for the transmitter timing with the external clock.



Note: SRXD Input in Synchronous mode only

Figure 97. SSI Transmitter External Clock Timing Diagram

Table 89. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	-10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	-10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	15.0	ns

Table 89. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.19.4 SSI Receiver Timing with External Clock

Figure 98 depicts the SSI receiver external clock timing and Table 90 lists the timing parameters for the receiver timing with the external clock.

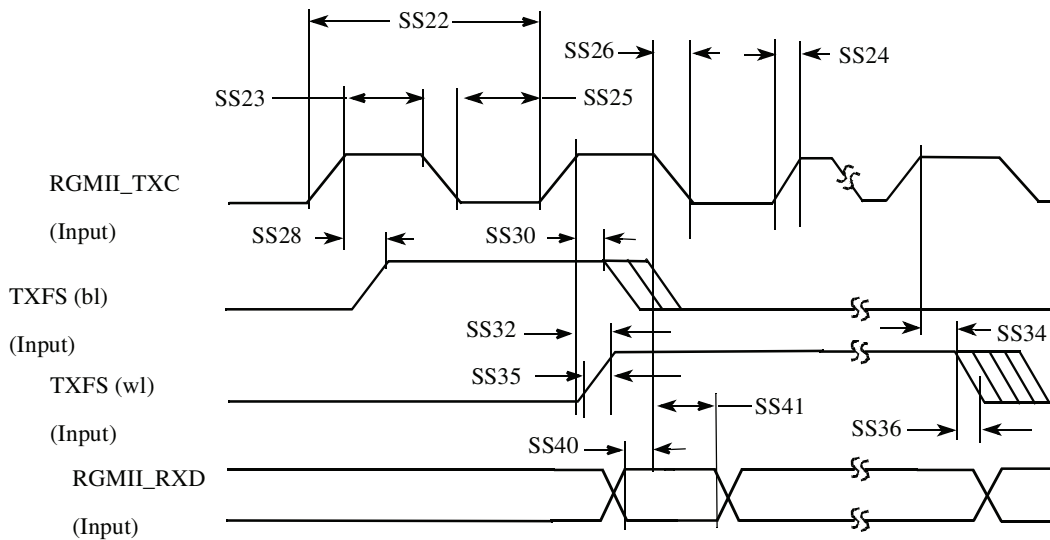


Figure 98. SSI Receiver External Clock Timing Diagram

Table 90. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	-10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	-10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.11.20 UART I/O Configuration and Timing Parameters**4.11.20.1 UART RS-232 I/O Configuration in Different Modes**

The i.MX 6Solo/6DualLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 — DCE mode). [Table 91](#) shows the UART I/O configuration based on the enabled mode.

Table 91. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.11.20.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.11.20.2.1 UART Transmitter

Figure 99 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 92 lists the UART RS-232 serial mode transmit timing characteristics.

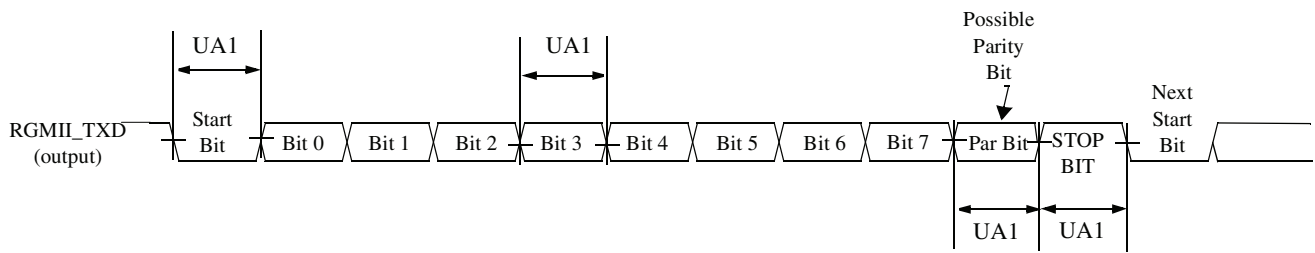


Figure 99. UART RS-232 Serial Mode Transmit Timing Diagram

Table 92. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}^1 - T_{ref_clk}^2$	$1/F_{baud_rate} + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

4.11.20.2.2 UART Receiver

Figure 100 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 93 lists serial mode receive timing characteristics.

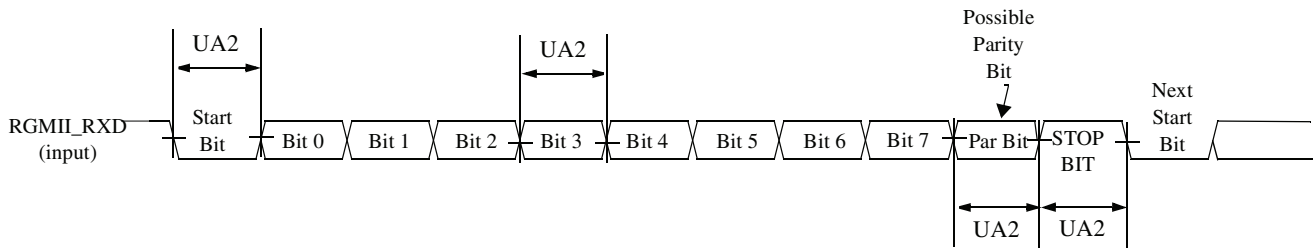


Figure 100. UART RS-232 Serial Mode Receive Timing Diagram

Table 93. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time ¹	t_{Rbit}	$1/F_{baud_rate}^2 - 1/(16 \times F_{baud_rate})$	$1/F_{baud_rate} + 1/(16 \times F_{baud_rate})$	—

¹ The UART receiver can tolerate $1/(16 \times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud_rate})$.

² F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

4.11.20.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 101 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 94 lists the transmit timing characteristics.

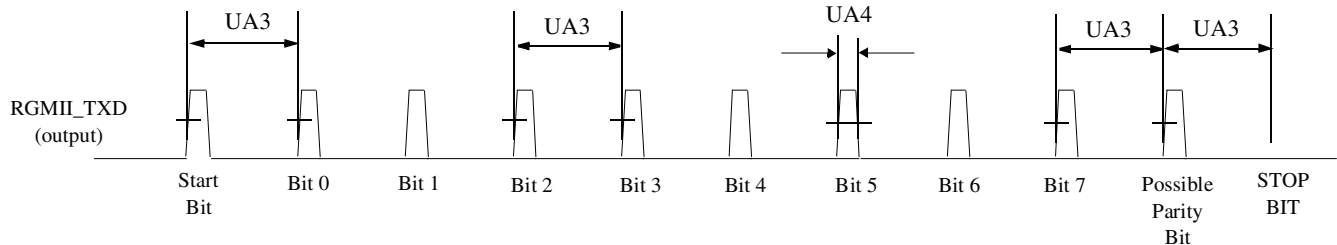


Figure 101. UART IrDA Mode Transmit Timing Diagram

Table 94. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$\frac{1}{F_{baud_rate}} - \frac{1}{F_{ref_clk}}$ ¹	$\frac{1}{F_{baud_rate}} + T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(\frac{3}{16}) \times (\frac{1}{F_{baud_rate}}) - T_{ref_clk}$	$(\frac{3}{16}) \times (\frac{1}{F_{baud_rate}}) + T_{ref_clk}$	—

¹ F_{baud_rate} : Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

² T_{ref_clk} : The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART IrDA Mode Receiver

Figure 102 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 95 lists the receive timing characteristics.

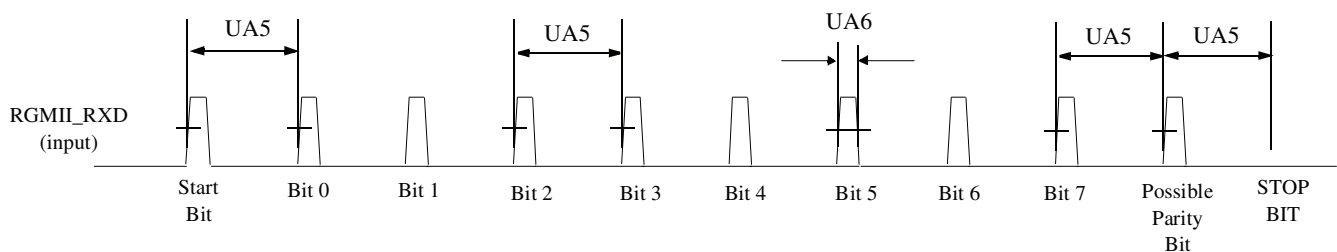


Figure 102. UART IrDA Mode Receive Timing Diagram

Table 95. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time ¹ in IrDA mode	t_{RIRbit}	$\frac{1}{F_{baud_rate}} - \frac{1}{(16 \times F_{baud_rate})}$ ²	$\frac{1}{F_{baud_rate}} + \frac{1}{(16 \times F_{baud_rate})}$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 μ s	$(\frac{5}{16}) \times (\frac{1}{F_{baud_rate}})$	—

Electrical Characteristics

- ¹ The UART receiver can tolerate $1/(16 \times F_{\text{baud_rate}})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{\text{baud_rate}})$.
- ² $F_{\text{baud_rate}}$: Baud rate frequency. The maximum baud rate the UART can support is $(ipg_perclk \text{ frequency})/16$.

4.11.21 USB HSIC Timings

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is DDR signal, following timing spec is for both rising and falling edge.

4.11.21.1 Transmit Timing

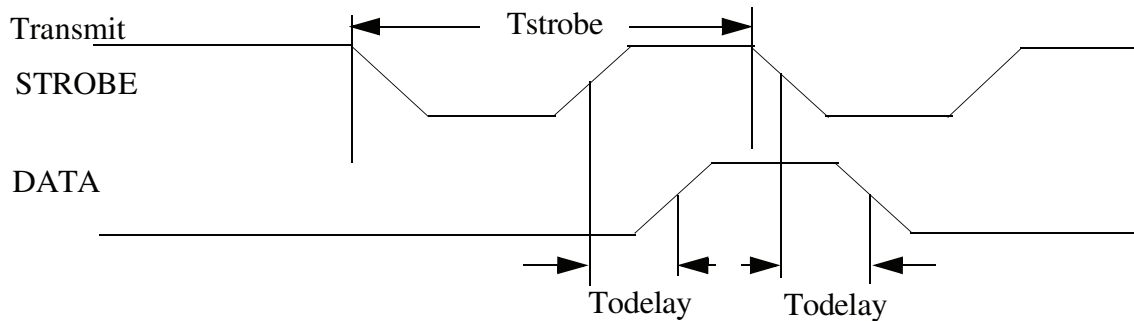


Figure 103. USB HSIC Transmit Waveform

Table 96. USB HSIC Transmit Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Todelay	data output delay time	550	1350	ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.11.21.2 Receive Timing

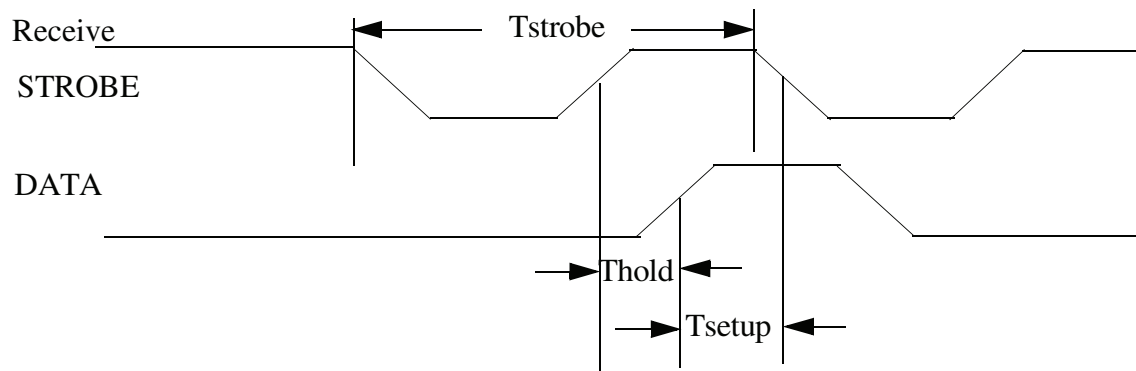


Figure 104. USB HSIC Receive Waveform

Table 97. USB HSIC Receive Parameters¹

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	strobe period	4.166	4.167	ns	
Thold	data hold time	300		ps	Measured at 50% point
Tsetup	data setup time	365		ps	Measured at 50% point
Tslew	strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

¹ The timings in the table are guaranteed when:
 —AC I/O voltage is between 0.9x to 1x of the I/O supply
 —DDR_SEL configuration bits of the I/O are set to (10)b

4.11.22 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
 - Title: 5V Short Circuit Withstand Requirement Change
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
 - Title: Pull-up/Pull-down resistors
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
 - Title: Suspend Current Limit Changes
 - Applies to: Universal Serial Bus Specification, Revision 2.0

Boot Mode Configuration

- USB ENGINEERING CHANGE NOTICE
 - Title: USB 2.0 Phase Locked SOFs
 - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
 - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
 - Revision 1.2, December 7, 2010

5 Boot Mode Configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

5.1 Boot Mode Configuration Pins

Table 98 provides boot options, functionality, fuse values, and associated pins. Several input pins are also sampled at reset and can be used to override fuse values, depending on the value of BT_FUSE_SEL fuse. The boot option pins are in effect when BT_FUSE_SEL fuse is '0' (cleared, which is the case for an unblown fuse). For detailed boot mode options configured by the boot mode pins, see the i.MX 6Solo/6DualLite Fuse Map document and the System Boot chapter in *i.MX 6Solo/6DualLite Reference Manual (IMX6SDLRM)*.

Table 98. Fuses and Associated Pins Used for Boot

Pin	Direction at Reset	eFuse Name	Details
BOOT_MODE1	Input	N/A	Boot Mode selection
BOOT_MODE0	Input	N/A	Boot Mode Selection

Table 98. Fuses and Associated Pins Used for Boot (continued)

Pin	Direction at Reset	eFuse Name	Details
EIM_DA0	Input	BOOT_CFG1[0]	Boot Options, Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.
EIM_DA1	Input	BOOT_CFG1[1]	
EIM_DA2	Input	BOOT_CFG1[2]	
EIM_DA3	Input	BOOT_CFG1[3]	
EIM_DA4	Input	BOOT_CFG1[4]	
EIM_DA5	Input	BOOT_CFG1[5]	
EIM_DA6	Input	BOOT_CFG1[6]	
EIM_DA7	Input	BOOT_CFG1[7]	
EIM_DA8	Input	BOOT_CFG2[0]	
EIM_DA9	Input	BOOT_CFG2[1]	
EIM_DA10	Input	BOOT_CFG2[2]	
EIM_DA11	Input	BOOT_CFG2[3]	
EIM_DA12	Input	BOOT_CFG2[4]	
EIM_DA13	Input	BOOT_CFG2[5]	
EIM_DA14	Input	BOOT_CFG2[6]	
EIM_DA15	Input	BOOT_CFG2[7]	
EIM_A16	Input	BOOT_CFG3[0]	
EIM_A17	Input	BOOT_CFG3[1]	
EIM_A18	Input	BOOT_CFG3[2]	
EIM_A19	Input	BOOT_CFG3[3]	
EIM_A20	Input	BOOT_CFG3[4]	
EIM_A21	Input	BOOT_CFG3[5]	
EIM_A22	Input	BOOT_CFG3[6]	
EIM_A23	Input	BOOT_CFG3[7]	
EIM_A24	Input	BOOT_CFG4[0]	
EIM_WAIT	Input	BOOT_CFG4[1]	
EIM_LBA	Input	BOOT_CFG4[2]	
EIM_EB0	Input	BOOT_CFG4[3]	
EIM_EB1	Input	BOOT_CFG4[4]	
EIM_RW	Input	BOOT_CFG4[5]	
EIM_EB2	Input	BOOT_CFG4[6]	
EIM_EB3	Input	BOOT_CFG4[7]	

5.2 Boot Device Interface Allocation

Table 99 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 99. Interface Allocation During Boot

Interface	IP Instance	Allocated Pads During Boot	Comment
SPI	ECSPI-1	EIM_D17, EIM_D18, EIM_D16, EIM_EB2, EIM_D19, EIM_D24, EIM_D25	
SPI	ECSPI-2	CSIO_DAT10, CSIO_DAT9, CSIO_DAT8, CSIO_DAT11, EIM_LBA, EIM_D24, EIM_D25	
SPI	ECSPI-3	DISP0_DAT2, DISP0_DAT1, DISP0_DAT0, DISP0_DAT3, DISP0_DAT4, DISP0_DAT5, DISP0_DAT6	
SPI	ECSPI-4	EIM_D22, EIM_D28, EIM_D21, EIM_D20, EIM_A25, EIM_D24, EIM_D25	
EIM	EIM	EIM_DA[15:0], EIM_D[31:16], CSIO_DAT[19:4], CSIO_DATA_EN, CSIO_VSYNC	Used for NOR, OneNAND boot Only CS0 is supported
NAND Flash	GPMI	NANDF_CLE, NANDF_ALE, NANDF_WP_B, SD4_CMD, SD4_CLK, NANDF_RB0, SD4_DAT0, NANDF_CS0, NANDF_CS1, NANDF_CS2, NANDF_CS3, NANDF_D[7:0]	8 bit Only CS0 is supported
SD/MMC	USDHC-1	SD1_CLK, SD1_CMD, SD1_DAT0, SD1_DAT1, SD1_DAT2, SD1_DAT3, GPIO_1, NANDF_D0, NANDF_D1, NANDF_D2, NANDF_D3, KEY_COL1	1, 4, or 8 bit
SD/MMC	USDHC-2	SD2_CLK, SD2_CMD, SD2_DAT0, SD2_DAT1, SD2_DAT2, SD2_DAT3, GPIO_4, NANDF_D5, NANDF_D6, NANDF_D7, NANDF_D8, KEY_ROW1	1, 4, or 8 bit
SD/MMC	USDHC-3	SD3_CLK, SD3_CMD, SD3_DAT0, SD3_DAT1, SD3_DAT2, SD3_DAT3, SD3_DAT4, SD3_DAT5, SD3_DAT6, SD3_DAT7, SD3_RST, GPIO_18	1, 4, or 8 bit
SD/MMC	USDHC-4	SD4_CLK, SD4_CMD, SD4_DAT0, SD4_DAT1, SD4_DAT2, SD4_DAT3, SD4_DAT4, SD4_DAT5, SD4_DAT6, SD4_DAT7, NANDF_ALE, NANDF_CS1	1, 4, or 8 bit
I ² C	I ² C-1	EIM_D28, EIM_D21	—
I ² C	I ² C-2	EIM_D16, EIM_EB2	—
I ² C	I ² C-3	EIM_D18, EIM_D17	—
USB	USB-OTG PHY	USB_OTG_DP USB_OTG_DN USB_OTG_VBUS	—

6 Package Information and Contact Assignments

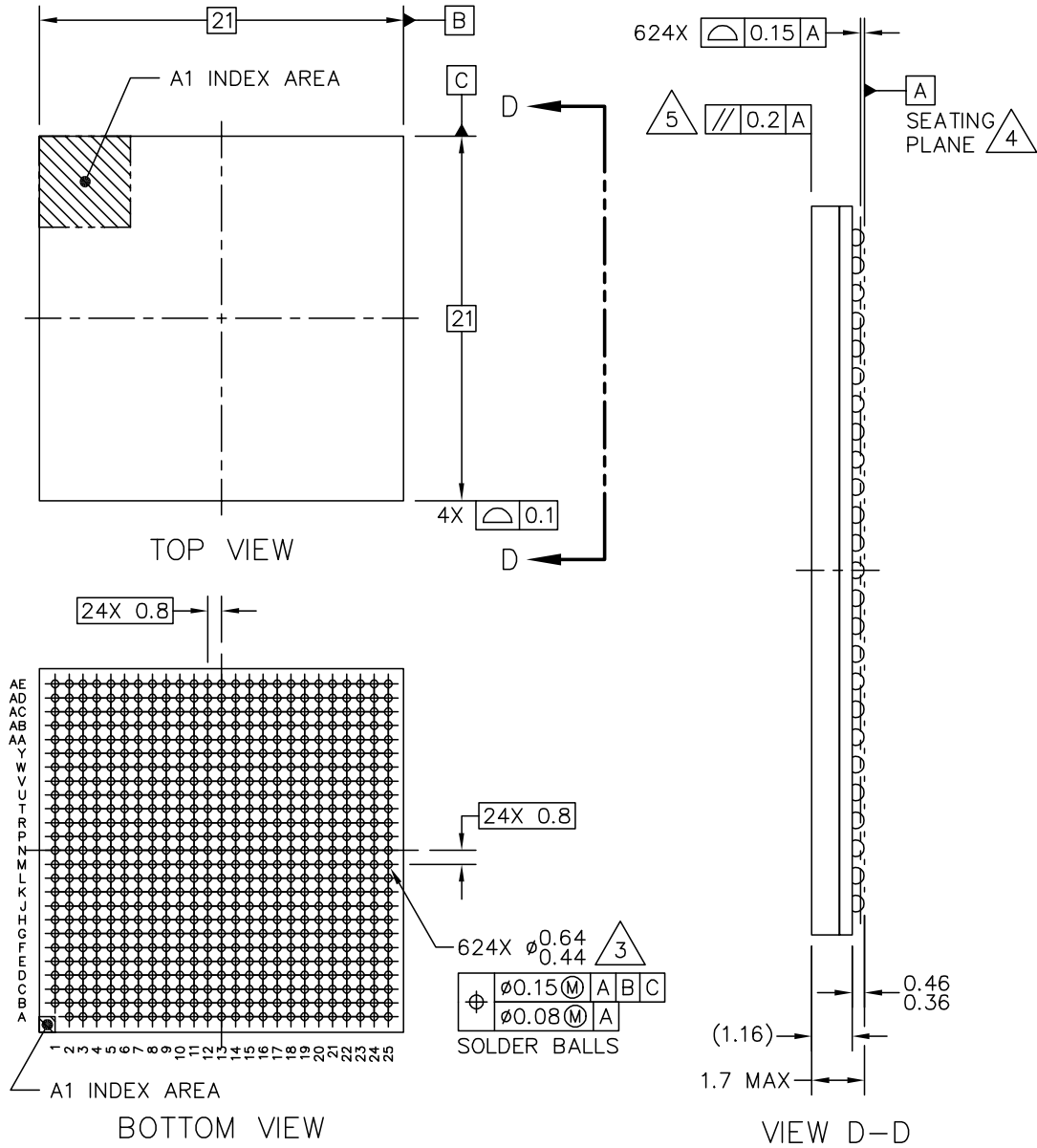
This section includes the contact assignment information and mechanical package drawing.

6.1 21x21 mm Package Information

6.1.1 Case 2240, 21 x 21 mm, 0.8 mm Pitch, 25 x 25 Ball Matrix

[Figure 105](#) shows the top, bottom, and side views of the 21x21 mm BGA package.

Package Information and Contact Assignments



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TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00404D	REV: 0	
	CASE NUMBER: 2240-01	27 SEP 2011	
	STANDARD: NON-JEDEC		

i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors, Rev. 1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: PBGA, LOW PROFILE, FINE PITCH, 624 I/O, 21 X 21 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00404D	REV: 0	
	CASE NUMBER: 2240–01	27 SEP 2011	
	STANDARD: NON–JEDEC		

Figure 105. 21 x 21 mm BGA, Case 2240 Package Top, Bottom, and Side Views

i.MX 6Solo/6DualLite Automotive and Infotainment Applications Processors, Rev. 1

6.1.2 21 x 21 mm Supplies Contact Assignments and Functional Contact Assignments

Table 100 shows supplies contact assignments for the 21 x 21 mm package.

Table 100. 21 x 21 mm Supplies Contact Assignments

Supply Rail Name	Ball(s) Position(s)	Remark
CSI_REXT	D4	
DRAM_VREF	AC2	
DSI_REXT	G4	
GND	A4, A8, A13, A25, B4, C1, C4, C6, C10, D3, D6, D8, E5, E6, E7, F5, F6, F7, F8, G3, G10, G19, H8, H12, H15, H18, J2, J8, J12, J15, J18, K8, K10, K12, K15, K18, L2, L5, L8, L10, L12, L15, L18, M8, M10, M12, M15, M18, N8, N10, N15, N18, P8, P10, P12, P15, P18, R8, R12, R15, R17, T8, T11, T12, T15, T17, T19, U8, U11, U12, U15, U17, U19, V8, V19, W3, W7, W8, W9, W10, W11, W12, W13, W15, W16, W17, W18, W19, Y5, Y24, AA7, AA10, AA13, AA16, AA19, AA22, AB3, AB24, AD4, AD7, AD10, AD13, AD16, AD19, AD22, AE1, AE25	
HDMI_REF	J1	
HDMI_VP	L7	
HDMI_VPH	M7	
NVCC_CSI	N7	Supply of the camera sensor interface
NVCC_DRAM	R18, T18, U18, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18	Supply of the DDR interface
NVCC_EIM	K19, L19, M19	Supply of the EIM interface
NVCC_ENET	R19	Supply of the ENET interface
NVCC_GPIO	P7	Supply of the GPIO interface
NVCC_JTAG	J7	Supply of the JTAG tap controller interface
NVCC_LCD	P19	Supply of the LCD interface
NVCC_LVDS2P5	V7	Supply of the LVDS display interface and DDR pre-drivers
NVCC_MIPI	K7	Supply of the MIPI interface
NVCC_NANDF	G15	Supply of the raw NAND Flash memories interface
NVCC_PLL_OUT	E8	
NVCC_RGMII	G18	Supply of the ENET interface
NVCC_SD1	G16	Supply of the SD card interface
NVCC_SD2	G17	Supply of the SD card interface
NVCC_SD3	G14	Supply of the SD card interface

Table 100. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
PCIE_REXT	A2	
PCIE_VP	H7	
PCIE_VPH	G7	PCI PHY supply
PCIE_VPTX	G8	PCI PHY supply
VDD_SNVS_CAP	G9	Secondary supply for the SNVS (internal regulator output—requires capacitor if internal regulator is used)
VDD_SNVS_IN	G11	Primary supply for the SNVS regulator
VDDARM_CAP	H11, H13, J11, J13, K11, K13, L11, L13, M11, M13, N11, N13, P11, P13, R11, R13	Secondary supply for core (internal regulator output—requires capacitor if internal regulator is used)
VDDARM_IN	H14, J14, K9, K14, L9, L14, M9, M14, N9, N14, P9, P14, R9, R14, T9, U9	Primary supply for the ARM core's regulator
VDDHIGH_CAP	H10, J10	Secondary supply for the 2.5 V domain (internal regulator output—requires capacitor if internal regulator is used)
VDDHIGH_IN	H9, J9	Primary supply for the 2.5 V regulator
VDDPU_CAP	H17, J17, K17, L17, M17, N17, P17	Secondary supply for VPU and GPUs (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_CAP	R10, T10, T13, T14, U10, U13, U14	Secondary supply for SoC and PU regulators (internal regulator output—requires capacitor if internal regulator is used)
VDDSOC_IN	H16, J16, K16, L16, M16, N16, P16, R16, T16, U16	Primary supply for SoC and PU regulators
VDDUSB_CAP	F9	Secondary supply for the 3 V Domain (internal regulator output—requires capacitor if internal regulator is used)
USB_H1_VBUS	D10	Primary supply for the 3 V regulator
USB_OTG_VBUS	E9	Primary supply for the 3 V regulator
HDMI_DDCCEC	K2	Analog Ground (Ground reference for the Hot Plug Detect signal)
FA_ANA	A5	
GPANAIO	C8	
VDD_FA	B5	
ZQPAD	AE17	
NC	C14	
NC	G12	

Table 100. 21 x 21 mm Supplies Contact Assignments (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
NC	G13	
NC	N12	

Table 101 shows an alpha-sorted list of functional contact assignments for the 21 x 21 mm package.

Table 101. 21 x 21 mm Functional Contact Assignments¹

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
BOOT_MODE0	C12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[0]	Input	100 kΩ pull-down
BOOT_MODE1	F12	VDD_SNVS_IN	GPIO	ALT0	src.BOOT_MODE[1]	Input	100 kΩ pull-down
CLK1_N	C7	VDDHIGH_CAP					
CLK1_P	D7	VDDHIGH_CAP					
CLK2_N	C5	VDDHIGH_CAP					
CLK2_P	D5	VDDHIGH_CAP					
CSI_CLK0M	F4	NVCC_MIPI	ANALOG				
CSI_CLK0P	F3	NVCC_MIPI	ANALOG				
CSI_D0M	E4	NVCC_MIPI	ANALOG				
CSI_D0P	E3	NVCC_MIPI	ANALOG				
CSI_D1M	D1	NVCC_MIPI	ANALOG				
CSI_D1P	D2	NVCC_MIPI	ANALOG				
CSI0_DAT10	M1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[28]	Input	100 kΩ pull-up
CSI0_DAT11	M3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[29]	Input	100 kΩ pull-up
CSI0_DAT12	M2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[30]	Input	100 kΩ pull-up
CSI0_DAT13	L1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[31]	Input	100 kΩ pull-up
CSI0_DAT14	M4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[0]	Input	100 kΩ pull-up
CSI0_DAT15	M5	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[1]	Input	100 kΩ pull-up
CSI0_DAT16	L4	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[2]	Input	100 kΩ pull-up
CSI0_DAT17	L3	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[3]	Input	100 kΩ pull-up
CSI0_DAT18	M6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[4]	Input	100 kΩ pull-up
CSI0_DAT19	L6	NVCC_CSI	GPIO	ALT5	gpio6.GPIO[5]	Input	100 kΩ pull-up
CSI0_DAT4	N1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[22]	Input	100 kΩ pull-up
CSI0_DAT5	P2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[23]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
CSI0_DAT6	N4	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[24]	Input	100 kΩ pull-up
CSI0_DAT7	N3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[25]	Input	100 kΩ pull-up
CSI0_DAT8	N6	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[26]	Input	100 kΩ pull-up
CSI0_DAT9	N5	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[27]	Input	100 kΩ pull-up
CSI0_DATA_EN	P3	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[20]	Input	100 kΩ pull-up
CSI0_MCLK	P4	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[19]	Input	100 kΩ pull-up
CSI0_PIXCLK	P1	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[18]	Input	100 kΩ pull-up
CSI0_VSYNC	N2	NVCC_CSI	GPIO	ALT5	gpio5.GPIO[21]	Input	100 kΩ pull-up
DI0_DISP_CLK	N19	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[16]	Input	100 kΩ pull-up
DI0_PIN15	N21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[17]	Input	100 kΩ pull-up
DI0_PIN2	N25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[18]	Input	100 kΩ pull-up
DI0_PIN3	N20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[19]	Input	100 kΩ pull-up
DI0_PIN4	P25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[20]	Input	100 kΩ pull-up
DISP0_DAT0	P24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[21]	Input	100 kΩ pull-up
DISP0_DAT1	P22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[22]	Input	100 kΩ pull-up
DISP0_DAT10	R21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[31]	Input	100 kΩ pull-up
DISP0_DAT11	T23	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[5]	Input	100 kΩ pull-up
DISP0_DAT12	T24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[6]	Input	100 kΩ pull-up
DISP0_DAT13	R20	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[7]	Input	100 kΩ pull-up
DISP0_DAT14	U25	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[8]	Input	100 kΩ pull-up
DISP0_DAT15	T22	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[9]	Input	100 kΩ pull-up
DISP0_DAT16	T21	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[10]	Input	100 kΩ pull-up
DISP0_DAT17	U24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[11]	Input	100 kΩ pull-up
DISP0_DAT18	V25	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[12]	Input	100 kΩ pull-up
DISP0_DAT19	U23	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[13]	Input	100 kΩ pull-up
DISP0_DAT2	P23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[23]	Input	100 kΩ pull-up
DISP0_DAT20	U22	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[14]	Input	100 kΩ pull-up
DISP0_DAT21	T20	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[15]	Input	100 kΩ pull-up
DISP0_DAT22	V24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[16]	Input	100 kΩ pull-up
DISP0_DAT23	W24	NVCC_LCD	GPIO	ALT5	gpio5.GPIO[17]	Input	100 kΩ pull-up

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Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DISP0_DAT3	P21	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[24]	Input	100 kΩ pull-up
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[25]	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[26]	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[27]	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[28]	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[29]	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	gpio4.GPIO[30]	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[0]	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[1]	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[10]	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[11]	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[12]	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[13]	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[14]	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[15]	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[2]	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[3]	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[4]	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[5]	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[6]	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[7]	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[8]	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_A[9]	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[0]	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_CS[1]	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[0]	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[1]	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[10]	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[11]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[12]	Input	100 kΩ pull-up
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[13]	Input	100 kΩ pull-up
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[14]	Input	100 kΩ pull-up
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[15]	Input	100 kΩ pull-up
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[16]	Input	100 kΩ pull-up
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[17]	Input	100 kΩ pull-up
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[18]	Input	100 kΩ pull-up
DRAM_D19	Y9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[19]	Input	100 kΩ pull-up
DRAM_D2	AC4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[2]	Input	100 kΩ pull-up
DRAM_D20	Y7	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[20]	Input	100 kΩ pull-up
DRAM_D21	Y8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[21]	Input	100 kΩ pull-up
DRAM_D22	AC8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[22]	Input	100 kΩ pull-up
DRAM_D23	AA9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[23]	Input	100 kΩ pull-up
DRAM_D24	AE9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[24]	Input	100 kΩ pull-up
DRAM_D25	Y10	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[25]	Input	100 kΩ pull-up
DRAM_D26	AE11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[26]	Input	100 kΩ pull-up
DRAM_D27	AB11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[27]	Input	100 kΩ pull-up
DRAM_D28	AC9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[28]	Input	100 kΩ pull-up
DRAM_D29	AD9	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[29]	Input	100 kΩ pull-up
DRAM_D3	AA5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[3]	Input	100 kΩ pull-up
DRAM_D30	AD11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[30]	Input	100 kΩ pull-up
DRAM_D31	AC11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[31]	Input	100 kΩ pull-up
DRAM_D32	AA17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[32]	Input	100 kΩ pull-up
DRAM_D33	AA18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[33]	Input	100 kΩ pull-up
DRAM_D34	AC18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[34]	Input	100 kΩ pull-up
DRAM_D35	AE19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[35]	Input	100 kΩ pull-up
DRAM_D36	Y17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[36]	Input	100 kΩ pull-up
DRAM_D37	Y18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[37]	Input	100 kΩ pull-up
DRAM_D38	AB19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[38]	Input	100 kΩ pull-up
DRAM_D39	AC19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[39]	Input	100 kΩ pull-up

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Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_D4	AC1	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[4]	Input	100 kΩ pull-up
DRAM_D40	Y19	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[40]	Input	100 kΩ pull-up
DRAM_D41	AB20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[41]	Input	100 kΩ pull-up
DRAM_D42	AB21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[42]	Input	100 kΩ pull-up
DRAM_D43	AD21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[43]	Input	100 kΩ pull-up
DRAM_D44	Y20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[44]	Input	100 kΩ pull-up
DRAM_D45	AA20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[45]	Input	100 kΩ pull-up
DRAM_D46	AE21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[46]	Input	100 kΩ pull-up
DRAM_D47	AC21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[47]	Input	100 kΩ pull-up
DRAM_D48	AC22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[48]	Input	100 kΩ pull-up
DRAM_D49	AE22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[49]	Input	100 kΩ pull-up
DRAM_D5	AD1	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[5]	Input	100 kΩ pull-up
DRAM_D50	AE24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[50]	Input	100 kΩ pull-up
DRAM_D51	AC24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[51]	Input	100 kΩ pull-up
DRAM_D52	AB22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[52]	Input	100 kΩ pull-up
DRAM_D53	AC23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[53]	Input	100 kΩ pull-up
DRAM_D54	AD25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[54]	Input	100 kΩ pull-up
DRAM_D55	AC25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[55]	Input	100 kΩ pull-up
DRAM_D56	AB25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[56]	Input	100 kΩ pull-up
DRAM_D57	AA21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[57]	Input	100 kΩ pull-up
DRAM_D58	Y25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[58]	Input	100 kΩ pull-up
DRAM_D59	Y22	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[59]	Input	100 kΩ pull-up
DRAM_D6	AB4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[6]	Input	100 kΩ pull-up
DRAM_D60	AB23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[60]	Input	100 kΩ pull-up
DRAM_D61	AA23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[61]	Input	100 kΩ pull-up
DRAM_D62	Y23	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[62]	Input	100 kΩ pull-up
DRAM_D63	W25	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[63]	Input	100 kΩ pull-up
DRAM_D7	AE4	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[7]	Input	100 kΩ pull-up
DRAM_D8	AD5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[8]	Input	100 kΩ pull-up
DRAM_D9	AE5	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_D[9]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_DQM0	AC3	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[0]	Output	Low
DRAM_DQM1	AC6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[1]	Output	Low
DRAM_DQM2	AB8	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[2]	Output	Low
DRAM_DQM3	AE10	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[3]	Output	Low
DRAM_DQM4	AB18	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[4]	Output	Low
DRAM_DQM5	AC20	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[5]	Output	Low
DRAM_DQM6	AD24	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[6]	Output	Low
DRAM_DQM7	Y21	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_DQM[7]	Output	Low
DRAM_RAS	AB15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_RAS	Output	Low
DRAM_RESET	Y6	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_RESET	Output	Low
DRAM_SDBA0	AC15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[0]	Output	Low
DRAM_SDBA1	Y15	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[1]	Output	Low
DRAM_SDBA2	AB12	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDBA[2]	Output	Low
DRAM_SDCKE0	Y11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDCKE[0]	Output	Low
DRAM_SDCKE1	AA11	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDCKE[1]	Output	Low
DRAM_SDCLK_0	AD15	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDCLK0	Output	Low
DRAM_SDCLK_0_B	AE15	NVCC_DRAM			DRAM_SDCLK_0_B	-	-
DRAM_SDCLK_1	AD14	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDCLK1	Output	Low
DRAM_SDCLK_1_B	AE14	NVCC_DRAM			DRAM_SDCLK_1_B	-	-
DRAM_SDOT0	AC16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_ODT[0]	Output	Low
DRAM_SDOT1	AB17	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_ODT[1]	Output	Low
DRAM_SDQS0	AE3	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[0]	Input	Hi-Z
DRAM_SDQS0_B	AD3	NVCC_DRAM			DRAM_SDQS0_B	-	-
DRAM_SDQS1	AD6	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[1]	Input	Hi-Z
DRAM_SDQS1_B	AE6	NVCC_DRAM			DRAM_SDQS1_B	-	-
DRAM_SDQS2	AD8	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[2]	Input	Hi-Z
DRAM_SDQS2_B	AE8	NVCC_DRAM			DRAM_SDQS2_B	-	-
DRAM_SDQS3	AC10	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[3]	Input	Hi-Z
DRAM_SDQS3_B	AB10	NVCC_DRAM			DRAM_SDQS3_B	-	-
DRAM_SDQS4	AD18	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[4]	Input	Hi-Z

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
DRAM_SDQS4_B	AE18	NVCC_DRAM			DRAM_SDQS4_B	-	-
DRAM_SDQS5	AD20	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[5]	Input	Hi-Z
DRAM_SDQS5_B	AE20	NVCC_DRAM			DRAM_SDQS5_B	-	-
DRAM_SDQS6	AD23	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[6]	Input	Hi-Z
DRAM_SDQS6_B	AE23	NVCC_DRAM			DRAM_SDQS6_B	-	-
DRAM_SDQS7	AA25	NVCC_DRAM	DDRCLK	ALT0	mmdc.DRAM_SDQS[7]	Input	Hi-Z
DRAM_SDQS7_B	AA24	NVCC_DRAM			DRAM_SDQS7_B	-	-
DRAM_SDWE	AB16	NVCC_DRAM	DDR	ALT0	mmdc.DRAM_SDWE	Output	Low
DSI_CLK0M	H3	NVCC_MIPI	ANALOG				
DSI_CLK0P	H4	NVCC_MIPI	ANALOG				
DSI_D0M	G2	NVCC_MIPI	ANALOG				
DSI_D0P	G1	NVCC_MIPI	ANALOG				
DSI_D1M	H2	NVCC_MIPI	ANALOG				
DSI_D1P	H1	NVCC_MIPI	ANALOG				
EIM_A16	H25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[16]	Output	Low
EIM_A17	G24	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[17]	Output	Low
EIM_A18	J22	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[18]	Output	Low
EIM_A19	G25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[19]	Output	Low
EIM_A20	H22	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[20]	Output	Low
EIM_A21	H23	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[21]	Output	Low
EIM_A22	F24	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[22]	Output	Low
EIM_A23	J21	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[23]	Output	Low
EIM_A24	F25	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[24]	Output	Low
EIM_A25	H19	NVCC_EIM	GPIO	ALT0	weim.WEIM_A[25]	Output	Low
EIM_BCLK	N22	NVCC_EIM	GPIO	ALT0	weim.WEIM_BCLK	Output	Low
EIM_CS0	H24	NVCC_EIM	GPIO	ALT0	weim.WEIM_CS[0]	Output	High
EIM_CS1	J23	NVCC_EIM	GPIO	ALT0	weim.WEIM_CS[1]	Output	High
EIM_D16	C25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[16]	Input	100 kΩ pull-up
EIM_D17	F21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[17]	Input	100 kΩ pull-up
EIM_D18	D24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[18]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EIM_D19	G21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[19]	Input	100 kΩ pull-up
EIM_D20	G20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[20]	Input	100 kΩ pull-up
EIM_D21	H20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[21]	Input	100 kΩ pull-up
EIM_D22	E23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[22]	Input	100 kΩ pull-down
EIM_D23	D25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[23]	Input	100 kΩ pull-up
EIM_D24	F22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[24]	Input	100 kΩ pull-up
EIM_D25	G22	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[25]	Input	100 kΩ pull-up
EIM_D26	E24	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[26]	Input	100 kΩ pull-up
EIM_D27	E25	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[27]	Input	100 kΩ pull-up
EIM_D28	G23	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[28]	Input	100 kΩ pull-up
EIM_D29	J19	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[29]	Input	100 kΩ pull-up
EIM_D30	J20	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[30]	Input	100 kΩ pull-up
EIM_D31	H21	NVCC_EIM	GPIO	ALT5	gpio3.GPIO[31]	Input	100 kΩ pull-down
EIM_DA0	L20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[0]	Input	100 kΩ pull-up
EIM_DA1	J25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[1]	Input	100 kΩ pull-up
EIM_DA10	M22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[10]	Input	100 kΩ pull-up
EIM_DA11	M20	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[11]	Input	100 kΩ pull-up
EIM_DA12	M24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[12]	Input	100 kΩ pull-up
EIM_DA13	M23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[13]	Input	100 kΩ pull-up
EIM_DA14	N23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[14]	Input	100 kΩ pull-up
EIM_DA15	N24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[15]	Input	100 kΩ pull-up
EIM_DA2	L21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[2]	Input	100 kΩ pull-up
EIM_DA3	K24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[3]	Input	100 kΩ pull-up
EIM_DA4	L22	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[4]	Input	100 kΩ pull-up
EIM_DA5	L23	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[5]	Input	100 kΩ pull-up
EIM_DA6	K25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[6]	Input	100 kΩ pull-up
EIM_DA7	L25	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[7]	Input	100 kΩ pull-up
EIM_DA8	L24	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[8]	Input	100 kΩ pull-up
EIM_DA9	M21	NVCC_EIM	GPIO	ALT0	weim.WEIM_DA_A[9]	Input	100 kΩ pull-up
EIM_EB0	K21	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[0]	Output	High

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
EIM_EB1	K23	NVCC_EIM	GPIO	ALT0	weim.WEIM_EB[1]	Output	High
EIM_EB2	E22	NVCC_EIM	GPIO	ALT5	gpio2.GPIO[30]	Input	100 kΩ pull-up
EIM_EB3	F23	NVCC_EIM	GPIO	ALT5	gpio2.GPIO[31]	Input	100 kΩ pull-up
EIM_LBA	K22	NVCC_EIM	GPIO	ALT0	weim.WEIM_LBA	Output	High
EIM_OE	J24	NVCC_EIM	GPIO	ALT0	weim.WEIM_OE	Output	High
EIM_RW	K20	NVCC_EIM	GPIO	ALT0	weim.WEIM_RW	Output	High
EIM_WAIT	M25	NVCC_EIM	GPIO	ALT0	weim.WEIM_WAIT	Input	100 kΩ pull-up
ENET_CRS_DV	U21	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[25]	Input	100 kΩ pull-up
ENET_MDC	V20	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[31]	Input	100 kΩ pull-up
ENET_MDIO	V23	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[22]	Input	100 kΩ pull-up
ENET_REF_CLK	V22	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[23]	Input	100 kΩ pull-up
ENET_RX_ER	W23	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[24]	Input	100 kΩ pull-up
ENET_RXD0	W21	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[27]	Input	100 kΩ pull-up
ENET_RXD1	W22	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[26]	Input	100 kΩ pull-up
ENET_TX_EN	V21	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[28]	Input	100 kΩ pull-up
ENET_TXD0	U20	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[30]	Input	100 kΩ pull-up
ENET_TXD1	W20	NVCC_ENET	GPIO	ALT5	gpio1.GPIO[29]	Input	100 kΩ pull-up
GPIO_0	T5	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[0]	Input	100 kΩ pull-down
GPIO_1	T4	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[1]	Input	100 kΩ pull-up
GPIO_16	R2	NVCC_GPIO	GPIO	ALT5	gpio7.GPIO[11]	Input	100 kΩ pull-up
GPIO_17	R1	NVCC_GPIO	GPIO	ALT5	gpio7.GPIO[12]	Input	100 kΩ pull-up
GPIO_18	P6	NVCC_GPIO	GPIO	ALT5	gpio7.GPIO[13]	Input	100 kΩ pull-up
GPIO_19	P5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[5]	Input	100 kΩ pull-up
GPIO_2	T1	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[2]	Input	100 kΩ pull-up
GPIO_3	R7	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[3]	Input	100 kΩ pull-up
GPIO_4	R6	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[4]	Input	100 kΩ pull-up
GPIO_5	R4	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[5]	Input	100 kΩ pull-up
GPIO_6	T3	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[6]	Input	100 kΩ pull-up
GPIO_7	R3	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[7]	Input	100 kΩ pull-up
GPIO_8	R5	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[8]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
GPIO_9	T2	NVCC_GPIO	GPIO	ALT5	gpio1.GPIO[9]	Input	100 kΩ pull-up
HDMI_CLKM	J5	HDMI					
HDMI_CLKP	J6	HDMI					
HDMI_D0M	K5	HDMI					
HDMI_D0P	K6	HDMI					
HDMI_D1M	J3	HDMI					
HDMI_D1P	J4	HDMI					
HDMI_D2M	K3	HDMI					
HDMI_D2P	K4	HDMI					
HDMI_HPDP	K1	HDMI					
JTAG_MOD	H6	NVCC_JTAG	GPIO	ALT0	sjc.MOD	Input	100 kΩ pull-up
JTAG_TCK	H5	NVCC_JTAG	GPIO	ALT0	sjc.TCK	Input	47 kΩ pull-up
JTAG_TDI	G5	NVCC_JTAG	GPIO	ALT0	sjc.TDI	Input	47 kΩ pull-up
JTAG_TDO	G6	NVCC_JTAG	GPIO	ALT0	sjc.TDO	Output	Low
JTAG_TMS	C3	NVCC_JTAG	GPIO	ALT0	sjc.TMS	Input	47 kΩ pull-up
JTAG_TRSTB	C2	NVCC_JTAG	GPIO	ALT0	sjc.TRSTB	Input	47 kΩ pull-up
KEY_COL0	W5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[6]	Input	100 kΩ pull-up
KEY_COL1	U7	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[8]	Input	100 kΩ pull-up
KEY_COL2	W6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[10]	Input	100 kΩ pull-up
KEY_COL3	U5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[12]	Input	100 kΩ pull-up
KEY_COL4	T6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[14]	Input	100 kΩ pull-up
KEY_ROW0	V6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[7]	Input	100 kΩ pull-up
KEY_ROW1	U6	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[9]	Input	100 kΩ pull-up
KEY_ROW2	W4	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[11]	Input	100 kΩ pull-up
KEY_ROW3	T7	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[13]	Input	100 kΩ pull-up
KEY_ROW4	V5	NVCC_GPIO	GPIO	ALT5	gpio4.GPIO[15]	Input	100 kΩ pull-down
LVDS0_CLK_N	V4	NVCC_LVDS2P5					
LVDS0_CLK_P	V3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_CLK	Input	Keeper
LVDS0_TX0_N	U2	NVCC_LVDS2P5					
LVDS0_TX0_P	U1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX0	Input	Keeper

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
LVDS0_TX1_N	U4	NVCC_LVDS2P5					
LVDS0_TX1_P	U3	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX1	Input	Keeper
LVDS0_TX2_N	V2	NVCC_LVDS2P5					
LVDS0_TX2_P	V1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX2	Input	Keeper
LVDS0_TX3_N	W2	NVCC_LVDS2P5					
LVDS0_TX3_P	W1	NVCC_LVDS2P5		ALT0	ldb.LVDS0_TX3	Input	Keeper
LVDS1_CLK_N	Y3	NVCC_LVDS2P5					
LVDS1_CLK_P	Y4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_CLK	Input	Keeper
LVDS1_TX0_N	Y1	NVCC_LVDS2P5					
LVDS1_TX0_P	Y2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX0	Input	Keeper
LVDS1_TX1_N	AA2	NVCC_LVDS2P5					
LVDS1_TX1_P	AA1	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX1	Input	Keeper
LVDS1_TX2_N	AB1	NVCC_LVDS2P5					
LVDS1_TX2_P	AB2	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX2	Input	Keeper
LVDS1_TX3_N	AA3	NVCC_LVDS2P5					
LVDS1_TX3_P	AA4	NVCC_LVDS2P5		ALT0	ldb.LVDS1_TX3	Input	Keeper
MLB_CN	A11	VDDHIGH_CAP					
MLB_CP	B11	VDDHIGH_CAP					
MLB_DN	B10	VDDHIGH_CAP					
MLB_DP	A10	VDDHIGH_CAP					
MLB_SN	A9	VDDHIGH_CAP					
MLB_SP	B9	VDDHIGH_CAP					
NANDF_ALE	A16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[8]	Input	100 kΩ pull-up
NANDF_CLE	C15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[7]	Input	100 kΩ pull-up
NANDF_CS0	F15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[11]	Input	100 kΩ pull-up
NANDF_CS1	C16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[14]	Input	100 kΩ pull-up
NANDF_CS2	A17	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[15]	Input	100 kΩ pull-up
NANDF_CS3	D16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[16]	Input	100 kΩ pull-up
NANDF_D0	A18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[0]	Input	100 kΩ pull-up
NANDF_D1	C17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[1]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
NANDF_D2	F16	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[2]	Input	100 kΩ pull-up
NANDF_D3	D17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[3]	Input	100 kΩ pull-up
NANDF_D4	A19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[4]	Input	100 kΩ pull-up
NANDF_D5	B18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[5]	Input	100 kΩ pull-up
NANDF_D6	E17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[6]	Input	100 kΩ pull-up
NANDF_D7	C18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[7]	Input	100 kΩ pull-up
NANDF_RB0	B16	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[10]	Input	100 kΩ pull-up
NANDF_WP_B	E15	NVCC_NANDF	GPIO	ALT5	gpio6.GPIO[9]	Input	100 kΩ pull-up
ONOFF	D12	VDD_SNVS_IN	GPIO	ALT0	src.RESET_B	Input	100 kΩ pull-up
PCIE_RXM	B1	PCIE_VPH					
PCIE_RXP	B2	PCIE_VPH					
PCIE_TXM	A3	PCIE_VPH					
PCIE_TXP	B3	PCIE_VPH					
PMIC_ON_REQ	D11	VDD_SNVS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVS_WAKEUP_ALARM	Output	Low
PMIC_STBY_REQ	F11	VDD_SNVS_IN	GPIO	ALT0	ccm.PMIC_VSTBY_REQ	Output	Low
POR_B	C11	VDD_SNVS_IN	GPIO	ALT0	src.POR_B	Input	100 kΩ pull-up
RGMII_RD0	C24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[25]	Input	100 kΩ pull-up
RGMII_RD1	B23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[27]	Input	100 kΩ pull-up
RGMII_RD2	B24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[28]	Input	100 kΩ pull-up
RGMII_RD3	D23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[29]	Input	100 kΩ pull-up
RGMII_RX_CTL	D22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[24]	Input	100 kΩ pull-down
RGMII_RXC	B25	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[30]	Input	100 kΩ pull-down
RGMII_TD0	C22	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[20]	Input	100 kΩ pull-up
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[21]	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[22]	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[23]	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[26]	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	gpio6.GPIO[19]	Input	100 kΩ pull-down

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
RTC_XTALI	D9	VDD_SNV5_CAP					
RTC_XTALO	C9	VDD_SNV5_CAP					
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[20]	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[18]	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[16]	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[17]	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[19]	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	gpio1.GPIO[21]	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[10]	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[11]	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[15]	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[14]	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[13]	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	gpio1.GPIO[12]	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[3]	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[2]	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[4]	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[5]	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[6]	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[7]	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[1]	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[0]	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[18]	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	gpio6.GPIO[17]	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	gpio7.GPIO[8]	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[10]	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	gpio7.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[8]	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[9]	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[10]	Input	100 kΩ pull-up

Table 101. 21 x 21 mm Functional Contact Assignments¹ (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition ²			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[11]	Input	100 kΩ pull-up
SD4_DAT4	E18	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[12]	Input	100 kΩ pull-up
SD4_DAT5	C19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[13]	Input	100 kΩ pull-up
SD4_DAT6	B20	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[14]	Input	100 kΩ pull-up
SD4_DAT7	D19	NVCC_NANDF	GPIO	ALT5	gpio2.GPIO[15]	Input	100 kΩ pull-up
TAMPER	E11	VDD_SNVIS_IN	GPIO	ALT0	snvs_lp_wrapper.SNVIS_TD1	Input	100 kΩ pull-down
TEST_MODE	E12	VDD_SNVIS_IN	GPIO	ALT0	tcu.TEST_MODE	Input	100 kΩ pull-down
USB_H1_DN	F10	VDDUSB_CAP					
USB_H1_DP	E10	VDDUSB_CAP					
USB_OTG_CHD_B	B8	VDDUSB_CAP					
USB_OTG_DN	B6	VDDUSB_CAP					
USB_OTG_DP	A6	VDDUSB_CAP					
XTALI	A7	NVCC_PLL_OUT					
XTALO	B7	NVCC_PLL_OUT					
NC	A1						
NC	A12						
NC	A14						
NC	B12						
NC	B14						
NC	E1						
NC	E2						
NC	F1						
NC	F2						

¹ DRAM_D32 to DRAM_D63 are only available for i.MX 6DualLite chip; for i.MX 6Solo chip, these pins are NC.

² The state immediately after reset and before ROM firmware or software has executed.

6.1.3 21 x 21 mm, 0.8 mm Pitch Ball Map

Table 102 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6Solo.

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map

G	F	E	D	C	B	A
DSI_D0P	NC	NC	CSI_D1M	GND	PCIE_RXM	NC
DSI_D0M	NC	NC	CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT
GND	CSI_CLK0P	CSI_D0P	GND	JTAG_TMS	PCIE_TXP	PCIE_TXM
DSI_REXT	CSI_CLK0M	CSI_D0M	CSI_REXT	GND	GND	GND
JTAG_TDI	GND	GND	CLK2_P	CLK2_N	VDD_FA	FA_ANA
JTAG_TDO	GND	GND	GND	GND	USB_OTG_DN	USB_OTG_DP
PCIE_VPH	GND	GND	CLK1_P	CLK1_N	XTALO	XTALI
PCIE_VPTX	GND	NVCC_PLL_OUT	GND	GPANAIO	USB_OTG_CHD_B	GND
VDD_SNV5_CAP	VDDUSB_CAP	USB_OTG_VBUS	RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN
GND	USB_H1_DN	USB_H1_DP	USB_H1_VBUS	GND	MLB_DN	MLB_DP
VDD_SNV5_IN	PMIC_STBY_REQ	TAMPER	PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN
NC	BOOT_MODE1	TEST_MODE	ONOFF	BOOT_MODE0	NC	NC
NC	SD3_DAT7	SD3_DAT6	SD3_DAT4	SD3_DAT5	SD3_CMD	GND
NVCC_SD3	SD3_DAT1	SD3_DAT0	SD3_CLK	NC	NC	NC
NVCC_NANDF	NANDF_CS0	NANDF_WP_B	SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2
NVCC_SD1	NANDF_D2	SD4_CLK	NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE
NVCC_SD2	SD4_DAT2	NANDF_D6	NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2
NVCC_RGMII	SD1_DAT3	SD4_DAT4	SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0
GND	SD2_CMD	SD1_DAT2	SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4
EIM_D20	RGMII_TD1	SD2_DAT1	SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3
EIM_D19	EIM_D17	RGMII_TD2	RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0
EIM_D25	EIM_D24	EIM_EB2	RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0
EIM_D28	EIM_EB3	EIM_D22	RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2
EIM_A17	EIM_A22	EIM_D26	EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3
EIM_A19	EIM_A24	EIM_D27	EIM_D23	EIM_D16	RGMII_RXC	GND
G	F	E	D	C	B	A

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

R	P	N	M	L	K	J	H
GPIO_17	CSIO_PIXCLK	CSIO_DAT4	CSIO_DAT10	CSIO_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P
GPIO_16	CSIO_DAT5	CSIO_VSYNC	CSIO_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M
GPIO_7	CSIO_DATA_EN	CSIO_DAT7	CSIO_DAT11	CSIO_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M
GPIO_5	CSIO_MCLK	CSIO_DAT6	CSIO_DAT14	CSIO_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P
GPIO_8	GPIO_19	CSIO_DAT9	CSIO_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK
GPIO_4	GPIO_18	CSIO_DAT8	CSIO_DAT18	CSIO_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD
GPIO_3	NVCC_GPIO	NVCC_CSI	HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP
GND	GND	GND	GND	GND	GND	GND	GND
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN
VDDSOC_CAP	GND	GND	GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
GND	GND	NC	GND	GND	GND	GND	GND
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
GND	GND	GND	GND	GND	GND	GND	GND
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
GND	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP
NVCC_DRAM	GND	GND	GND	GND	GND	GND	GND
NVCC_ENET	NVCC_LCD	DIO_DISP_CLK	NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25
DISP0_DAT13	DISP0_DAT4	DIO_PIN3	EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21
DISP0_DAT10	DISP0_DAT3	DIO_PIN15	EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31
DISP0_DAT8	DISP0_DAT1	EIM_BCLK	EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20
DISP0_DAT6	DISP0_DAT2	EIM_DA14	EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21
DISP0_DAT7	DISP0_DAT0	EIM_DA15	EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0
DISP0_DAT5	DIO_PIN4	DIO_PIN2	EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16
R	P	N	M	L	K	J	H

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

AC	AB	AA	Y	W	V	U	T
DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P	LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2
DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N	LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9
DRAM_DQM0	GND	LVDS1_TX3_N	LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6
DRAM_D2	DRAM_D6	LVDS1_TX3_P	LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1
DRAM_D13	DRAM_D12	DRAM_D3	GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0
DRAM_DQM1	DRAM_D14	DRAM_D10	DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4
DRAM_D15	DRAM_D16	GND	DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3
DRAM_D22	DRAM_DQM2	DRAM_D17	DRAM_D21	GND	GND	GND	GND
DRAM_D28	DRAM_D18	DRAM_D23	DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN
DRAM_SDQS3	DRAM_SDQS3_B	GND	DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_D31	DRAM_D27	DRAM_SDCKE1	DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND
DRAM_A11	DRAM_SDBA2	DRAM_A14	DRAM_A15	GND	NVCC_DRAM	GND	GND
DRAM_A6	DRAM_A8	GND	DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_A0	DRAM_A1	DRAM_A2	DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP
DRAM_SDBA0	DRAM_RAS	DRAM_A10	DRAM_SDBA1	GND	NVCC_DRAM	GND	GND
DRAM_SDODT0	DRAM_SDWE	GND	DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN
DRAM_A13	DRAM_SDODT1	NC	NC	GND	NVCC_DRAM	GND	GND
NC	NC	NC	NC	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM
NC	NC	GND	NC	GND	GND	GND	GND
NC	NC	NC	NC	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21
NC	NC	NC	NC	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16
NC	NC	GND	NC	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15
NC	NC	NC	NC	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11
NC	GND	NC	GND	DISP0_DAT23	DISP0_DAT22	DISP0_DAT17	DISP0_DAT12
NC	NC	NC	NC	NC	DISP0_DAT18	DISP0_DAT14	DISP0_DAT9
AC	AB	AA	Y	W	V	U	T

Table 102. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD
1	GND	DRAM_D5
2	DRAM_D1	DRAM_D0
3	DRAM_SDQS0	DRAM_SDQS0_B
4	DRAM_D7	GND
5	DRAM_D9	DRAM_D8
6	DRAM_SDQS1_B	DRAM_SDQS1
7	DRAM_D11	GND
8	DRAM_SDQS2_B	DRAM_SDQS2
9	DRAM_D24	DRAM_D29
10	DRAM_DQM3	GND
11	DRAM_D26	DRAM_D30
12	DRAM_A9	DRAM_A12
13	DRAM_A5	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0
16	DRAM_CAS	GND
17	ZQPAD	DRAM_CS1
18	NC	NC
19	NC	GND
20	NC	NC
21	NC	NC
22	NC	GND
23	NC	NC
24	NC	NC
25	GND	NC
	AE	AD

Table 103 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map

D	C	B	A
CSI_D1M	GND	PCIE_RXM	NC
CSI_D1P	JTAG_TRSTB	PCIE_RXP	PCIE_REXT
GND	JTAG_TMS	PCIE_TXP	PCIE_TXM
CSI_REXT	GND	GND	GND
CLK2_P	CLK2_N	VDD_FA	FA_ANA
GND	GND	USB_OTG_DN	USB_OTG_DP
CLK1_P	CLK1_N	XTALO	XTALI
GND	GPANAIO	USB_OTG_CHD_B	GND
RTC_XTALI	RTC_XTALO	MLB_SP	MLB_SN
USB_H1_VBUS	GND	MLB_DN	MLB_DP
PMIC_ON_REQ	POR_B	MLB_CP	MLB_CN
ONOFF	BOOT_MODE0	NC	NC
SD3_DAT4	SD3_DAT5	SD3_CMD	GND
SD3_CLK	NC	NC	NC
SD3_RST	NANDF_CLE	SD3_DAT3	SD3_DAT2
NANDF_CS3	NANDF_CS1	NANDF_RB0	NANDF_ALE
NANDF_D3	NANDF_D1	SD4_CMD	NANDF_CS2
SD4_DAT0	NANDF_D7	NANDF_D5	NANDF_D0
SD4_DAT7	SD4_DAT5	SD4_DAT1	NANDF_D4
SD1_CLK	SD1_DAT1	SD4_DAT6	SD4_DAT3
RGMII_TXC	SD2_CLK	SD1_CMD	SD1_DAT0
RGMII_RX_CTL	RGMII_TD0	SD2_DAT3	SD2_DAT0
RGMII_RD3	RGMII_TX_CTL	RGMII_RD1	SD2_DAT2
EIM_D18	RGMII_RD0	RGMII_RD2	RGMII_TD3
EIM_D23	EIM_D16	RGMII_RXC	GND
D	C	B	A

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

M	L	K	J	H	G	F	E
CSIO_DAT10	CSIO_DAT13	HDMI_HPD	HDMI_REF	DSI_D1P	DSI_D0P	NC	NC
CSIO_DAT12	GND	HDMI_DDCCEC	GND	DSI_D1M	DSI_D0M	NC	NC
CSIO_DAT11	CSIO_DAT17	HDMI_D2M	HDMI_D1M	DSI_CLK0M	GND	CSI_CLK0P	CSI_D0P
CSIO_DAT14	CSIO_DAT16	HDMI_D2P	HDMI_D1P	DSI_CLK0P	DSI_REXT	CSI_CLK0M	CSI_D0M
CSIO_DAT15	GND	HDMI_D0M	HDMI_CLKM	JTAG_TCK	JTAG_TDI	GND	GND
CSIO_DAT18	CSIO_DAT19	HDMI_D0P	HDMI_CLKP	JTAG_MOD	JTAG_TDO	GND	GND
HDMI_VPH	HDMI_VP	NVCC_MIPI	NVCC_JTAG	PCIE_VP	PCIE_VPH	GND	GND
GND	GND	GND	GND	GND	PCIE_VPTX	GND	NVCC_PLL_OUT
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDHIGH_IN	VDDHIGH_IN	VDD_SNV5_CAP	VDDUSB_CAP	USB_OTG_VBUS
GND	GND	GND	VDDHIGH_CAP	VDDHIGH_CAP	GND	USB_H1_DN	USB_H1_DP
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDD_SNV5_IN	PMIC_STBY_REQ	TAMPER
GND	GND	GND	GND	GND	NC	BOOT_MODE1	TEST_MODE
VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP	NC	SD3_DAT7	SD3_DAT6
VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	NVCC_SD3	SD3_DAT1	SD3_DAT0
GND	GND	GND	GND	GND	NVCC_NANDF	NANDF_CS0	NANDF_WP_B
VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	NVCC_SD1	NANDF_D2	SD4_CLK
VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	VDDPU_CAP	NVCC_SD2	SD4_DAT2	NANDF_D6
GND	GND	GND	GND	GND	NVCC_RGMII	SD1_DAT3	SD4_DAT4
NVCC_EIM	NVCC_EIM	NVCC_EIM	EIM_D29	EIM_A25	GND	SD2_CMD	SD1_DAT2
EIM_DA11	EIM_DA0	EIM_RW	EIM_D30	EIM_D21	EIM_D20	RGMII_TD1	SD2_DAT1
EIM_DA9	EIM_DA2	EIM_EB0	EIM_A23	EIM_D31	EIM_D19	EIM_D17	RGMII_TD2
EIM_DA10	EIM_DA4	EIM_LBA	EIM_A18	EIM_A20	EIM_D25	EIM_D24	EIM_EB2
EIM_DA13	EIM_DA5	EIM_EB1	EIM_CS1	EIM_A21	EIM_D28	EIM_EB3	EIM_D22
EIM_DA12	EIM_DA8	EIM_DA3	EIM_OE	EIM_CS0	EIM_A17	EIM_A22	EIM_D26
EIM_WAIT	EIM_DA7	EIM_DA6	EIM_DA1	EIM_A16	EIM_A19	EIM_A24	EIM_D27
M	L	K	J	H	G	F	E

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

Y	W	V	U	T	R	P	N
LVDS1_TX0_N	LVDS0_TX3_P	LVDS0_TX2_P	LVDS0_TX0_P	GPIO_2	GPIO_17	CSIO_PIXCLK	CSIO_DATA4
LVDS1_TX0_P	LVDS0_TX3_N	LVDS0_TX2_N	LVDS0_TX0_N	GPIO_9	GPIO_16	CSIO_DATA5	CSIO_VSYNC
LVDS1_CLK_N	GND	LVDS0_CLK_P	LVDS0_TX1_P	GPIO_6	GPIO_7	CSIO_DATA_EN	CSIO_DATA7
LVDS1_CLK_P	KEY_ROW2	LVDS0_CLK_N	LVDS0_TX1_N	GPIO_1	GPIO_5	CSIO_MCLK	CSIO_DATA6
GND	KEY_COL0	KEY_ROW4	KEY_COL3	GPIO_0	GPIO_8	GPIO_19	CSIO_DATA9
DRAM_RESET	KEY_COL2	KEY_ROW0	KEY_ROW1	KEY_COL4	GPIO_4	GPIO_18	CSIO_DATA8
DRAM_D20	GND	NVCC_LVDS2P5	KEY_COL1	KEY_ROW3	GPIO_3	NVCC_GPIO	NVCC_CSI
DRAM_D21	GND	GND	GND	GND	GND	GND	GND
DRAM_D19	GND	NVCC_DRAM	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_D25	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDSOC_CAP	GND	GND
DRAM_SDCKE0	GND	NVCC_DRAM	GND	GND	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A15	GND	NVCC_DRAM	GND	GND	GND	GND	NC
DRAM_A7	GND	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_CAP	VDDARM_CAP	VDDARM_CAP
DRAM_A3	DRAM_A4	NVCC_DRAM	VDDSOC_CAP	VDDSOC_CAP	VDDARM_IN	VDDARM_IN	VDDARM_IN
DRAM_SDBA1	GND	NVCC_DRAM	GND	GND	GND	GND	GND
DRAM_CS0	GND	NVCC_DRAM	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN	VDDSOC_IN
DRAM_D36	GND	NVCC_DRAM	GND	GND	GND	VDDPU_CAP	VDDPU_CAP
DRAM_D37	GND	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	NVCC_DRAM	GND	GND
DRAM_D40	GND	GND	GND	GND	NVCC_ENET	NVCC_LCD	DIO_DISP_CLK
DRAM_D44	ENET_TXD1	ENET_MDC	ENET_TXD0	DISP0_DAT21	DISP0_DAT13	DISP0_DATA4	DIO_PIN3
DRAM_DQM7	ENET_RXD0	ENET_TX_EN	ENET_CRS_DV	DISP0_DAT16	DISP0_DAT10	DISP0_DATA3	DIO_PIN15
DRAM_D59	ENET_RXD1	ENET_REF_CLK	DISP0_DAT20	DISP0_DAT15	DISP0_DATA8	DISP0_DATA1	EIM_BCLK
DRAM_D62	ENET_RX_ER	ENET_MDIO	DISP0_DAT19	DISP0_DAT11	DISP0_DATA6	DISP0_DATA2	EIM_DA14
GND	DISP0_DATA23	DISP0_DATA22	DISP0_DATA17	DISP0_DATA12	DISP0_DATA7	DISP0_DATA0	EIM_DA15
DRAM_D58	DRAM_D63	DISP0_DATA18	DISP0_DATA14	DISP0_DATA9	DISP0_DATA5	DIO_PIN4	DIO_PIN2
Y	W	V	U	T	R	P	N

Table 103. 21 x 21 mm, 0.8 mm Pitch Ball Map (continued)

	AE	AD	AC	AB	AA
1	GND	DRAM_D5	DRAM_D4	LVDS1_TX2_N	LVDS1_TX1_P
2	DRAM_D1	DRAM_D0	DRAM_VREF	LVDS1_TX2_P	LVDS1_TX1_N
3	DRAM_SDQS0	DRAM_SDQS0_B	DRAM_DQM0	GND	LVDS1_TX3_N
4	DRAM_D7	GND	DRAM_D2	DRAM_D6	LVDS1_TX3_P
5	DRAM_D9	DRAM_D8	DRAM_D13	DRAM_D12	DRAM_D3
6	DRAM_SDQS1_B	DRAM_SDQS1	DRAM_DQM1	DRAM_D14	DRAM_D10
7	DRAM_D11	GND	DRAM_D15	DRAM_D16	GND
8	DRAM_SDQS2_B	DRAM_SDQS2	DRAM_D22	DRAM_DQM2	DRAM_D17
9	DRAM_D24	DRAM_D29	DRAM_D28	DRAM_D18	DRAM_D23
10	DRAM_DQM3	GND	DRAM_SDQS3	DRAM_SDQS3_B	GND
11	DRAM_D26	DRAM_D30	DRAM_D31	DRAM_D27	DRAM_SDCKE1
12	DRAM_A9	DRAM_A12	DRAM_A11	DRAM_SDBA2	DRAM_A14
13	DRAM_A5	GND	DRAM_A6	DRAM_A8	GND
14	DRAM_SDCLK_1_B	DRAM_SDCLK_1	DRAM_A0	DRAM_A1	DRAM_A2
15	DRAM_SDCLK_0_B	DRAM_SDCLK_0	DRAM_SDBA0	DRAM_RAS	DRAM_A10
16	DRAM_CAS	GND	DRAM_SDODT0	DRAM_SDWE	GND
17	ZQPAD	DRAM_CS1	DRAM_A13	DRAM_SDODT1	DRAM_D32
18	DRAM_SDQS4_B	DRAM_SDQS4	DRAM_D34	DRAM_DQM4	DRAM_D33
19	DRAM_D35	GND	DRAM_D39	DRAM_D38	GND
20	DRAM_SDQS5_B	DRAM_SDQS5	DRAM_DQM5	DRAM_D41	DRAM_D45
21	DRAM_D46	DRAM_D43	DRAM_D47	DRAM_D42	DRAM_D57
22	DRAM_D49	GND	DRAM_D48	DRAM_D52	GND
23	DRAM_SDQS6_B	DRAM_SDQS6	DRAM_D53	DRAM_D60	DRAM_D61
24	DRAM_D50	DRAM_DQM6	DRAM_D51	GND	DRAM_SDQS7_B
25	GND	DRAM_D54	DRAM_D55	DRAM_D56	DRAM_SDQS7
	AE	AD	AC	AB	AA

7 Revision History

Table 104 provides a revision history for this datasheet.

Table 104. i.MX 6Solo/6DualLite Datasheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 1	11/2012	<ul style="list-style-type: none"> • Updated Table 1, "Orderable Part Numbers," on page 3. • Updated Figure 1, "Part Number Nomenclature—i.MX 6DualLite and 6Solo," on page 4. • In Section 1.2, "Features," added a footnote on the bottom of page 6 to specify performance limitation of 1 Gbps ENET. • In Table 7, "Absolute Maximum Ratings," on page 22, added details of VDD_SNVS_IN parameter. • Updated Table 9, "Operating Ranges," on page 24. • In Table 10, "On-Chip LDOs and their On-Chip Loads," on page 25, removed VDD_CACHE_CAP load. • Updated Table 12, "Maximal Supply Currents," on page 27. • Updated Table 15, "PCIe PHY Current Drain," on page 30. • Updated Table 16, "HDMI PHY Current Drain," on page 31. • In Table 23, "OSC32K Main Characteristics," on page 36, added 100 kΩ as ESR parameter max value. • Updated Table 27, "LVDS I/O DC Characteristics," on page 41. • In Table 42, "EIM Internal Module Multiplexing," on page 51, Multiplexed Address/Data mode, 16 Bit column, changed DSZ value to "001." • In Table 54, "ECSPI Master Mode Timing Parameters," on page 78, updated CS5 and CS6 min values. • Updated Table 64, "RMII Signal Timing," on page 91. • Updated Section 4.11.5.3, "RGMIISignal Switching Specifications." • Updated Section 4.11.6, "Flexible Controller Area Network (FLEXCAN) AC Electrical Specifications." • Updated Table 64, "RMII Signal Timing," on page 91. • In Table 76, "Electrical and Timing Information," on page 116, updated $\Delta V_{\text{CMTX(LF)}}$ max value. • Updated Figure 88, "PWM Timing," on page 127. • Updated Table 83, "PWM Output Timing Parameters," on page 127. • Updated Section 4.11.22, "USB PHY Parameters."
Rev. 0	10/2012	Initial public release.

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