HALIOS® MULTI-PURPOSE OPTICAL SENSOR WITH HIGH LIGHT IMMUNITY E909.05

PRELIMINARY DATA SHEET - AUG 02, 2011

RoHS compliant

Features

- Up to 4 emitters and 1 compensator
- Automatic calibration of all relevant values
- Optical principle with no mechanics
- SPI and I²C communication interfaces available
- 16bit microcontroller with 8MHz clock
- 32kByte Flash and 3kByte SRAM memory
- 50µA standby current
- 2.5mA circuit operating current
- Supply voltage range
  Core 2.25V to 2.75V / IO 1.50V to 2.8V

Applications

- Highly intuitive input devices (e.g. handheld devices, HMI steering wheel, 3D MMIs, etc.)
- In combination with suitable optics and additional software, resolves real x, y, z coordinates
  (64 x 64 x 16 positions)
- Navigation keys, rotary switches, sliders, proximity sensors and optical switches
- Multi-key applications for rough environmental conditions
- Long range (up to 3m) proximity & motion detection

General Description

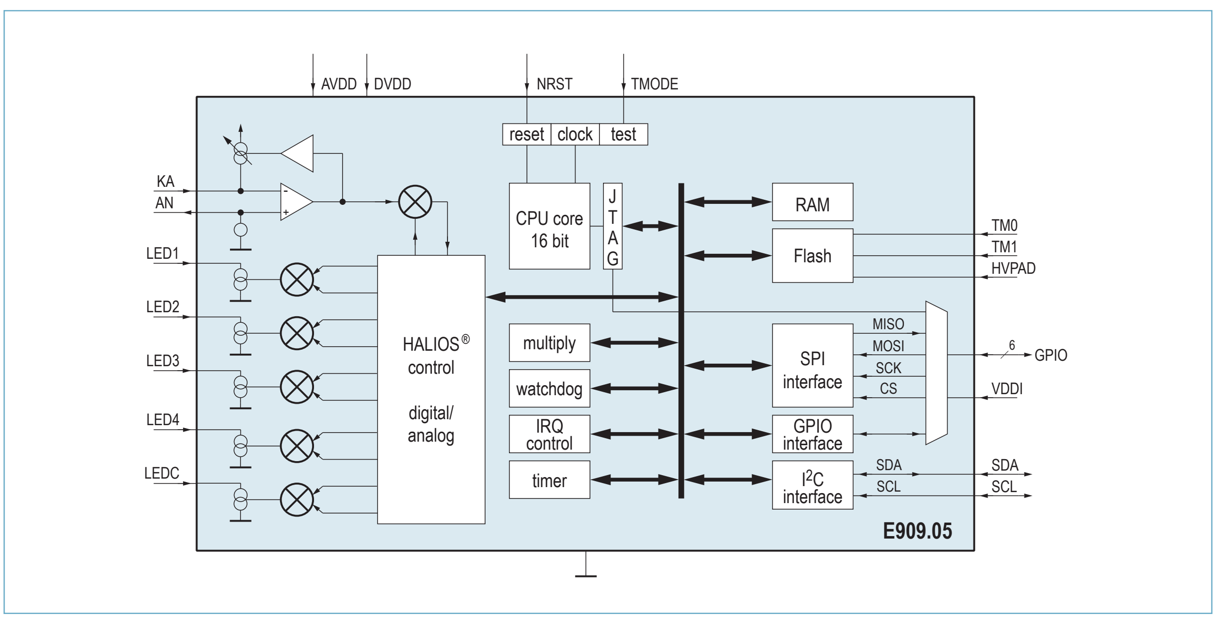
The HALIOS® multi purpose optical sensor is based on an optical bridge which provides a contactless detection of gestures (e.g. movement of a finger). The IC E909.05 processes data from optical reflections of an object in front of the sensor using a system called HALIOS® (High Ambient Light Independent Optical System). HALIOS® is highly efficient suppressing ambient light and also has an inherent self calibration capability to eliminate disturbances caused by housing reflections such as dirt or scratches.

New intuitive user interfaces are possible with this unique input device. All data is analyzed and evaluated internally with a high performance microprocessor and the data output can be easily customized.

HALIOS® devices can be applied behind closed surfaces which allows very flexible designs. HALIOS® firmware provides all necessary algorithms and software based filters.

Ordering Information

Product ID	Temp. Range	Package
E909.05	-40°C to +85°C	QFN32L5



1 Pinout

1.1 Pin Description

Nr.	Name	Type	Pull	ESD	Description
1	SDA	D_IO	---	+/- 2KV HBM	I²C data in/out
2	SCL	D_IO	---	+/- 2KV HBM	I²C clock input
3	IO5	D_IO	Down	+/- 2KV HBM	Multifunctional digital output 5
4	IO4	D_IO	Down	+/- 2KV HBM	Multifunctional digital output 4
5	IO3	D_IO	Down	+/- 2KV HBM	Multifunctional digital output 3
6	IO2	D_IO	Down	+/- 2KV HBM	Multifunctional digital output 2
7	IO1	D_IO	Down	+/- 2KV HBM	Multifunctional digital output 1
8	LED4	A_O	---	+/- 2KV HBM	Output sending LED4
9	LEDVSS	A_G	---	+/- 2KV HBM	Power ground LED
10	IO0	D_IO	Down	+/- 2KV HBM	Multifunctional digital output 0
11	TMODE	D_I	Down	+/- 2KV HBM	Test mode enable
12	NRST	D_I	Up	+/- 2KV HBM	Reset input, active low
13	VSSI	S	---	+/- 2KV HBM	Ground IO pins
14	VDDI	S	---	+/- 2KV HBM	Supply IO pins
15	DVDD	S	---	+/- 2KV HBM	Digital supply
16	DVSS	S	---	+/- 2KV HBM	Digital ground
17	LEDVSS	S	---	+/- 2KV HBM	Power ground LED
18	LED3	A_O	---	+/- 2KV HBM	Output sending LED3
19	LEDC	A_O	---	+/- 2KV HBM	Output compensation LED
20	nc	---	---	+/- 2KV HBM	---
21	nc	---	---	+/- 2KV HBM	---
22	CA	A_I	---	+/- 2KV HBM	Photo diode amplifier input
23	AN	A_I	---	+/- 2KV HBM	Reference voltage for photo diode
24	LED2	A_O	---	+/- 2KV HBM	Output sending LED2
25	LEDVSS	S	---	+/- 2KV HBM	Power ground LED
26	AVSS	S	---	+/- 2KV HBM	Analogue ground
27	AVDD	S	---	+/- 2KV HBM	Analogue supply voltage
28	TM1	A_IO	---	+/- 2KV HBM	FLASH test, analogue test bus
29	TM0	A_IO	---	+/- 2KV HBM	FLASH test, analogue test bus
30	VPP	HV_S	---	+/- 2KV HBM	FLASH program voltage
31	LED1	A_O	---	+/- 2KV HBM	Output sending LED1
32	LEDVSS	S	---	+/- 2KV HBM	Power ground LED

D = Digital, A = Analogue, S = Supply, I = Input, O = Output, HV = High Voltage (max. 15V), nc = not connected

Table 1.1.1 Pin Description

1.2 Package Reference

The device is available in a Pb free, RoHS compliant, 20-lead Quad Flat No Lead QFN32L5 package with 25mm² (0.0388 square inch) according to JEDEC standard MO-220- K ; Variant: VHHD-4.

1.3 Package Pinout

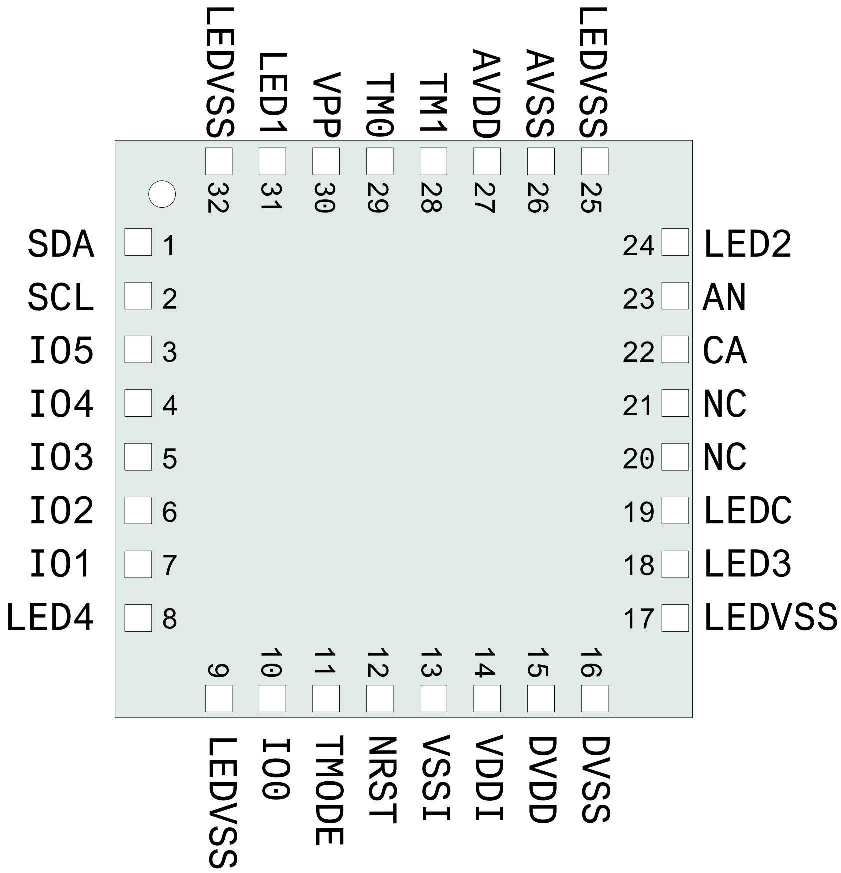


Figure 1.3-1: Package Pinout

2 Block Diagram

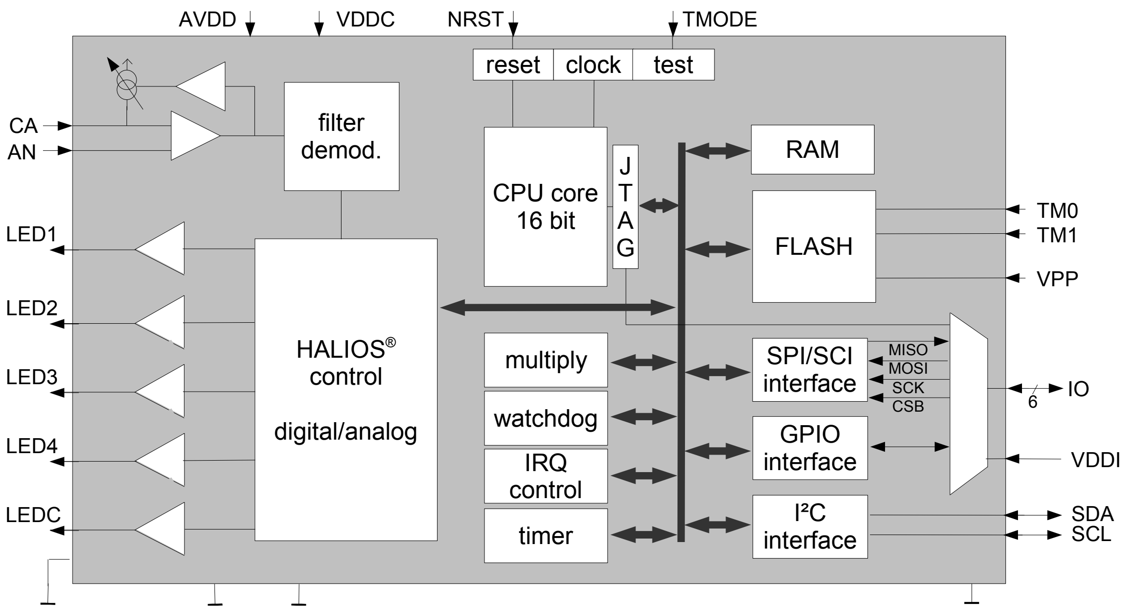


Figure 2-1 Block Diagram

3 Operating Conditions

3.1 Absolute Maximum Ratings

Continuous operation of the device above these ratings is not allowed and may destroy the device. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

Parameter	Condition	Symbol	Min.	Max.	Unit
Supply voltage: digital core, analogue part	Referenced to D_{VSS} / A_{VSS}	D_{VSS} / A_{VSS}	-0.3	2.8	V
IO supply voltage/digital pins (see "type"/chapter 1.1)	Referenced to V_{SSI}	V_{DDI}	-0.3	2.8	V
Input voltage analog pins (see "type"/chapter 1.1)	Referenced to A_{VSS}	V_{INA}	-0.3	A_{VDD} + 0.3	V
Input voltage digital pins/GPIO (see "type"/chapter 1.1)	Referenced to V_{SSI}	V_{IND}	-0.3	V_{DDI} + 0.3	V
Ground offset	D_{VSS} to A_{VSS} to LED_{VSS}		-0.3	0.3	V
Junction Temperature		T_J	-40	125	°C
Storage temperature		T_{STG}	-50	150	°C

Table 3.1.1 Absolute Maximum Ratings

3.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Supply voltage: analogue part, digital core	Referenced to D_{VSS}/A_{VSS}	D_{VDD}/A_{VDD}	2.25	2.5	2.75	V
IO supply voltage/digital pins (see "type"/chapter 1.1)	Referenced to V_{SSI}	V_{DDI}	1.50	1.8	D_{VDD}	V
Filter capacitor analogue part	Connected to A_{VDD}	C_{AVDD}		100		nF
Filter capacitor digital part	Connected to D_{VDD}	C_{DVDD}		100		nF
Ambient operating temperature range		T_{OPT}	-40	25	85	°C

Table 3.2.1 Recommended Operating Conditions

All voltages are referred to D_{VSS}, and currents are positive when flowing into the node unless otherwise specified.

4 Detailed Electrical Data Specification

The following conditions apply unless otherwise stated. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

4.1 Supply Voltages

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Digital operating current, run mode	FSYS = 8 MHz, system state: run	I_{DVDD}		5.8	12	mA
2	Digital operating current, standby mode	System state: standby	$I_{STANDBY}$		1.8	5	mA
3	Digital operating current, off mode	System state: off	I_{OFF}			35	µA
4	Analogue operating current	Analogue on = 1	I_{AVDD}		4.5	5.0	mA
5	Analogue operating current	Analogue on = 0	I_{AVDD_OFF}			15	µA
6	Over all current consumption in application mode	Active mode [1])	I_{ACTIVE}		2.0	2.25	mA
7	Over all current consumption in application mode	Idle mode ($I_{IDLE} = I_{OFF} + I_{AVDD\_OFF}$)	I_{IDLE}		16	50	µA
8	State change from STANDBY to RUN mode		TSTANDBY2RUN			3	1/FSYS
9	State change from OFF to RUN mode		TOFF2RUN			5	1/FSYS

Table 4.1.1 Supply: Parameters

[1]) In application mode the current consumption is calculated from the duty cycle of the digital operating current and the analogue operating current.

4.2 Reset Generation

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Power on reset level	Reference is D_{VDD}	V_{POR}			2.25	V
2	Brown out high-to-low threshold level	Reference is D_{VDD}	V_{BOHL}	1.95			V
3	Brown out reset hysteresis		V_{BOHYST}	100	200	300	mV
4	Minimum supply voltage for power on reset and brown out circuit ①		VDDmin		0.9		V
5	NRST-pin low-to-high threshold level		$NRST_{LH}$			0.80	V_{DDI}
6	NRST-pin high-to-low threshold level		$NRST_{HL}$	0.25			V_{DDI}
7	Pull up current NRST-pin	$V_{NRST} = V_{DDI}$	I_{NRSTPU}		20		µA
8	Min. pulse width for a valid reset at pin NRST (denoun-cing)	$D_{VDD} > D_{VDD}$ min	$T_{DEBNRST}$	200		-	ns
9	Delay Watchdog start ⇨ reset ①		T_{WDOG}		timer value		1/FSYS

Table 4.2.1 Reset Generation

① : Will not be tested in production test

4.3 Internal Clock Generation

4.3.1 Reference Clocks

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Wakeup clock frequency	Within recom-mended operating conditions	FWK	115.2	128.0	140.8	kHz
2	Master clock	Within recom-mended operating conditions	FSYS	7.2	8.0	8.8	MHz

Table 4.3.1.1 Reference Clocks

4.4 Module Description

4.4.1 I²C Interface

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	SDA/SCL: Input voltage low [1])		V_{IL}	-0.3		$0.3 \cdot V_{DDI}$	V
2	SDA/SCL: Input voltage high [1])		V_{IH}	$0.7 \cdot V_{DDI}$		$V_{DDI} + 0.3$	V
3	SDA/SCL: Hysteresis of Schmitt trigger inputs ①	$V_{DDI} > 2.0$ V	V_{hys}	$0.05 \cdot V_{DDI}$		-	V
4		$V_{DDI} < 2.0$ V	V_{hys}	$0.1 \cdot V_{DDI}$		-	V
5	SDA/SCL: Output voltage low, (open drain)	I = 3 mA $V_{DDI} > 2.0$ V	V_{OL}			0.4	V
6		I = 3 mA $V_{DDII} < 2.0$ V	V_{OL}			$0.2 \cdot V_{DDI}$	V
7	SDA/SCL: Input current	$0 < V_{IN} < V_{DDI}$	I_i	-10		10	µA
8	SDA/SCL: capacitance ①		C_i	-		10	pF
9	SCL clock frequency		f_{SCL}	0		400	kHz
10	Hold time (repeated) START condition ①		$t_{HD.:STA}$	600		-	ns
11	LOW period of SCL clock		t_{LOW}	1300		-	ns
12	HIGH period of SCL clock		t_{HIGH}	600		-	ns
13	Set-up time for repeated start condition ①		$t_{SU.:STA}$	600		-	ns
14	Data hold time ①		$t_{HD.DAT}$	0		900	ns
15	Data set-up time ①		$t_{SU:DAT}$	100		-	ns
16	Rise time of SDA and SCL signals with a bus capacitance (C_b) from 10 pF to 400 pF ①		t_r	20 + $0.1 \cdot C_b$		300	ns
17	Fall time of SDA and SCL signals with a bus capacitance (C_b) from 10 pF to 400 pF ①		t_f	20 + $0.1 \cdot C_b$		300	ns
18	SDA/SCL: Output fall time from V_{IH} to V_{IL} with a bus capacitance (C_b) from 10 pF to 400 pF ①		t_{of}	20 + $0.1 \cdot C_b$		250	ns
19	Set-up time for STOP condition ①		$t_{SU:STO}$	600		-	ns
20	Bus free time between STOP and START ①		t_{BUF}	1300		-	ns
21	Pulse width of spikes which must be suppressed by the ASIC-internal input filter		t_{SP}	0		50	ns

Table 4.4.1.1 I²C Interface

① : Will not be tested in production test

4.4.2 SPI Module

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	SCK pulse low width / pulse high width	transfer	Tck	4			1/FSYS
2	first SCK after falling CSB	start of transfer	Tcs1	2			1/FSYS
3	last SCK before rising CSB	end of transfer	Tcs2	2			1/FSYS
4	set-up time		Tsetup	1			1/FSYS
5	hold time		Thold	1			1/FSYS
6	data out after shift		Tso			3	1/FSYS
7	CSB high time		Tcsh	2			1/FSYS
8	data out change from Z to driven data	start of transfer	Tz1			1	1/FSYS
9	data out change from driven data to Z	end of transfer	Tz2			1	1/FSYS

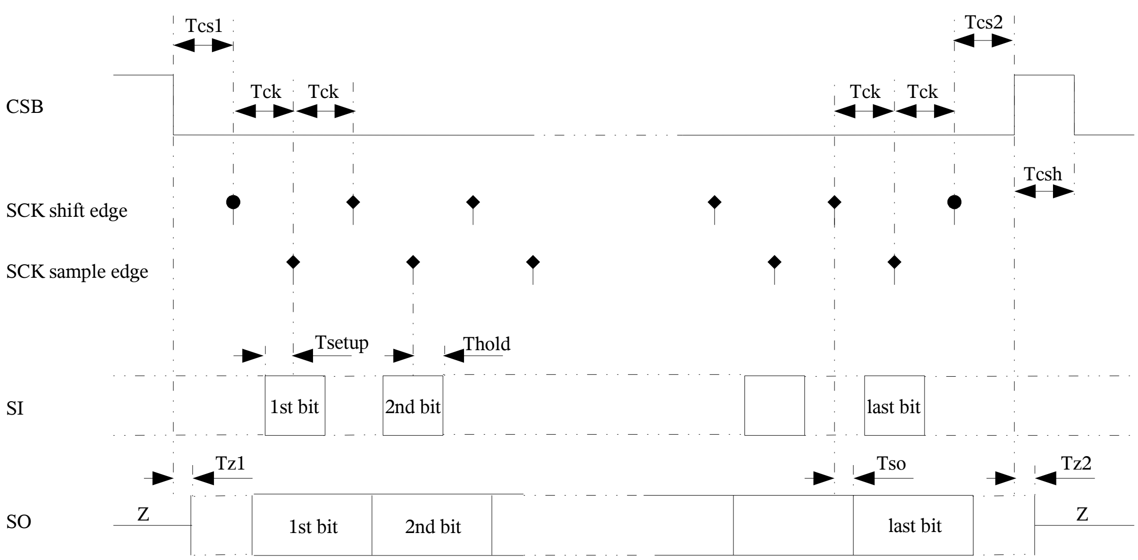


Figure 4.4.2-1 SPI Bus Timing Diagram

4.4.3 GPIO Module

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Low-to-high threshold level		$GPIO_{LH}$			0.80	V_{DDI}
2	High-to-low threshold level		$GPIO_{HL}$	0.25			V_{DDI}
3	Pull down resistor	$V_{IN} > 0.75 \cdot V_{DDI}$	R_{GPIOPD}	43	61	119	kΩ
4	Output Voltage Low	GPIOIOL = 2 mA VDDI = 1.8 V	GPIOVOL			0.4	V
5	Output Voltage High	GPIOIOH = 2 mA VDDI = 1.8 V	GPI- OVOH	1.4			V
6	Low Level Output Current	GPIOVOL=0.4V	GPIOIOL	3.5	5.7	7	mA
7	High Level Output Current	GPIOVOH=2.4V	GPIOIOH	-12.8	-8	-3.9	mA
8	Tri-State Input/Output Leak- age Current	Vout=VDDI or 0 V	GPIOILC	-1		1	uA

Table 4.4.3.1 IO Interface

① : Will not be tested in production test

4.4.4 HALIOS Interface

4.4.4.1 Current Generation for LED Modulators

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	DAC resolution		N		10		bit
2	Integral non linearity (INL)		Ei		2		LSB
3	Differential non linearity (DNL)		Ed		2		LSB
4	DAC output voltage at full scale		V_{MAX}		1.22		V

Table 4.4.4.1.1 Transmitting path: 10 bit DAC

4.4.4.2 LED Driver 1 -4

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Regulated proportion of LED current @ DAC = 0	DAC = 0	I_{R_MINS}			5 % of I_{R_MAXS} [1])	mA
2	Max. regulated proportion of LED current (RANGE)	RANGE = 31 DAC = 1023	I_{R_MAXS}		10.0		mA
3	Step size for regulated current-range configuration		I_{R_STEPS}		312.5		µA
4	Resolution current-range configuration		N_{RS}		5		bit
5	Max. fixed proportion of LED current (OFFSET)	OFFSET = 31	I_{O_MAXS}		10.0		mA
6	Step size for fixed offset-current configuration		I_{O_STEPS}		312.5		µA
7	Resolution offset-current configuration		N_{OS}		5		bit
8	DC-bias current		$I_{BIAS\ S}$		200		µA

Table 4.4.4.2.1 Transmitting path: current sources LED1-4

[1]) I_{R_MAXS} is the maximum current selected with parameter RANGE (Parameter “RANGE” described in chapter Fehler: Referenz nicht gefunden on page Fehler: Referenz nicht gefunden).

4.4.4.3 LED Driver C

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Regulated proportion of LED current @ DAC = 0	DAC = 0	I_{R_MINC}			5 % of I_{R_MAXS} [1])	mA
2	Max. regulated proportion of LED current (RANGE)	RANGE = 31 DAC = 1023	I_{R_MAXC}		4.0		mA
3	Step size for regulated current-range configuration		I_{R_STEPC}		125.0		µA
4	Resolution current-range configuration		N_{RC}		5		bit
5	Max. fixed proportion of LED current (OFFSET)	OFFSET = 127	I_{O_MAXC}		5.0		mA
6	Step size for fixed offset-current configuration		I_{O_STEPC}		40.0		µA
7	Resolution offset-current configuration		N_{OC}		7		bit
8	DC-bias current		$I_{BIAS\ C}$		100		µA

Table 4.4.4.3.1 Transmitting path: current source LEDC

[1]) $I_{RANGEMAXSX}$ is the maximum current selected with parameter RANGE (Parameter “RANGE” described in chapter Fehler: Referenz nicht gefunden on page Fehler: Referenz nicht gefunden).

4.4.4.4 Receiver

No.	Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
1	Transimpedance at amplifier input (CA)		Rf	70	100	130	kΩ
2	DC photo-current compensation		I_{DC}			1000	µA
3	Voltage at transimpedance amplifier input		V_{KA}		1.25		V
4	Corner frequency high pass filter		f_G		22		kHz
5	Gain amplifier		G_0		30		dB
6	Total gain		G_{TOT}		130		dBΩ
7	Center frequency		f_C		125		kHz
8	Resolution demodulator output		N_{DEMOD}	-	1	-	bit
9	Capacitance of photo diode at input CA		C_{DIODE}			70	pF
10	Internal reference voltage		V_{REF}		1.22		V
11	Internal reference current		I_{BIAS}		10		µA

Table 4.4.4.4.1 Receiver

5 Functional Description

5.1 Introduction

The general architecture of the 3D-optical input device is shown in the system block diagram.

The CPU is connected to the memory (FLASH and SRAM) and the peripheral modules via the internal system bus. The system bus provides a 16 bit address space and allows 8 and 16 bit data transfers.
The memory contains the program code and the data. Memory and registers are mapped to the global memory map and can be accessed through all memory related operation provided by the CPUs instruction set.
The memory of the ASIC consists of a 16Kx16 (32KByte) flash cell and a 1.5Kx16 (3KByte) SRAM cell.
The Interrupt Controller collects requests from all interrupt sources and provides an interrupt signal to the CPU. Interrupt sources can be masked within the interrupt controller. Interrupts are generated by the modules and hold until they are cleared within the module. See module description for clearing procedures.
The SPI can be configured either as a master or a slave. Transfer length is eight bit and can be extended by a multiple of eight bit. Data FIFOs are provided for transmit and receive tasks.

The timer module contains a 32 bit timer module as well as a watchdog timer. Additionally a second timer module operating on wakeup clock is implemented that remains active even in off mode, so it can be used for a periodical wake up from off mode for applications that require a low current consumption.

6 IO port pins can either be configured as general purpose IO`s or can be configured as ports for the SPI or JTAG module. Additionally two ports are reserved for the I^2C slave interface.

A more detailed diagram of the clock / reset generation block (CRG) is shown in the following sections.
The clock and reset generator module provides the system clock and the global reset signal. A power-on-reset, brown out detect and a power watch are implemented. As external reset source a reset input will be considered. The system clock is generated by two on-chip oscillators.

5.2 Supply voltages

5.2.1 Block Diagram

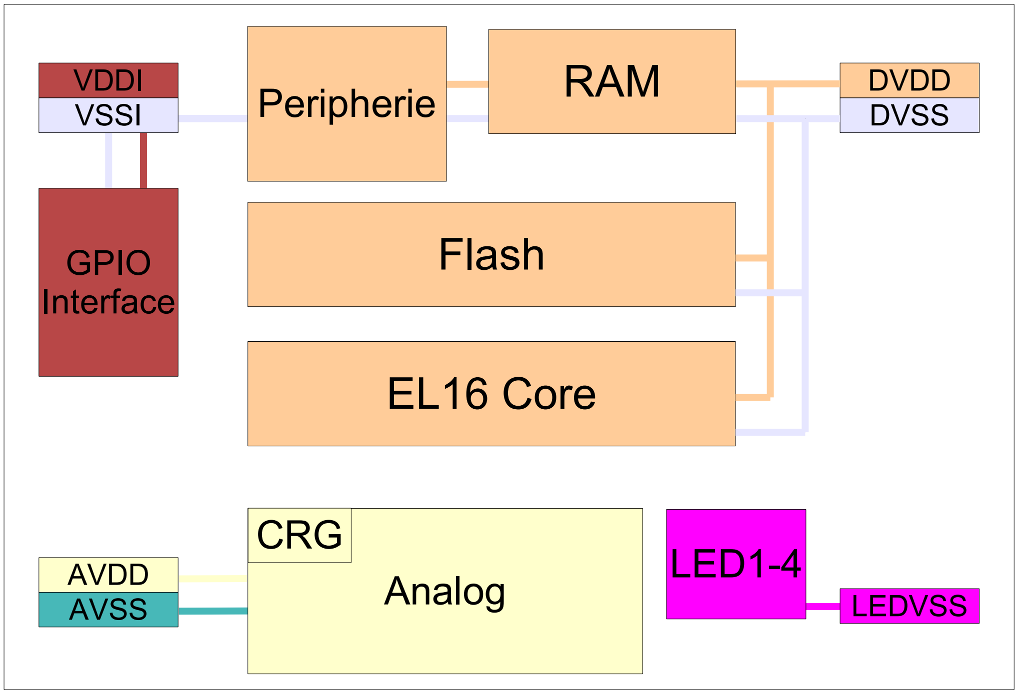


Figure 5.2.1-1 Block Diagram of Power Supply

5.2.2 Functional Description

Three separate power supplies are needed to operate the ASIC. The core voltage supplying all digital blocks, the analog parts needed for the oscillator and supply observation as well as the preamplifiers of the output pads and the IO supply which powers the post drivers of the GPIO pads. The third supply is used for the HALIOS measurement analog part. In the figure above the different power supply regions are depicted.

5.2.3 Power Up Sequence Considerations

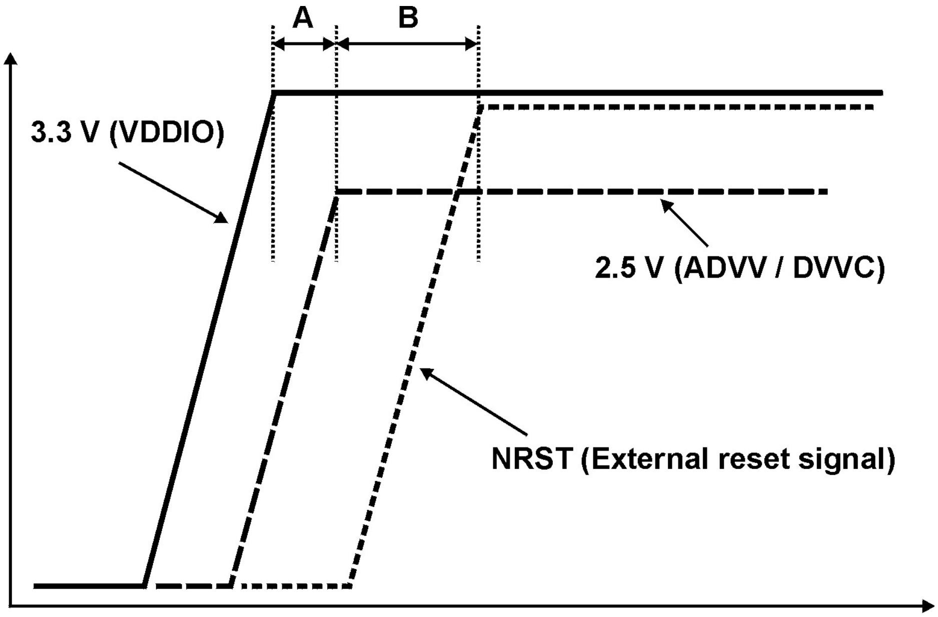
During power-up the power-on-reset configures all pads as inputs consequently disabling the output drivers. The IO supply is watched after power up if the core supply is in the specified range and causes a reset if it leaves the allowed region. The core supply is watched via a brown out circuit.
The pads will remain input pads as long as the software does not reconfigure them.

According the following diagram it must be guaranteed that ADVV / DVVC is not switched on before VDDIO. NRST can be switched on if the VDDIO and AVDD/DVVC are stabilized on its potential.

A >= 0ms
B > 5ms (recommended)

To avoid floating gates, A < 100µs is recommended.

Fig. 5.2.3-1: Power Up Sequence: A >= 0 ms; B > 5 ms



5.2.4 Power Down Sequence Considerations

During power down the chip will enter the reset state as soon as the core or IO supply leaves the specified region bringing all pads into input configuration again.

Note!

It has to be assured that VDDIO – VDDC > -0.3V at any time during power up and power down.

5.3 Brown Out Detection

5.3.1 Timing Diagram

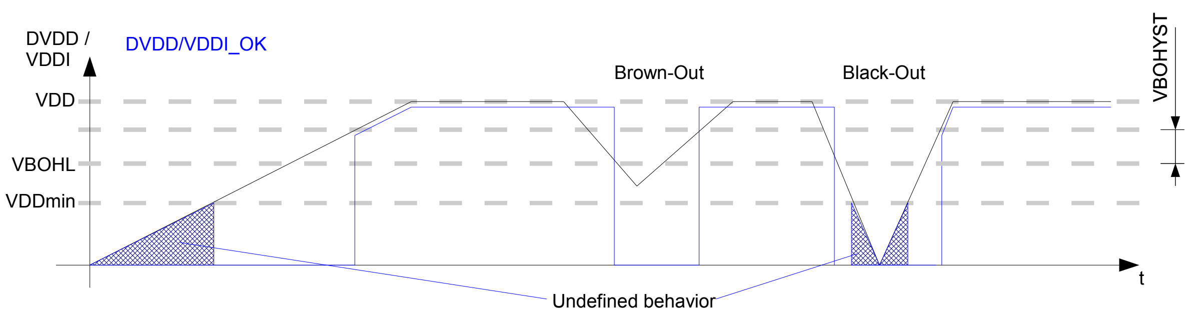


Figure 5.3.1-1 Brown-Out timing diagram

5.3.2 Functional Description

The brown out detection of the chip will cause a reset whenever the core or IO power supply falls below the specified region. An over-voltage protection is not implemented. The circuit will not be operational when the core supply is below VDDmin. In these cases the power-on-reset will take care of proper reset generation.

5.4 Reset Generation

5.4.1 Reset Generation (RESGEN)

The ASIC is equipped with a reset input pin which can be used to reset the chip. Any low pulse longer than TDEBNRST on the external reset line will be sensed and causes an ASIC reset.
The ASIC contains different dynamic and static reset sources. The static sources trigger the master reset as long as the cause for the reset persists. The dynamic sources trigger the reset for a defined minimum reset time. After that time has expired the system reset is released. In case the dynamic source is still signaling a reset the reset is re-triggered.

- Static reset sources:
  - A power up sequence of the core voltage (power on reset)
  - Brown out of the core voltage

- Dynamic reset sources:
  - SRAM parity error
  - CPU register parity error
  - watchdog time out

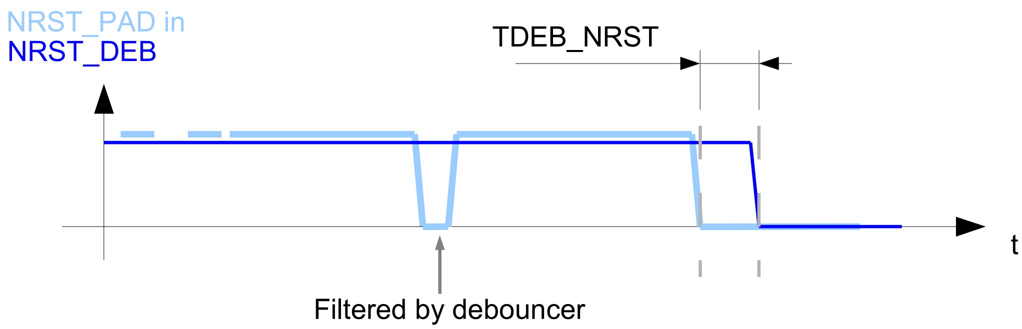


Figure 5.4.1-1 Timing of the external reset signal

5.4.2 Power-On-Reset

5.4.2.1 Timing Diagram

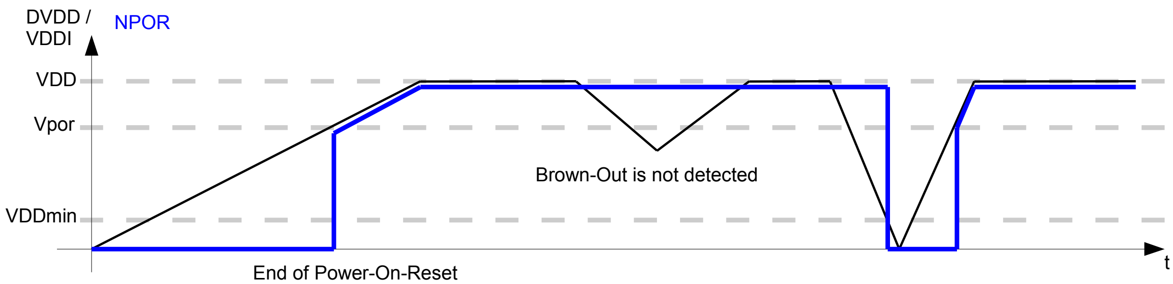


Figure 5.4.2.1-1 Power-On-Reset timing diagram

5.4.2.2 Functional Description

The power on reset is designed to cause a reset during the power on cycle of the chip. The reset will be deactivated when the supply crosses Vpor.
After the power up sequence the power on reset block will only cause a new reset if the power supply voltage drops below VDDmin and the rise and fall times of the supply are below the specified values.

5.5 System Failsafe Features

failsafe feature	asserts interrupt	asserts reset
FLASH write detection	x	
RAM byte parity		x
uninitialized RAM word / byte read detection		x
CPU register parity		x
CPU undefined opcode detection	x	
CPU misaligned word access detection	x	
opcode execution memory protection	x	
stack overflow detection	x	
invalid module register access detection	x	
watchdog time out		x
watchdog window protection	x	
brownout detection (supply voltage monitoring)		x

Table 5.5.1: Fail-safe Features

5.6 HALIOS Interface

5.6.1 Block Diagram

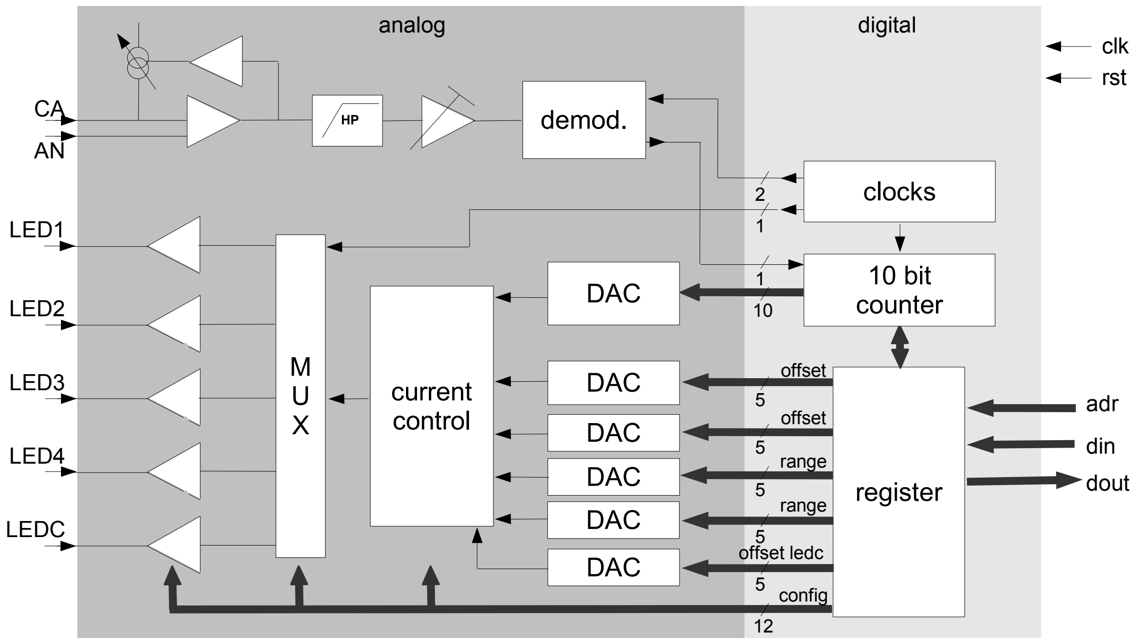


Figure 5.6.1-1 Block Diagram

5.6.2 Features

The ASIC contains a configurable HALIOS interface. It is possible to drive up to four sending LEDs and one compensation LED. The HALIOS measurement loop is closed by a 10 bit DAC which regulates the output current for the sending/compensation LED. The DAC is controlled by a counter that sets the DAC dependent on the received signal amplitudes up or down. To follow fast signal changes the counter can be increased or decreased by 1, 2, 4 or 8 steps, this is called the step size that is set due to the number of up/down-counts in the same direction. To start a new measurement the interface is configured with the counter-value and the step size (generally the values from the last measurement), the LED configuration and the current configuration for the LED driver. The measurement regulates the DAC and performs 25 counter steps to follow the actual reflection conditions of the sensor. After one measurement the interface returns the counter-value, the mean-value (it is calculated from the last 16 counter-steps during one measurement) and the step size from the last integrator cycle. After the automated measurement cycle is finished an interrupt appears if the interrupt is enabled. The interrupt is used to wake the system from standby mode..

5.6.3 HALIOS Module Registers

address offset	reset value	register name	size
0x00	0x0000	Start Value Counter	16
0x02	0x0000	Measurement Configuration	16
0x04	0x0000	Current Configuration phase A	16
0x06	0x0000	Current Configuration phase B	16

address offset	reset value	register name	size
0x08	0x00	Current Configuration compensator offset	8
0x0A	0x0000	Measurement result: Counter Value	16
0x0C	0x0000	Measurement result: Mean Value	16
0x0E	0x00	Interrupt	8

Table 5.6.3.1: Module Registers

Register Start Value Counter (0x00)

	MSB															LSB
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:12** : STZ: Startup step size for one step of the integrator (range: "0001", "0010", "0100" or "1000") **10** : 0 - normal settling time of optical gyrator 1 - decrease settling time of optical gyrator **9:0** : STRTCNT: Startup counter - value from the integrator (range: 0 ... 1023)															

Table 5.6.3.2: Start Value Counter

Register **Measurement Configuration** (0x02)

	MSB															**LSB**
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** : HALMEAS: Starts a new measurement phase, switching from '0' to '1' starts measurement. After measurement the bit resets itself. **14** : ACCON: En/disables the acceleration of the integrator ('0' = disabled, '1' = enabled) **13** : Deactivation of AN input to reduce current consumption in the case that only the CA input is used ('0' = active, '1' = deactivated) **12** : AON: Control of analogue part ('0' = off, '1' = on) **11** : FIXB: Sets the LEDs activated in phase B to fixed sending current ('0' = variable, '1' = fixed) **10** : FIXA: Sets the LEDs activated in phase A to fixed sending current ('0' = variable, '1' = fixed) **9** : LED C A: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: Bits 9 down to 0 will be reset after measurement **8** : LED C B: Decides if LED is active for the measurement ('0' = off, '1' = on) **7** : LED 4 A: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **6** : LED 4 B: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **5** : LED 3 A: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **4** : LED 3 B: Decides if LED is active for the measurement ('0' = off, '1' = on) Note: not available in version 1 and version 2 **3** : LED 2 A: Decides if LED is active for the measurement ('0' = off, '1' = on) **2** : LED 2 B: Decides if LED is active for the measurement ('0' = off, '1' = on) **1** : LED 1 A: Decides if LED is active for the measurement ('0' = off, '1' = on) **0** : LED 1 B: Decides if LED is active for the measurement ('0' = off, '1' = on)																

Table 5.6.3.3: Measurement Configuration

Register **Current Configuration Phase A** (0x04)

	MSB															LSB
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**9:5** : OFF: Offset phase A **4:0** : RNG: Range phase A															

Table 5.6.3.4: Current Configuration Phase A

Register **Current Configuration Phase B** (0x06)

	MSB															LSB
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**9:5** : OFF: OFFSET phase B **4:0** : RNG: RANGE phase B															

Table 5.6.3.5: Current Configuration Phase B

Transmitting current LED1-4:

In the regulated mode (FIXA/B = '0') the total current is

$$I_{total} = I_{OFFSET} + \frac{I_{REGULATE}}{1023} \cdot I_{RANGE} + I_{BIAS\,S}$$

, with $I_{REGULATE}$ = 0 ... 1023 (10 bit DAC)

I_{OFFSET} = OFFSET $\cdot$ I_{O_STEPS}
I_{RANGE} = RANGE $\cdot$ I_{R_STEPS}

In constant mode (FIXA = '1' or FIXB = '1'):

$$I_{total} = I_{OFFSET} + \frac{I_{RANGE}}{2} + I_{BIAS\,S}$$

where $I_{BIAS\,S}$ is a small current which always keeps the LEDs turned on to maximise speed and minimise parasitic effects.

Register **Current Configuration Compensator Offset** (0x08)

	MSB															LSB
Content	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**11:8** : DC_OFFSET current LEDC (4 Bit) **6:0** : OFFSET compensation LEDC															

Table 5.6.3.6: Current Configuration Compensator Offset

The offset current for the terminal LEDC is configureable with the seven bit value *OFFSET*.

Transmitting current LEDC:

The total current in regulated mode (FIXA/B = '0') for LEDC is

$$I_{total} = I_{OFFSET} + \frac{I_{REGULATE}}{1023} \cdot I_{RANGE} + I_{BIASC}$$

, with $I_{REGULATE}$ = 0 ... 1023 (10 bit DAC)

I_{OFFSET} = OFFSET $\cdot$ I_{O_STEPC}
I_{RANGE} = RANGE $\cdot$ I_{R_STEPC}

Register **Measurement Result: Counter Value** (0x0A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:12** : STZ: Stepsize integrator **9:0** : COUNT: Integrator value from the measurement															

Table 5.6.3.7: Measurement Result: Counter Value

Register **Measurement Result: Mean Value** (0x0C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:12** : STZ: Stepsize integrator **11:0** : MEAN: Mean value from the measurement															

Table 5.6.3.8: Measurement Result: Mean Value

Register **Interrupt** (0x0E)

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Content	-	-	-	-	-	-	1	0
Reset value	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R/W	R/W
External access	R	R	R	R	R	R	R/W	R/W
Bit Description	**1** : CLHALI: Clear HALIOS® interrupt 0 - no influence 1 - clear HALIOS® interrupt **0** : HALIE: HALIOS® interrupt enable: 0 - interrupt disabled 1 - interrupt enabled							

Table 5.6.3.9: Interrupt

6 Microcontroller EL16

6.1 Feature List

The CPU incorporates features specifically designed for modern programming techniques such as calculated branching, table processing and the use of high-level languages such as C. The CPU can address the complete address range without paging.
The CPU features include:

- RISC architecture with 27 instructions and 7 addressing modes.
- Orthogonal architecture with every instruction usable with every addressing mode
- Full register access including program counter, status registers, and stack pointer
- 16 registers including PC, SP and status register
- non paged 16-Bit address space
- Word and byte addressing and instruction formats.
- Single-cycle register operations.
- interrupt support
- standby and stop mode support
- bus wait support
- debugging support (JTAG interface)
- failsafe architecture

6.2 Debugging

To access the debug structures of the EL16 CPU a 4-wire standard JTAG interface is used. The JTAG interface can be accessed via the GPIO pins 2 to 5 when the TMODE pin is set to one. TMODE pin set to zero resets all test and debug structures and the ASIC operates in normal mode (see Fehler: Referenz nicht gefunden Fehler: Referenz nicht gefunden for details).

6.3 CPU Registers

The EL16 contains 16 registers (R0 to R15) including program counter, stack pointer and status register

6.3.1 Program Counter (PC)

The 16-bit program counter (PC/R0) points to the next instruction to be executed. Each instruction uses an even number of bytes (two, four, or six), and the PC is incremented accordingly. Instruction accesses in the 64-KB address space are performed on word boundaries, and the PC is aligned to even addresses. The PC can be addressed with all instructions and addressing modes.

6.3.2 Stack Pointer (SP)

The stack pointer (SP/R1) is used by the CPU to store the return addresses of subroutine calls and interrupts. It uses a pre-decrement, post-increment scheme. In addition, the SP can be used by software with all instructions and addressing modes. The SP is initialized into RAM by the user, and is aligned to even addresses.

6.3.3 Status Register (SR)

The status register (SR/R2), used as a source or destination register, can be used in the register mode only addressed with word instructions. The remaining combinations of addressing modes are used to support the constant generator.

Register **Status Register** (SR/R2)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**Bit 8** : V **Bit 5** : CLK OFF **Bit 4** : CPU OFF **BIT3** : GIE **Bit2** : N **Bit1** : Z **BIT0** : C															

Table 6.3.3.1: Status Register

V: Overflow bit
This bit is set when the result of an arithmetic operation overflows the signed-variable range.

CLKOFF: Stop flag
CPU clock gated

CPUOFF: Standby flag
CPU halted

GIE: Global Interrupt Enable

N: Negative bit
This bit is set when the result of a byte or word operation is negative and cleared when the result is not negative. Word operation: N is set to the value of bit 15 of the result Byte operation: N is set to the value of bit 7 of the result

Z: Zero bit
This bit is set when the result of a byte or word operation is 0 and cleared when the result is not 0.

C: Carry bit
This bit is set when the result of a byte or word operation
produced a carry and cleared when no carry occurred.

6.3.4 Constant Generation Registers CG1 and CG2

Six commonly-used constants are generated with the constant generator registers R2 and R3, without requiring an additional 16-bit word of program code. The constants are selected with the source-register addressing modes (As), as described in the table below:

Register	**As**	**Value**	**Remarks**
R2	00	-----	Register Mode
R2	01	(0)	Absolute Address Mode
R2	10	00004h	+4, bit processing

Register	As	Value	Remarks
R2	11	00008h	+8, bit processing
R3	00	00000h	0, byte processing
R3	01	00001h	+1
R3	10	00002h	+2, bit processing
R3	11	0FFFFh	-1, word processing

Table 6.3.4.1: Constant Generation Register CG1/CG2 Table

The constant generator advantages are:

- No special instructions required
- No additional code word for the six constants
- No code memory access required to retrieve the constant

The assembler uses the constant generator automatically if one of the six constants is used as an immediate source operand. Registers R2 and R3, used in the constant mode, cannot be addressed explicitly; they act as source-only registers.

6.3.5 General-Purpose Register R4 - R15

The twelve registers, R4−R15, are general-purpose registers. All of these registers can be used as data registers, address pointers, or index values and can be accessed with byte or word instructions.

6.4 Addressing Modes

Seven addressing modes for the source operand and four addressing modes for the destination operand can address the complete address space with no exceptions. The bit numbers in the table below describe the contents of the As(source) and Ad (destination) mode bits.

As/Ad	Addressing Mode	Syntax	Description
00/0	Register mode	Rn	Register contents are operand
01/1	Indexed mode	X(Rn)	(Rn + X) point to the operand. Xis stored in the next word
01/1	Symbolic mode	ADDR	(Rn + X) point to the operand. Xis stored in the next word. Indexed mode X(PC) is used.
01/1	Absolute mode	&ADDR	The word following the instruction contains the absolute address. X is stored in the next word. Indexed mode X(SR) is used.
10/-	Indirect Register mode	@Rn	Rn is used as a pointer to the operand.
11/-	Indirect auto increment	@Rn+	Rn is used as a pointer to the operand. Rn is incremented afterwards by 1 for .B instructions and by 2 for .W instructions.

As/Ad	Addressing Mode	Syntax	Description
11/-	Immediate mode	#N	The word following the instruction contains the immediate constant N. Indirect auto-increment mode @PC+ is used.

Table 6.4.1: Addressing Modes Table

6.5 EL16 Instruction Set

The complete EL16 instruction set consists of 27 core instructions and 24 emulated instructions. The core instructions are instructions that have unique op-codes decoded by the CPU. The emulated instructions are instructions that make code easier to write and read, but do not have op-codes themselves, instead they are replaced automatically by the assembler with an equivalent core instruction. There is no code or performance penalty for using emulated instruction.
There are three core-instruction formats:

- Dual-operand
- Single-operand
- Jump

All single-operand and dual-operand instructions can be byte or word instructions by using .B or .W extensions. Byte instructions are used to access byte data or byte peripherals. Word instructions are used to access word data or word peripherals. If no extension is used, the instruction is a word instruction.
The source and destination of an instruction are defined by the following fields:

Abbr.	Description
src	The source operand defined by As and S-reg
dst	The destination operand defined by Ad and D-reg
As	The addressing bits responsible for the addressing mode used for the source (src)
S-reg	The working register used for the source (src)
Ad	The addressing bits responsible for the addressing mode used for the destination (dst)
D-reg	The working register used for the destination (dst)
B/W	Byte or word operation: 0: word operation, 1: byte operation

Table 6.5.1: source and destination of an instruction

The following tables shows coding table of the 16 bit opcode:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Mnemonic
0	0	0	0	0	0											--
0	0	0	1	0	0	0	0	0	0	Ad/As		D-Reg/S-Reg				RRC
						0	0	0	1							RRC.B
						0	0	1	0							SWP.B
						0	0	1	1							---
						0	1	0	0							RRA
						0	1	0	1							RRA.B
						0	1	1	0							SXT
						0	1	1	1							---
						1	0	0	0							PUSH
						1	0	0	1							PUSH.B
						1	0	1	0							CALL
						1	0	1	1							---
						1	1	0	0							RETI
						1	1	0	1							---
						1	1	1	0							---
						1	1	1	1							---
0	0	0	1	0	1											---
				1	0											---
				1	1											---
0	0	1	0	0	0	10-Bit PC Offset										JNZ / JNE
			0	0	1											JZ / JEQ
			0	1	0											JNC / JLO
			0	1	1											JC / JHS
			1	0	0											JN
			1	0	1											JGE
			1	1	0											JL
			1	1	1											JMP
0	1	0	0	S-Reg				Ad	B/W	As		D-Reg				MOV
0	1	0	1													ADD
0	1	1	0													ADDC
0	1	1	1													SUBC
1	0	0	0													SUB
1	0	0	1													CMP
1	0	1	0													DADD
1	0	1	1													BIT
1	1	0	0													BIC
1	1	0	1													BIS
1	1	1	0													XOR
1	1	1	1													AND

Fig. 6.5-1: coding of the 16 bit op-code

Mnemonic	Parameters	Description		V	N	Z	C
ADC(.B)**	dst	Add C to destination	dst + C -> dst	*	*	*	*
ADD(.B)	src, dst	Add source to destination	src + dst -> dst	*	*	*	*
ADDC(.B)	src, dst	Add source to C and destination	src + dst + C -> dst	*	*	*	*
AND(.B)	src, dst	AND source and destination	src AND dst -> dst	0	*	*	*
BIC(.B)	src, dst	Clear bits in destination	NOT(src) AND dst -> dst	-	-	-	-
BIS(.B)	src, dst	Set bits in destination	src OR dst -> dst	-	-	-	-
BIT(.B)	src, dst	Test bits in destination	src AND dst	0	*	*	*
BR	dst	Branch to destination	dst -> PC	-	-	-	-
CALL	dst	Call destination	SP-2 -> SP, PC+2 -> @SP, dst -> PC	-	-	-	-
CLR (.B)**	dst	Clear destination 0	0 -> dst	-	-	-	-
CLRC**	---	Clear C 0	0 -> C	-	-	-	0
CLRN**	---	Clear N 0	0 -> N	-	0	-	-
CLRZ**	---	Clear Z 0	0 -> Z	-	-	0	-
CMP (.B)	src, dst	Compare source and destination	dst - src	*	*	*	*
DADC (.B)**	dst	Add C decimally to destination	dst + C -> dst	0	*	*	*
DADD (.B)	src, dst	Add source and C decimally to destination	src + dst + C -> dst	0	*	*	*
DEC (.B)**	dst	Decrement destination	dst -1 -> dst	*	*	*	*
DECD (.B)**	dst	Double decrement destination	dst -2 -> dst	*	*	*	*
DINT**	---	Disable interrupts 0	0 -> GIE	-	-	-	-
EINT**	---	Enable interrupts 1	1 -> GIE	-	-	-	-
INC (.B)	dst	Increment destination	dst +1 -> dst	*	*	*	*
INCD (.B)**	dst	Double increment destination	dst +2 -> dst	*	*	*	*
INV (.B)**	dst	Invert destination	NOT(dst) -> dst	*	*	*	*
JC / JHS	label	Jump if C set / Jump if higher or same	if (condition) PC + 2 * offset -> PC	-	-	-	-
JZ / JEQ	label	Jump if Z set / Jump if equal	if (condition) PC + 2 * offset -> PC	-	-	-	-
JGE	label	Jump if greater or equal	if (condition) PC + 2 * offset -> PC	-	-	-	-
JL	label	Jump if less	if (condition) PC + 2 * offset -> PC	-	-	-	-
JMP	label	Jump	PC + 2 * offset -> PC	-	-	-	-
JN	label	Jump if N set / Jump if negative	if (condition) PC + 2 * offset -> PC	-	-	-	-
JNC /JLO	label	Jump if C not set / Jump if lower	if (condition) PC + 2 * offset -> PC	-	-	-	-
JNZ / JNE	label	Jump if Z not set / Jump if equal	if (condition) PC + 2 * offset -> PC	-	-	-	-
MOV (.B)	src, dst	Move source to destination	src -> dst	-	-	-	-
NOP	---	No operation	---	-	-	-	-
POP (.B)**	dst	Pop item from stack to destination	@SP+ -> dst	-	-	-	-
PUSH (.B)	src	Push source onto stack	SP -2 -> SP, src -> SP	-	-	-	-
RET**	---	Return from subroutine	@SP -> PC	-	-	-	-
RETI	---	Return from interrupt	@SP -> SR, @SP+ -> PC	*	*	*	*
RLA (.B)**	dst	Rotate left arithmetically	dst * 2 -> dst	*	*	*	*
RLC (.B)**	dst	Rotate left through C	dst * 2 -> dst, C -> LSB(dst)	*	*	*	*
RRA (.B)	dst	Rotate right arithmetically	dst / 2 -> dst	0	*	*	*
RRC (.B)	dst	Rotate right through C	dst / 2 -> dst, C -> MSB(dst)	0	*	*	*
SBC (.B)**	dst	Subtract not(C) from destination	dst + NOT(0) + C -> dst	*	*	*	*
SETC**	---	Set C	1 -> C	-	-	-	1
SETN**	---	Set N	1 -> N	-	1	-	-
SETZ**	---	Set Z	1 -> Z	-	-	1	-
SUB (.B)	src, dst	subtract source from destination	dst + NOT(src) + 1 -> dst	*	*	*	*
SUBC (.B)**	src, dst	subtract source and not(C) from destination	dst + NOT(src) + C -> dst	*	*	*	*
SWPB	dst	Swap bytes	---	-	-	-	-
SXT	dst	Extend sign	---	0	*	*	*
TST (.B)**	dst	Test destination	dst + NOT (0) + 1	0	*	*	1
XOR(.B)	src, dst	Exclusive OR source and destination	src XOR dst -> dst	*	*	*	*

Fig. 6.5-2: Instruction Set of EL16

6.5.1 EL16 Instruction Cycle Counts

command type	operation	cycles	cycles(dreg==PC)
MOV DOUBLE	sreg -> dreg sreg x dreg -> dreg	1 1	2 2
MOV DOUBLE	sreg -> Y(dreg) -> dreg sreg x Y(dreg) -> Ydreg	3 4	---
MOV DOUBLE	@sreg -> dreg @sreg x dreg -> dreg	2 2	3 3
MOV DOUBLE	@sreg -> Y(dreg) -> dreg @sreg x Y(dreg) -> Ydreg	4 5	---
MOV DOUBLE	@sreg+ -> dreg @sreg+ x dreg -> dreg	2 2	3 3
MOV DOUBLE	@sreg+ -> Y(dreg) -> dreg @sreg+ x Y(dreg) -> Ydreg	4 5	---
MOV DOUBLE	Xsreg+ -> dreg Xsreg+ x dreg -> dreg	3 3	4 4
MOV DOUBLE	Xsreg+ -> Y(dreg) -> dreg Xsreg+ x Y(dreg) -> Ydreg	5 6	---
SINGLE SINGLE SINGLE SINGLE	dreg @dreg @dreg+ Y(dreg)	--- --- --- ---	2 --- --- ---
JUMP RETI IRCQ	--- --- ---	2 3 4	--- --- ---
PUSH PUSH PUSH PUSH	reg @reg @reg+ X(reg)	3 4 4 5	--- --- --- ---
CALL CALL CALL CALL	reg @reg @reg+ X(reg)	3 4 4 5	--- --- --- ---

Fig. 6.5.1-1: EL16 Instruction Cycle Counts

6.6 Memory Description

6.6.1 Memory Map

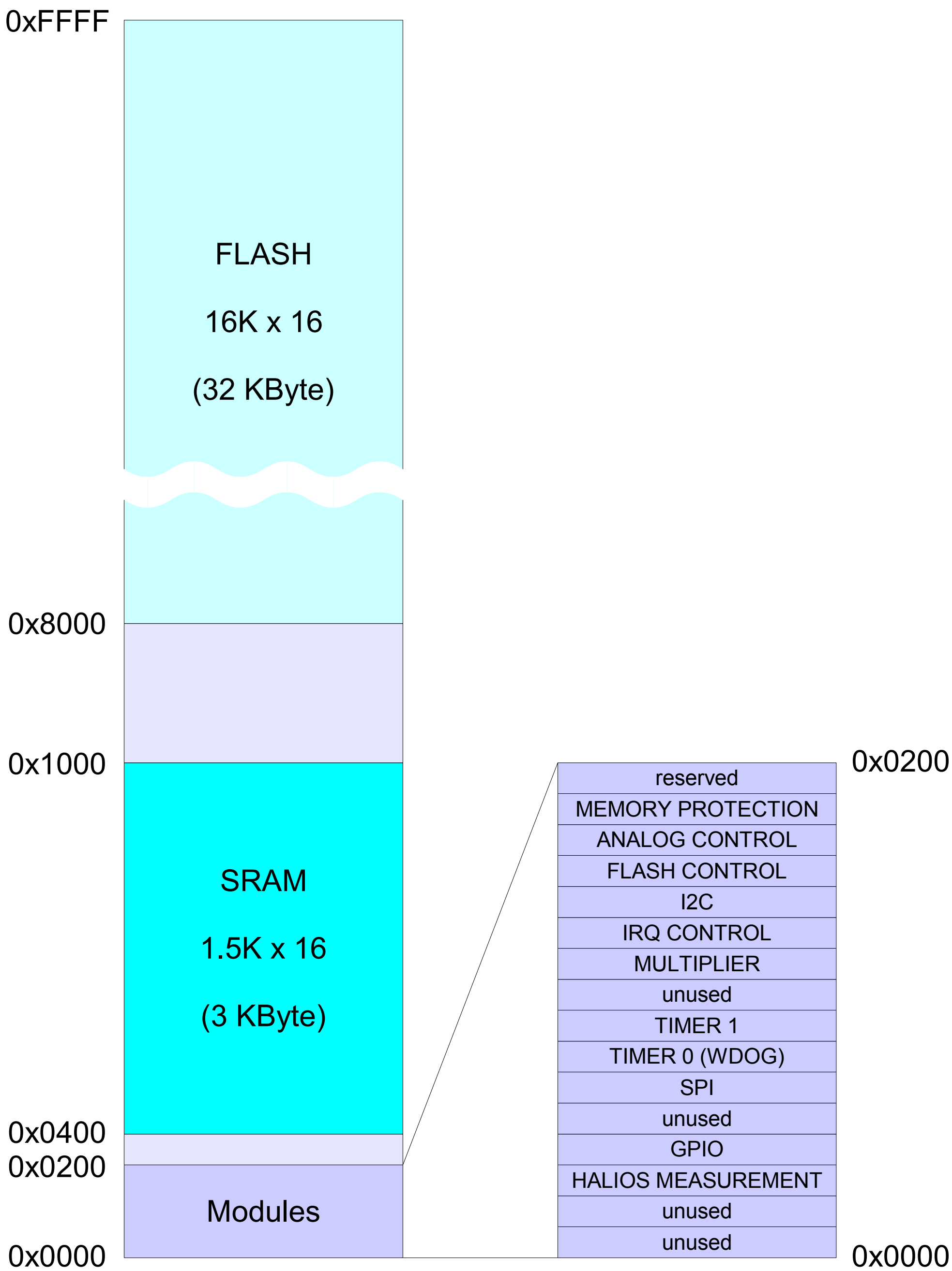


Figure 6.6.1-1: memory map

6.6.2 Base Address Table

base address	size	module name
0x8000	0x7FFF	FLASH
0x1000	0x7000	reserved
0x0400	0x0C00	SRAM
0x0200	0x0200	reserved
0x01E0	0x0020	reserved
0x01C0	0x0020	memory protection module
0x01A0	0x0020	analogue control module
0x0180	0x0020	FLASH control module
0x0160	0x0020	I2C module
0x0140	0x0020	interrupt control module
0x0120	0x0020	multiplier module
0x0100	0x0020	reserved
0x00E0	0x0020	timer module 1
0x00C0	0x0020	timer module 0 (watchdog)
0x00A0	0x0020	SPI module
0x0080	0x0020	reserved
0x0060	0x0020	GPIO module
0x0040	0x0020	HALIOS measurement module
0x0020	0x0020	reserved
0x0000	0x0020	reserved

Table 6.6.2.1: Base Address Table

6.6.3 FLASH

- main block size: 16k x 16Bit (32 kByte)
- info block size: 64 x 16Bit (128 Byte)
- for FLASH test mode details see flash control and test mode description

6.6.4 SRAM

- size: 1.5K x 16Bit (3KByte)
- byte write enable support
- each byte is extended by a parity bit

6.7 Memory Protection Module

- opcode execute area configuration (granularity: 1KByte, 64 areas)
- stack area configuration (granularity: 256Byte, 12 areas)
- invalid module register address handling

6.7.1 Memory Protection Module Registers

address offset	reset value	register name	size
0x00	0x0000	opcode execute enable 0	16
0x02	0x0000	unused	16
0x04	0xFFFF	opcode execute enable 2	16
0x06	0xFFFF	opcode execute enable 3	16
0x08	0x0000	execute address value	16
0x0A	0x0FFF	stack enable	16
0x0C	0x0000	invalid address value	16
0x0E	-	interrupt clear	16

Table 6.7.1.1: Memory Protection Module Registers

Register op-code **execute enable 0** (0x00)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15** :4 unused enable 0 - execution of opcode denied 1 - execution of opcode allowed area size: 1 KByte bit 0 - area 0x0000 to 0x03FE bit 1 - area 0x0400 to 0x07FE bit 2 - area 0x0800 to 0x0BFE bit 3 - area 0x0C00 to 0x0FFE															

Table 6.7.1.2: op-code execute enable 0

Register op-code **execute enable 1** (0x02)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	enable 0 - execution of opcode denied 1 - execution of opcode allowed area size: 1 KByte bit 0 - area 0x4000 to 0x43FE bit 1 - area 0x4400 to 0x47FE .... bit 15 - area 0x7000 to 0x7FFE															

Table 6.7.1.3: op-code execute enable 0

Register op-code **execute enable 2** (0x04)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	enable 0 - execution of opcode denied 1 - execution of opcode allowed area size: 1KByte bit 0 - area 0x8000 to 0x83FE bit 1 - area 0x8400 to 0x87FE .... bit 15 - area 0xB000 to 0xBFFE															

Table 6.7.1.4: op-code execute enable 2

Register op-code **execute enable 3** (0x06)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	enable 0 - execution of opcode denied 1 - execution of opcode allowed area size: 1KByte bit 0 - area 0xC000 to 0xC3FE bit 1 - area 0xC400 to 0xC7FE .... bit 15 - area 0xF000 to 0xFFFE															

Table 6.7.1.5: op-code execute enable 3

Register **execute address value** (0x08)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : address of last denied opcode access															

Table 1: failure address value

Register **stack enable** (0x0A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	enable 0 - use as stack denied 1 - use as stack allowed area size: 256Byte bit 0 - area 0x0400 to 0x04FE bit 1 - area 0x0500 to 0x05FE .... bit 11 - area 0x0F00 to 0x0FFE															

Table 2: stack enable

Register **invalid address value** (0x0C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : address of last invalid module register access															

Table 3: invalid address value

Register **interrupt clear** (0x0E)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W
External access	-	-	-	-	-	-	-	-	-	-	-	W	W	W	W	W
Bit Description	**4** : undefined op-code IRQ clear (address of undefined op-code can be obtained by looking to the return address stored in stack minus - 2) 0 - no influence 1 - clear interrupt **3** : misaligned 16 bit access IRQ clear 0 - no influence 1 - clear interrupt **2** : invalid address IRQ clear 0 - no influence 1 - clear interrupt **1** : stack protection IRQ clear 0 - no influence 1 - clear interrupt **0** : execute protection IRQ clear 0 - no influence 1 - clear interrupt																

Table 4: interrupt clear

6.8 Analogue Control Module

- controls clock and reset generator (CRG)

6.8.1 Analogue Control Module Registers

address offset	reset value	register name	size
0x00	0x0010	wakeup timer config	16
0x02	0x0000	MCLK trim value	16
0x04	0x0000	WKCLK trim value	16
0x10	-	reset source status	16
0x12	-	reset source status clear	16
0x14	-	wakeup timer interrupt status	16
0x16	-	wakeup timer interrupt clear	16

Table 6.8.1.1: Analog Control Module Registers

Register wake-up **timer config** (0x00)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5, will always be read as 0x96 **4** : enable timer 0 - timer off 1 - timer on **3:0** : timer value: timer period = 2 ms * [timer value + 1], with timer value 0...15															

Table 6.8.1.2: wake-up timer config

Register **MCLK trim value** (0x02)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:4** : unused **3:0:** Trim value for master clock oscillator: “0111”: lowest frequency “0000”: centre frequency “1000”: highest frequency															

Table 6.8.1.3: MCLK trim value

Register **WKLK trim value** (0x04)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:4** : unused **3:0:** Trim value for wakeup clock oscillator: “0111”: lowest frequency “0000”: centre frequency “1000”: highest frequency															

Table 6.8.1.4: WKCLK trim value

Register **reset source status** (0x10)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15** : level of incoming external reset signal (NRST) **8** : Trap -> masked interrupt event occurred (interrupt number 0 and 1) **7** : RAM parity error **6** : FLASH uncorrectable bit error **5** : CPU register parity error **4** : watchdog reset **1** : external reset **0** : power on reset / supply observe / trim register ECC error															

Table 6.8.1.5: reset source status

Register **reset source status clear** (0x12)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W
External access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Description	**0** : clears all reset status bits 0 - no influence 1 - clears all reset status bits															

Table 6.8.1.6: reset source status clear

Register wake-up **timer interrupt status** (0x14)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**0** : wake-up timer interrupt status 0 - no interrupt 1 - interrupt was asserted															

Table 6.8.1.7: wake-up timer interrupt status

Register wake-up **timer interrupt clear** (0x16)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W
External access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W
Bit Description	**0** : timer IRQ clear 0 - no influence 1 - clear interrupt															

Table 6.8.1.8: wake-up timer interrupt clear

6.9 FLASH Control Module

- FLASH area protection (area size: 2K words)
- main and info block read, program, page erase and mass erase support
- software adaptable program and erase timing

6.9.1 Flash Control Module Registers

address offset	reset value	register name	size
0x00	0x9600	area protection (areas 7 - 0)	16
0x02	0x9600	area protection (info block)	16
0x04	0x9600	mode	16
0x06	-	status	16
0x08	-	IRQ clear	16
0x0A	0	wait cycle register	16
0x0C	0	bit error corrected address	16
0x10	6	Tnvs / Tnvh	16
0x12	120	Tnvh1	16
0x14	12	Tpgs	16
0x16	1	Tpgh	16
0x18	2	Trcv	16
0x1A	30	Tprog	16
0x1C	6	Terase	16
0x1E	60	Tme	16

Table 6.9.1.1: FLASH Control Module Registers

Register **area protection (areas 0 - 7)** (0x00)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96															
	7:0 : writeable 0 - area protected 1 - area writeable areas 0 - 7 are FLASH main block areas (8 * 2K words)															

Table 6.9.1.2: area protection (areas 0 - 7)

Register **area protection (info_block)** (0x02)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96															
	7 writeable 0 - area protected 1 - area writeable															
	6:0 : reserved															

Table 6.9.1.3: area protection (info block)

Register **mode** (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	0	0	1	0	1	1	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **7:0** : mode 0x01 - main block read 0x02 - info block read 0x04 - main block program 0x08 - info block program 0x10 - erase main block page 0x20 - erase info block 0x40 - mass erase main block 0x80 - mass erase main and info block every over written mode value results in "main block read" mode															

Table 6.9.1.4: mode

Register **status** (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**2** : write error unexpected FLASH write access this bit is cleared by write error IRQ clear **1** : row programming incomplete current number of programmed row words != word config (see below) **0** : busy 0 - ready 1 - busy (program or erase is still in progress)															

Table 1: status

Register **IRQ clear** (0x08)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W
External access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W
Bit Description	**0** : write error IRQ clear 0 - no influence 1 - clear interrupt															

Table 2: IRQ clear

Register **wait cycle register** (0x0A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96															
	wait cycles per FLASH read access															

Table 3: wait cycles register

Register **bit error corrected address** (0x0C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : address of last correctable flash bit error															

Table 4: bit error corrected address

Register **Tnvs/Tnvh** (0x010)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 8 system clock cycles (1us, when FSYS is 8 MHz) 2 - 2*8 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 5: Tnvs/Tnvh

Register **Tnvh1** (0x012)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 8 system clock cycles (1us, when FSYS is 8 MHz) 2 - 2*8 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 6: Tnvh1

Register **Tpgs** (0x014)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 8 system clock cycles (1us, when FSYS is 8 MHz) 2 - 2*8 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 7: Tpgs

Register **Tpgh** (0x016)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 8 system clock cycles (1us, when FSYS is 8 MHz) 2 - 2*8 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 8: Tpgh

Register **Trcv** (0x018)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 8 system clock cycles (1us, when FSYS is 8 MHz) 2 - 2*8 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 9: Trcv

Register **Tprog** (0x01A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 8 system clock cycles (1us, when FSYS is 8 MHz) 2 - 2*8 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 10: Tprog

6.9.2 Terase / Tme

Register **Terase** (0x01C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 32000 system clock cycles (4096 us, when FSYS is 8 MHz) 2 - 2*32000 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 6.9.2.1: Terase

Register **Tme** (0x01E)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	time 0 or 1 - 32000 system clock cycles (4096 us, when FSYS is 8 MHz) 2 - 2*32000 system clock cycles ... this register can only be written, when mode is not "main block read"															

Table 6.9.2.2: Tme

6.10 I²C Interface

6.10.1 I²C Block Diagram

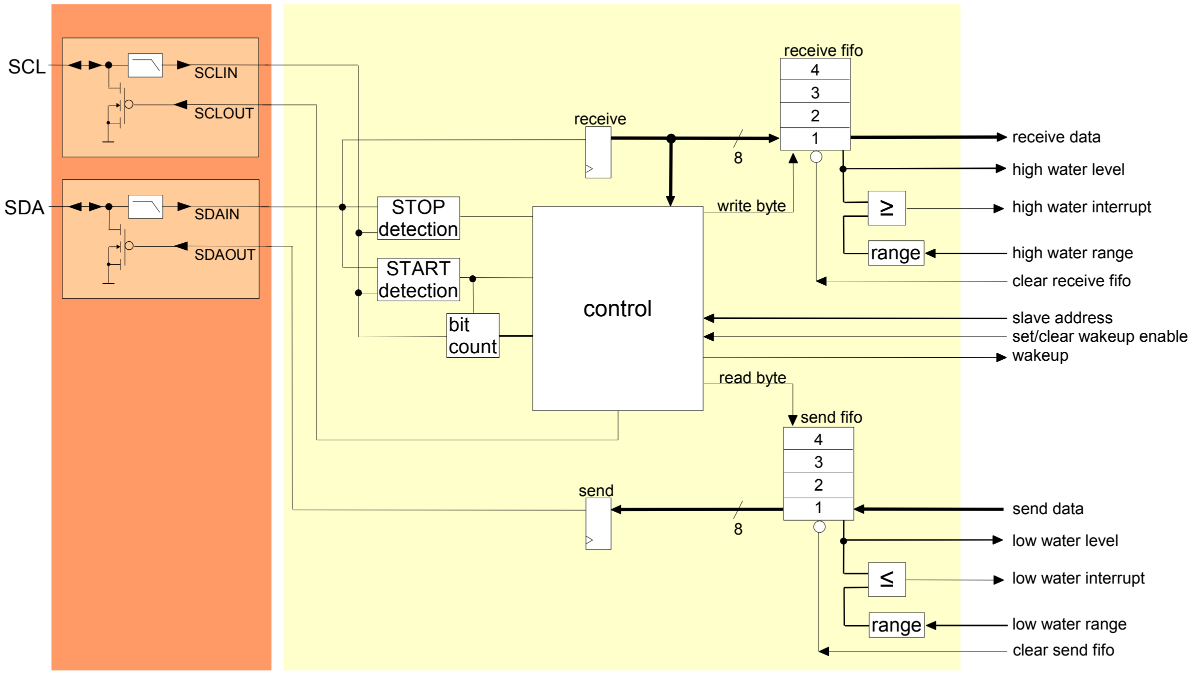


Figure 6.10.1-1 Block Diagram

6.10.2 I²C Function

The I²C slave interface operates in 7 bit addressing mode with a maximum frequency of 400 kHz (fast mode). To synchronize the ASIC to different operation voltages of the I²C bus the interface has a separate supply voltage input at pin V_{DDI} which is responsible for all interface pins. For more details of the addressing modes please refer to the "I²C – BUS SPECIFICATION VERSION 2.1" from Philips.

6.10.3 I²C Bus Timing Diagram

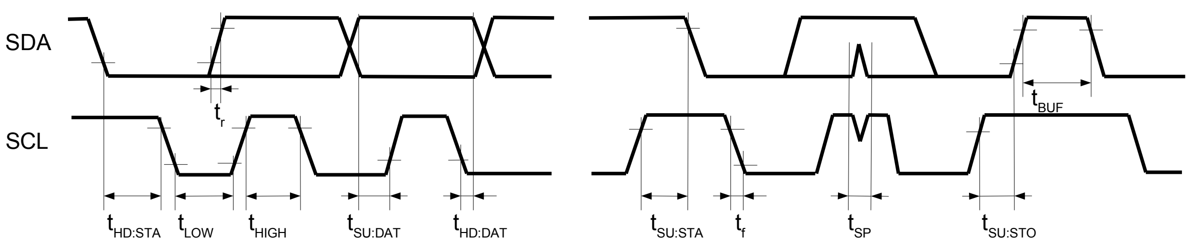


Figure 6.10.3-1 I²C Bus Timing Diagram

6.10.4 I²C Module Registers

address offset	reset value	register name	size
0x00	0x00	Receive data fifo register	8
0x02	0x00	Send data fifo register	8
0x04	0x0040	Control register	16
0x06	0x0000	Status register	16

Table 6.10.4.1: I²C Module Registers

6.10.5 Data FIFO Registers

Receive Data FIFO Registers

The data received from the master is stored in the receive fifo registers and has a depth of 4. The current fill level can be read in the status register. If the fifo is completely filled up and another byte should be received the interface will force the master into a wait state until the application software reads one byte from the fifo.

Register **Receive Data FIFO Register** (0x00)

Bit	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R
Bit Description	**7:0** : receive data (see Data FIFO Registers for details)							

Table 6.10.5.1: Receive Data FIFO Register

Send Registers:

The master reads data that is stored in the send fifo registers. This fifo buffer has a depth of 4 registers. The current fill level can be read in the status register. If the fifo is empty and a byte is requested by the master the interface will force the master into a wait state until the application software writes one byte to the fifo.

Register **Send Data FIFO Register** (0x02)

Bit	7	6	5	4	3	2	1	0
Reset value	-	-	-	-	-	-	-	-
Internal access	W	W	W	W	W	W	W	W
External access	W	W	W	W	W	W	W	W
Bit Description	**7:0** : send data (see Data FIFO Registers for details)							

Table 6.10.5.2: Send Data FIFO Register

6.10.6 Control Register

Register **Control Register** (0x04)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Internal access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W
External access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Description	 **15:14** reserved **13** : Clear contents of send FIFO registers 0 - read 1 - write **12** : Clear contents of receive FIFO registers 0 - read 1 - write **11** : Clear wake-up mode enable bit (see description below) 0 - read 1 - write **10** : Set wake-up mode enable bit (see description below) 0 - read 1 - write **9:8** : Slave address "00" - $58 (reset value) "01" - $59 "10" - $5A "11" - $5B **7:** reserved **6:4** : High water range for receive FIFO (range 0....4) **3:** reserved **2:0** : Low water range for send FIFO (range 0....4)																

Table 6.10.6.1 Configuration Register: I²C Control Register

6.10.7 Status Register

Register **Status Register** (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:9 reserved** **8** : Wake-up mode enable bit 0 - wake-up mode disabled 1 - wake-up mode enabled **7:** reserved **6:4** : Fill level of receive FIFO **3:** reserved **2:0** : Fill level of send FIFO															

Table 6.10.7.1 Configuration Register: I²C Status Register

6.10.8 Interrupt Handling

<u>I2C receive command</u> (see 6.11.2 List Of All Interrupts)

Command word pending in receive fifo, this means the next byte read from the receive fifo is the first received byte after the slave has been addressed. Depending on the application software this byte could be interpreted as a command. The interrupt flag is set back by reading a byte from the receive fifo. The master will force the interface into a wait state until the application software reads one byte from the fifo.

<u>I2C send request</u> (see 6.11.2 List Of All Interrupts)

This flag signalises that the master is requesting a byte but the send fifo is empty. The interrupt flag is set back by writing a byte to the send fifo. The master will force the interface into a wait state until the application software writes one byte to the fifo.
If this interrupt is not used for the communication protocol a default routine has to be implemented to clear the interrupt in case of unintentional appearance of this interrupt (the interrupt can occur under different circumstances when the slave address is enclosed in a data byte).
C-code example for default routine:

```
I2C_TXDATA = 0xff;          // fill "send data fifo register" (see above)
                            // with one byte of data to clear the interrupt
I2C_CTRL |= I2C_CLRTXFIFO;  // clear contents of send fifo registers to
                            // remove previous written 0xff (control reg.)
```

<u>I2C send fifo low water</u> (see 6.11.2 List Of All Interrupts)

In case the low water mark (defined in control register) is reached or is exceeded the send fifo low water flag becomes active. The flag is set back by filling to the send fifo.

<u>I2C receive fifo high water</u> (see 6.11.2 List Of All Interrupts)

If the high water mark (defined in control register) is reached or is exceeded the receive fifo high water flag becomes active. The flag is set back by reading from the receive fifo.

6.10.9 I²C Wake-up Detection

The I²C interface can be used to wake up the ASIC from any system state. In system state "off" the interface has to be configured to wake the CPU. Therefore the 'wakeup mode enable bit' has to be set (defined in control register) before setting the ASIC to "off-mode". It is only possible to set the 'wakeup mode enable bit' if the I²C Master has closed the communication on the bus, so the application software has to poll the bit 'wakeup mode enable' (defined in status register) after it was set to make sure the bus is in idle state and the ASIC can be set to "off-mode". After a new addressing of the slave on the bus the system will wake up from "off-mode" and the "I2C wakeup event" interrupt is active as long as the 'wakeup mode enable bit' is set back to zero (defined in control register). While the wake-up process the interface will force the Master into a wait state by holding the SCL line low. The application software has to clear the 'wakeup mode enable bit' (defined in control register) to release the SCL line in order to continue the communication.

6.11 Interrupt Control Module

6.11.1 Interrupt Control Module Structure

- interrupt pending bit flipflops (request hold elements) are located inside asserting modules
- interrupt vector support for more simple and faster interrupt entry
- nested interrupt support
- main interrupt enable MIE for easy cli() and sei() implementation
- N is the number of interrupt vectors

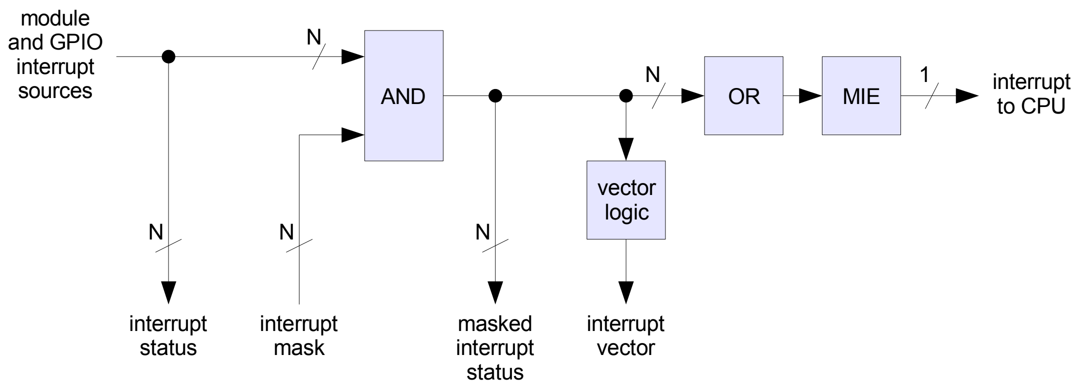


Figure 6.11.1-1: interrupt control circuit

6.11.2 List Of All Interrupts

vector number	interrupt source	priority
0	undefined opcode	highest
1	misaligned word access	
2	opcode execute protection error	
3	stack protection error	
4	invalid module register address access	
5	FLASH write error	
6	HALIOS measurement ready	
7	timer0 window error (watchdog)	
8	timer1 window error	
9	timer1 event	
10	I2C receive command	
11	I2C send request	
12	I2C send fifo low water	
13	I2C receive fifo high water	
14	SPI timeout	
15	SPI fifo error	
16	SPI receive high water	
17	SPI send low water	
18	GPIO rising	
19	GPIO falling	
20	I2C wakeup event	
21	wakeup timer wakeup event	
22	reserved	
23	reserved	
24	reserved	
25	reserved	
26	reserved	
27	reserved	
28	reserved	
29	reserved	
30	reserved	
31	reserved	lowest

Table 6.11.2.1: List Of All Interrupts

6.11.3 Interrupt Control Module Registers

address offset	reset value	register name	size
0x00	0x0000	interrupt mask	32
0x04	-	interrupt status	32
0x08	-	masked interrupt status	32
0x10	-	interrupt vector number	16
0x12	0x0000	interrupt routine address	16
0x14	0x0020	maximum interrupt level	16
0x16	0x0001	main interrupt enable	16

Table 6.11.3.1: Interrupt Control Module Registers

6.11.4 Interrupt Mask

Register **interrupt mask** (0x00)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**31:0** : mask (see List Of All Interrupts for details) 0 - disable 1 - enabled																															

Table 6.11.4.1: interrupt mask

6.11.5 Interrupt Status

Register **interrupt status** (0x04)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**31:0** : status (see List Of All Interrupts for details) 0 - not active 1 - active																															

Table 6.11.5.1: interrupt status

6.11.6 Masked Interrupt Status

Register **masked interrupt status** (0x08)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**31:0** : masked status (see List Of All Interrupts for details) 0 - not active 1 - active																															

Table 6.11.6.1: masked interrupt status

6.11.7 Interrupt Vector Number

Register **interrupt vector number** (0x10)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : number (see List Of All Interrupts for details) vector number of pending interrupt with highest priority (smallest vector number) when no interrupt is pending, vector will be 0xFFFF reset value: 0x0000															

Table 6.11.7.1: interrupt vector number

6.11.8 Interrupt Routine Address

Register **interrupt routine address** (0x12)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : address address of the software interrupt routine (is directly provided to the CPU for use as interrupt routine entry address and must be initialized by software before enabling interrupts)															

Table 6.11.8.1: interrupt routine address

6.11.9 Maximum Interrupt Level

Register **maximum interrupt level** (0x14)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**5:0** : level needed for nested interrupt support software writes current vector number to this register, so only interrupts with higher priority (lower vector number) can nest.															

Table 6.11.9.1: maximum interrupt level

6.11.9.1 Main Interrupt Enable

Register **main interrupt enable** (0x16)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W
Bit Description	MIE Main interrupt enable flag which can be used for easy implementation of cli() and sei() routines. Note: cli() usually must check (save current enable status) and then clear interrupt enable flag atomic (non interruptable). EL16 has no such operation, so GIE flag cannot be used. GIE should only be used for interrupt nesting. When MIE is only used inside cli() and sei(), cli() must not save current status, because MIE is always enabled on cli() entry.															

Table 6.11.9.1.1: main interrupt enable

6.12 Multiplier Module

The hardware multiplier is a peripheral and is not part of the EL16 CPU. This means, its activities do not interfere with the CPU activities. The multiplier registers are peripheral registers that are loaded and read with CPU instructions.
The hardware multiplier supports:

- Unsigned multiply
- Signed multiply
- Unsigned multiply accumulate
- Signed multiply accumulate
- 16 x 16 bits, 16 x 8 bits, 8 x 16 bits, 8 x 8 bits
- CPU is halted until result is valid (1 clock cycle)

The hardware multiplier supports unsigned multiply, signed multiply, unsigned multiply accumulate, and signed multiply accumulate operations. The type of operation is selected by the address the first operand is written to. The hardware multiplier has two 16-bit operand registers, OP1 and OP2, and three result registers, SumLo, SumHi, and SumExt. SumLo stores the low word of the result, SumHi stores the high word of the result, and SumExt stores information about the result.

6.12.1 Module Registers

address offset	reset value	register name	size
0x10	0x0000	MPY (operand 1)	16
0x12	0x0000	MPYS (operand 1)	16
0x14	0x0000	MAC (operand 1)	16
0x16	0x0000	MACS (operand 1)	16
0x18	0x0000	operand 2	16
0x1A	0x0000	SumLo	16
0x1C	0x0000	SumHi	16
0x1E	0x0000	SumExt	16

Table 6.12.1.1: Multiplier Module Registers

Register **MPY** (0x10)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 unsigned multiply															

Table 6.12.1.2: MPY

Register **MPYS** (0x12)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 signed multiply															

Table 6.12.1.3: MPYS

Register **MAC** (0x14)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 unsigned multiply accumulate															

Table 6.12.1.4: MAC

Register **MACS** (0x16)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 1 signed multiply accumulate															

Table 6.12.1.5: MACS

Register **Operand 2** (0x18)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Content	15:0															
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Rv	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : Operand 2 (write access starts multiplication)															

Table 6.12.1.6: Operand 2

Register **SumLo** (0x1A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : lower 16 bit of result															

Table 6.12.1.7: SumLo

Register **SumHi** (0x1C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : In case of operation: MPY: upper 16 bit of result MPYS: The MSB is the sign of the result. The remaining bits are the upper 15-bits of the result. Two's complement notation is used for the result. MAC: upper 16 bit of result MACS: Upper 16-bits of the result. Two's complement notation is used for the result.															

Table 6.12.1.8: SumHi

Register **SumExt** (0x1E)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**15:0** : In case of operation: MPY: always 0x0000 MPYS: contains the extended sign of the result 0x0000 if result was positive 0xFFFF if result was negative MAC: contains the carry of the result 0x0000 no carry result 0x0001 result with carry MPYS: contains the extended sign of the result 0x0000 if result was positive 0xFFFF if result was negative															

Table 6.12.1.9: SumExt

6.13 Timer0 (Window-Watchdog) Timer1

- two 32Bit width decrementing timers
- 32Bit little endian atomic read or write over 16Bit data bus
- timer 0 is used as watchdog, so it triggers a system reset instead of an interrupt
- timer reset window support

6.13.1 Module Registers

address offset	reset value	register name	size
0x00	0xFFFF.FFFF	timer value	32
0x04	0xFFFF.FFFF	timer counter	32
0x08	0x0000	timer control	16
0x0A	0x001F	timer window config	16
0x0C	-	timer interrupt clear	16

Table 6.13.1.1: Timer 0 and Timer 1 Module Registers

Register **timer value** (0x00)

Bit	**31**	**30**	**29**	**28**	**27**	**16**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**6**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**31:0** : timer start value																															

Table 6.13.1.2: timer value

Register **timer counter** (0x04)

Bit	**31**	**30**	**29**	**28**	**27**	**16**	**25**	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**6**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**31:0** : current timer value																															

Table 6.13.1.3: timer counter

Register **timer control** (0x08)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	(R) W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	(R) W	R/W	R/W
Bit Description	**15:8** : password must be written as 0xA5 will always be read as 0x96 **3** : clock base selector (timer 1 only) 0 - MCLK 1 – MCLK/(16*baud rate) synchronize timer to SPI clock **2** : timer reset 0 - no influence 1 - reset to start value **1** : loop 0 - run once and hold afterwards (clears "run enable") 1 - loop **0** : run enable 0 - timer stopped 1 - timer enabled															

Table 6.13.1.4: timer control

Register **timer window config** (0x0A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:8** : Timer Window Config (only applicable for window-watchdog) password must be written as 0xA5 will always be read as 0x96 **5** : window enable 0 - no window (default) 1 - window active **4:0** : window size reset window is defined as: timer value < (2^window size - 1)															

Table 6.13.1.5: timer window config

Register **timer interrupt clear** (0x0C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W
External access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W
Bit Description	**1** : timer IRQ clear 0 - no influence 1 - clear interrupt **0** : window IRQ clear 0 - no influence 1 - clear interrupt															

Table 6.13.1.6: timer interrupt clear

6.14 SPI Module

- can be used as master or salve
- the SPI Interface consists of the following 4 signals:
  - SCK: SPI clock (driven by master)
  - CSB: low active chip select (driven by master)
  - MISO: master in, slave out (data from slave to master)
  - MOSI: master out, slave in (data from master to slave)
- configurable phase, polarity and bit order
- byte and multi-byte transfer support
- slave mode SPI clock monitoring (time out)
- 4 data word transmit and receive FIFOs

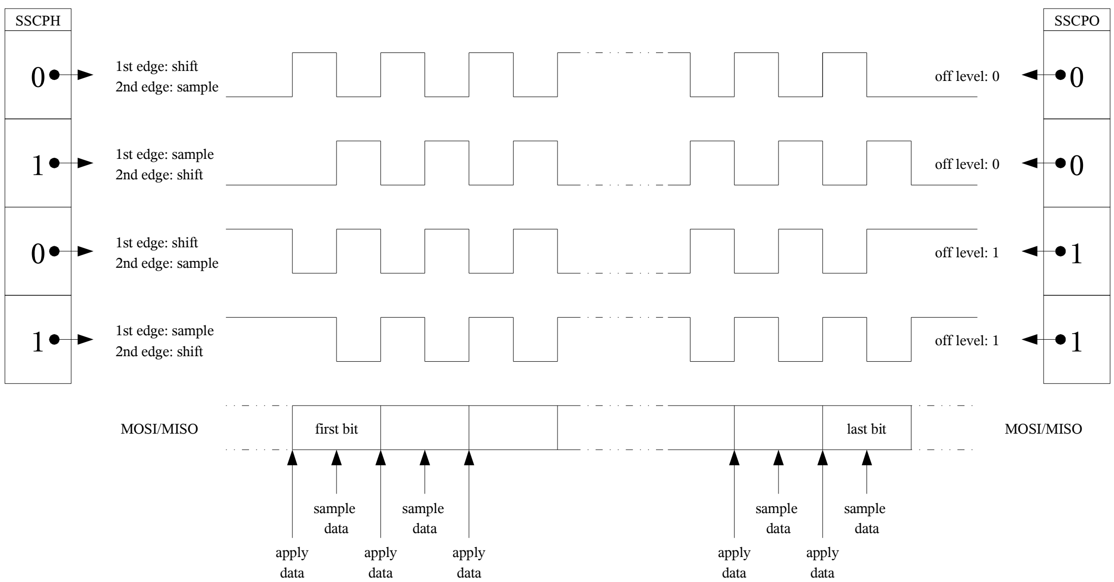


Figure 6.14-1: SPI timing diagram

6.14.1 SPI Module Registers

address offset	reset value	register name	size
0x00	0x0000	transmit data / receive data	16
0x02	0x2009	control	16
0x04	0x0000	baud config	16
0x06	0xFFFF	time out config	16
0x08	-	module reset	16
0x0A	-	status	16
0x0C	-	error	16
0x0E	-	interrupt clear	16

Table 6.14.1.1: SPI Module Registers

Register **transmit data / receive data** (0x00)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	(R) W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	(R) W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**8** : csb control (only for data transition and in master mode) 0 - byte mode 1 - keep csb active after related byte was transmitted **7:0** : transmit data / receive data The 'send low water' interrupt will be cleared by writing a byte to the transmit data register (FIFO). The 'receive high water' interrupt will be cleared by reading a byte from the receive data register (FIFO). (see List Of All Interrupts)															

Table 6.14.1.2: transmit data / receive data

Register **control** (0x02)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1
Internal access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
External access	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	**14:12** : high water receive FIFO level interrupt will be asserted when receive FIFO fill level increases to this value default value: 2 **10:8** : low water transmit FIFO level interrupt will be asserted when transmit FIFO fill level decreases to this value default value: 0 **3** : slave 0 - master 1 - slave **2** : polarity: SSCPO, see SPI mode diagram 0 - clock off level 0 1 - clock off level 1 **1** : phase: SSCPH, see SPI mode diagram 0 - 1st edge shift, 2nd edge sample 1 - 1st edge sample, 2nd edge shift **0** : order 0 - LSB first 1 - MSB first															

Table 6.14.1.3: control

Register **baud config** (0x04)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	Rv	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Description	**15:0** : baud divider = (system clock frequency) / (2 * baud rate) **NOTE:** Minimal value for baud divider is 4															

Table 6.14.1.4: baud config

Register **timeout config** (0x06)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**15:0** : timeout value maximum allowed count of system clock cycles between 2 SPI clock edges															

Table 6.14.1.5: timeout config

Register **module reset** (0x08)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W
External access	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W	W
Bit Description	**2** : SPI module reset **1** : receive FIFO clear **0** : transmit FIFO clear															

Table 6.14.1.6: module reset

Register **status** (0x0A)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**6:4** : receive FIFO level **2:0** : transmit FIFO level															

Table 6.14.1.7: status

Register **error** (0x0C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**1** : transmit FIFO was empty (only in slave mode) will be cleared on read **0** : receive FIFO was full (received data will be lost) will be cleared on read															

Table 6.14.1.8: error

Register **interrupt clear** (0x0E)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W
External access	-	-	-	-	-	-	-	-	-	-	-	-	-	-	W	W
Bit Description	**1** : clear error IRQ **0** : clear timeout IRQ															

Table 6.14.1.9: interrupt clear

6.15 GPIO Module

- up to 6 GPIOs
- interrupt capable (configurable for positive and / or negative signal edge interrupt)

6.15.1 GPIO Module Registers

address offset	reset value	register name	size
0x00	0x0000	output data	16
0x02	0x003F	direction	16
0x04	-	input data	16
0x06	0x0000	posedge interrupt enable	16
0x08	-	posedge interrupt status	16
0x0A	-	posedge interrupt clear	16
0x0C	0x0000	negedge interrupt enable	16
0x0E	-	negedge interrupt status	16
0x10	-	negedge interrupt clear	16
0x12	0x0000	port config	16

Table 6.15.1.1: GPIO Module Registers

Register **output data** (0x00)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : output data reset value: 0x0000															

Table 6.15.1.2: output data

Register **direction** (0x02)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : direction 0 - output, pull down disabled 1 - input, pull down enabled reset value: 0x00FF															

Table 6.15.1.3: direction

Register **input data** (0x04)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**7:0** : input data reset value: 0x0000															

Table 6.15.1.4: input data

Register **posedge interrupt enable** (0x06)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : enable 0 - disabled 1 - a positive edge on related "input data" bit will set interrupt bit reset value: 0x0000															

Table 6.15.1.5: posedge interrupt enable

Register **posedge interrupt status** (0x08)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**7:0** : status 0 - no interrupt 1 - interrupt was asserted reset value: 0x0000															

Table 6.15.1.6: posedge interrupt status

Register **posedge interrupt clear** (0x0A)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W
External access	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W
Bit Description	**7:0** : clear 0 - no influence 1 - clears related interrupt bit															

Table 6.15.1.7: posedge interrupt clear

Register **negedge interrupt enable** (0x0C)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**7:0** : enable 0 - disabled 1 - a negative edge on related "input data" bit will set interrupt bit reset value: 0x0000															

Table 6.15.1.8: negedge interrupt enable

Register **negedge interrupt status** (0x0E)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Bit Description	**7:0** : status 0 - no interrupt 1 - interrupt was asserted reset value: 0x0000															

Table 6.15.1.9: negedge interrupt status

Register **negedge interrupt clear** (0x10)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Internal access	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W
External access	-	-	-	-	-	-	-	-	W	W	W	W	W	W	W	W
Bit Description	**7:0** : clear 0 - no influence 1 - clears related interrupt bit															

Table 6.15.1.10: negedge interrupt clear

Register **port config** (0x12)

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Internal access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
External access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W
Bit Description	**1:0** : IO port config for details see IO Port Multiplexer reset value: 0x0000															

Table 6.15.1.11: port config

6.15.2 IO Port Multiplexer

IO Port	Test Mode	Normal Mode	
		cfg[0] = 0	*cfg[0] = 1*
TMODE	1	0	0
IO0	GPIO00	GPIO00	GPIO00
IO1	GPIO01	GPIO01	GPIO01
IO2	TDO	GPIO02	SCK
IO3	TDI	GPIO03	MISO
IO4	TMS	GPIO04	MOSI
IO5	TCK	GPIO05	CSB

Table 6.15.2.1: IO port multiplexer

- "port config" register (cfg) is located in GPIO module
- test mode default: pull down
- IO port default: GPIO input and pull down

7 Robustness

7.1 ESD

The ESD protection circuitry is measured according to AEC-Q100-002 with the following conditions:

Test Method (HBM):
- VIN = 2000 V (according to device class H1C)
- REXT = 1500 Ohm
- CEXT = 100 pF

Test Method (CDM):
- VIN = 500 V for all pins
- VIN = 750 V for corner pins

7.2 Latch up Test

Test Method:
- 100 mA positive and negative pulses at 85 °C according to AEC-Q100-004.

8 Package

8.1 Marking

8.1.1 Top side

ELMOS
E909.05A
XXX#LYWW*@

where

E / M / T	Volume production / prototype / test circuit
000.01	ELMOS project number
A	ELMOS project revision code
XXX	Production lot number
#	Assembler code
L	Production line code
YWW	Year and week of assembly
*	Mask revision code
@	ELMOS internal code

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