DC MOTOR 6 X HALF BRIDGE WITH SENSORLESS POSITIONING E910.72

ADVANCE PRODUCT INFORMATION - MAY 05, 2011

Features

- Operating supply voltage range 6V to 19V
- Tolerates automotive transients
- Standby current typ. 4µA
- 6 half bridges to drive 3, 4, or 5 DC motors
- $R_{DS,ON}$ of one half bridge typ. 1.25Ω
- Adjustable parameters to drive a high number of different motor types
- Output current max. 540mA per half bridge
- Three independent pulse detectors and counters
- Excellent positioning performance
- Minimum external components required
- SPI for communication with µC (5V or 3.3V)
- Diagnostic data via SPI (short circuit, open loop, overtemperature, over and undervoltage)
- AEC-Q100 qualified

Applications

- Automotive HVAC systems
- DC motor servo systems

General Description

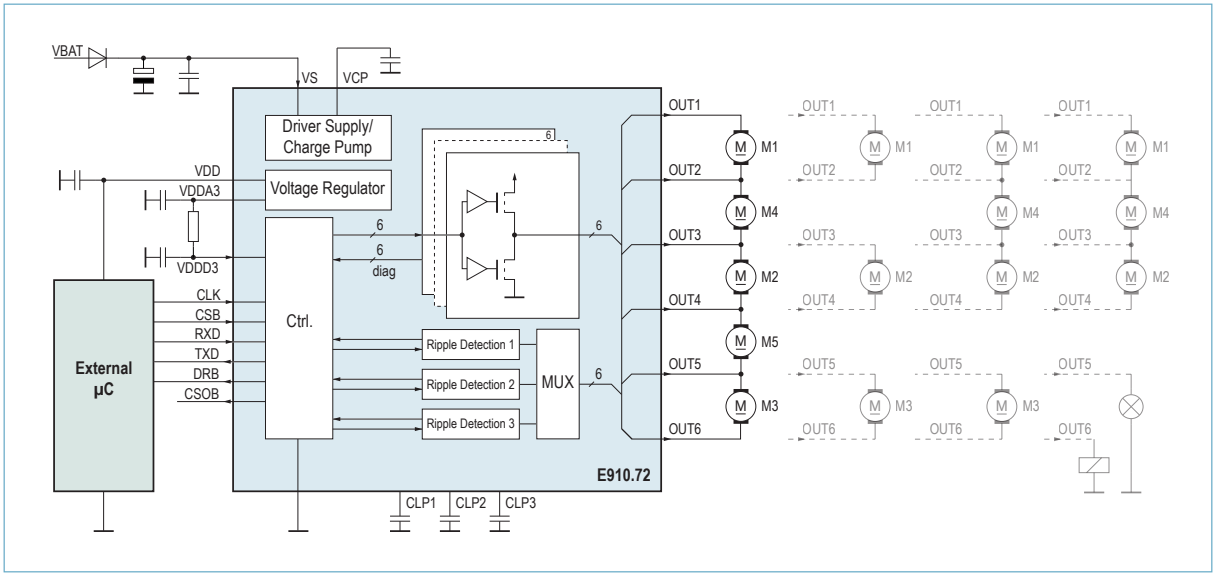
The E910.72 allows independent positioning of up to 5 DC motors. Pulse detection circuits convert the commutation current of the motors into countable digital signals especially for positioning of HVAC flap actuators.

Via an SPI a µC sends motor address, direction, and pulse count command to the device. The corresponding motor will then be driven to the desired position, and the actual number of counts is sent back to the µC.

Diagnostic data such as overcurrent, overtemperature and motor stall is also transmitted via the SPI. An open drain low side output indicates when a required motor position is reached or diagnostic data is available. ICs can be connected in a daisy chain.

Ordering Information

Product ID	Temp. Range	Package
E910.72	-40°C to +85°C	QFN32L5



This document contains information on a new product. ELMOS Semiconductor AG reserves the right to change specifications and information herein without notice.

1 Pinout

1.1 Pin Description

Pin	Name	Type [1)]	Description
1	CSOB	D_O	Chip Select Out Bar output / Daisy Chain output, active low
2	DRB	D_O	Data Ready Bar flag output, open drain, active low
3	TPIN	D_IO	Digital test input pin, to be connected to ground Scan enable signal In testmode the effective counts of the ripple detectors are visible at this pin.
4	TMODE	D_I	Test enable, to be connected to ground Input to enter test mode, when high
5	VDD	S	External 5V supply input
6	VSS	S	Ground connection for analog part
7	VDDD3	S	Supply input for digital part External 3.3V buffer capacitor or decoupling network to be connected
8	VDDA3	S	Internally regulated 3.3V supply output, supply input for analog part External 3.3V buffer capacitor to be connected
9	TANA	AD_IO	Test in/out analog, must not be connected It should be connected to external high-input-impedance buffer during testing.
10	CLP1	A_IO	Low pass filter capacitor for ripple detection 1
11	CLP2	A_IO	Low pass filter capacitor for ripple detection 2
12	CLP3	A_IO	Low pass filter capacitor for ripple detection 3
13	CCP_HV	HV_S	External charge pump capacitor
14	N.C./GND		No internal connection, to be connected to ground
15	VBAT_HV	HV_S	External battery voltage supply input for half bridge OUT1_HV
16	OUT1_HV	HV_A_O	Half bridge output OUT1_HV
17	PGND	S	Power ground connection for half bridges OUT1_HV and OUT2_HV
18	OUT2_HV	HV_A_O	Half bridge output OUT2_HV
19	VBAT_HV	HV_S	External battery voltage supply input for half bridges OUT2_HV and OUT3_HV
20	OUT3_HV	HV_A_O	Half bridge output OUT3_HV
21	PGND	S	Power ground connection for half bridges OUT3_HV and OUT4_HV
22	OUT4_HV	HV_A_O	Half bridge output OUT4_HV
23	VBAT_HV	HV_S	External battery voltage supply input for half bridges OUT4_HV and OUT5_HV
24	OUT5_HV	HV_A_O	Half bridge output OUT5_HV
25	PGND	S	Power ground connection for half bridges OUT5_HV and OUT6_HV
26	OUT6_HV	HV_A_O	Half bridge output OUT6_HV
27	VBAT_HV	HV_S	External battery voltage supply input for half bridge OUT6_HV
28	N.C./GND		No internal connection, to be connected to ground
29	CLK	D_I	Clock input of SPI
30	CSB	D_I	Chip Select Bar input, active low
31	RXD	D_I	Receive data input of SPI
32	TXD	D_O	Transmit data output of SPI

1) A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1.2 Pin Configuration

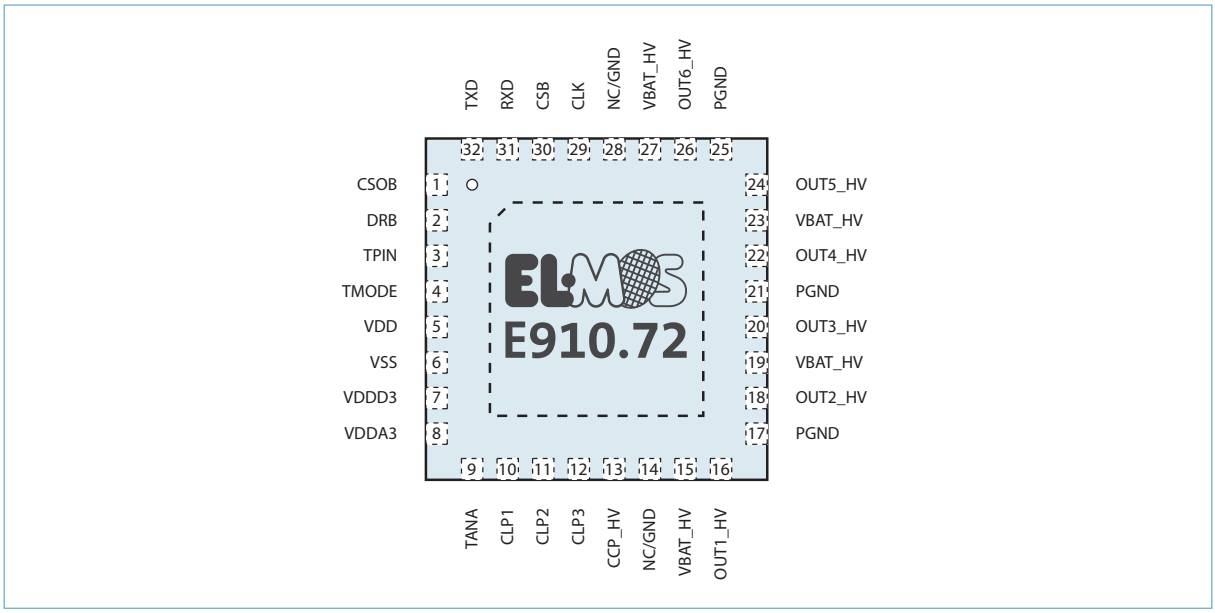


Figure 1: Package pinout. Top view

Note:

- It is mandatory to solder the exposed pad of the package to the PCB. Otherwise the thermal performance of the package will significantly be reduced as well as the mechanical integrity of the connections between package and PCB.

- Please refer to chapter "Maximum Ratings" for further information about thermal performance of a QFN package.

2 Block Diagram

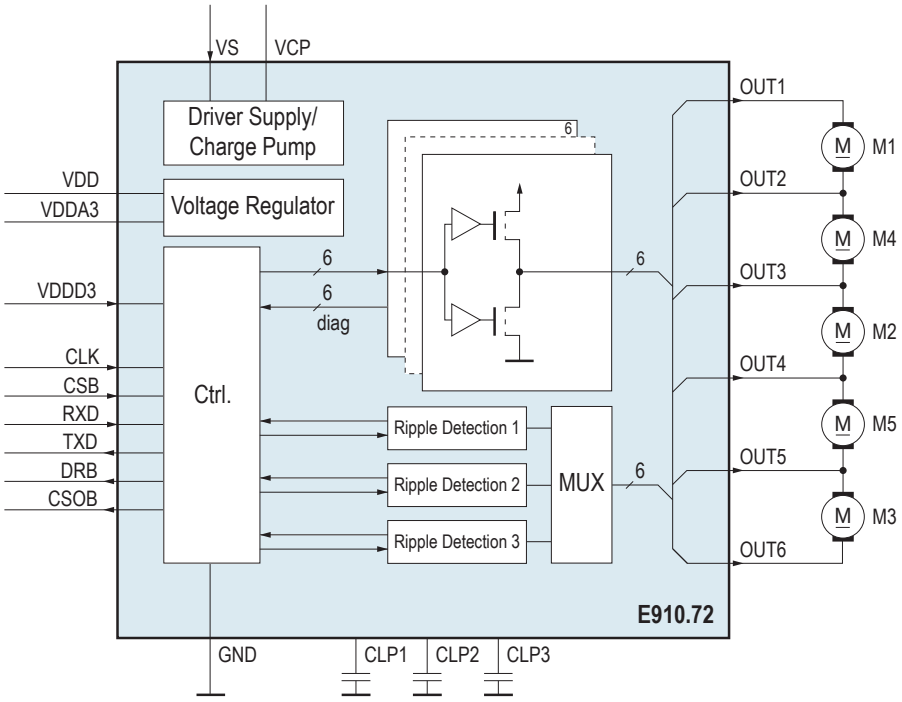


Figure 2: Block diagram

2.1 Recommended External Components

Pos.	Symbol	Function	Typ. value
1	C_{DD}	Bypass capacitor for 5.0V	100nF (20%)
2	C_{LP1}	Capacitance for low pass filter in ripple counter 1	47nF (20%)
3	C_{LP2}	Capacitance for low pass filter in ripple counter 2	47nF (20%)
4	C_{LP3}	Capacitance for low pass filter in ripple counter 3	47nF (20%)
5	C_{CCP}	Storage capacitor for charge pump	47nF (20%)
6	C_{B1}	Bypass capacitor for battery supply	100nF (20%)
7	C_{B2}	Buffer capacitor for battery supply	220µF (20%) or 470µF (20%)
8	D_1	Diode for reverse voltage protection, It is recommended to use a separate schottky diode for each E910.72 chip to achieve a small voltage drop. Please also refer to 5.3.2.	
9	R_{PU}	Pull up resistor for open drain pin DRB	10kΩ (20%) Min. 2.2kΩ Max. 100kΩ
10	C_{DDA3}	Buffer capacitance for analog supply	100nF (20%)
11	C_{DDD3}	Buffer capacitance for digital supply	100nF (20%)
12	R_F	Filter resistance between digital and analog supply	1Ω (10%)

3 Operating Conditions

3.1 Absolute Maximum Ratings

Operating the device at or beyond these limits may cause permanent damage.
All voltages are referred to ground (0V).
Currents flowing into the circuit have positive values.

No.	Symbol	Condition	Min.	Max.	Unit	Description
1	$V_{BAT\_HV, ABS}$		-0.3	28	V	Battery supply voltage
2	$V_{BAT\_HV, ABS}$	t500ms	-0.3	40	V	Battery supply voltage
3	$V_{DD, ABS}$		-0.3	5.5	V	5V supply voltage
4	$V_{DDD3, ABS}$		-0.3	3.6	V	3.3V digital supply voltage
5	$V_{DDA3, ABS}$		-0.3	3.6	V	3.3V analog supply voltage
6	$I_{DDA3, ABS}$		-20	20	mA	3.3V analog supply output current
7	$V_{HB, ABS}$		-0.3	V_{BAT_HV}+0.3	V	Output voltage of half bridges OUT1_HVOUT6_HV
8	$I_{HB, ABS}$	Output drivers in tristate mode t<100µs	-100	100	mA	Output current of half bridges OUT1_HV OUT6_HV
9	$V_{LVOUT, ABS}$		-0.3	V_{DD}+0.3	V	Output voltage of low voltage outputs TXD, CSOB, DRB
10	$I_{LVOUT, ABS}$		-5	5	mA	Output current of low voltage outputs TXD, CSOB, DRB
11	$V_{LVIN, ABS}$		-0.3	V_{DD}+0.3	V	Input voltage of low voltage inputs RXD, CSB, CLK, TMODE, TPIN
12	$I_{LVIN, ABS}$		-10	10	mA	Input current of low voltage inputs RXD, CSB, CLK, TMODE, TPIN
13	$V_{TANA, ABS}$		-0.3	V_{DDA3}+0.3	V	Voltage on test mode pin TANA
14	$V_{CLP, ABS}$		-0.3	V_{DDA3}+0.3	V	Voltage on low pass filter pins CLP1CLP3
15	$V_{CCP\_HV, ABS}$		-0.3	V_{BAT_HV}+10 or 40	V	Voltage on charge pump pin CCP_HV
16	$P_{DISS, ABS}$	T_{AMB}≤+85°C		1000	mW	Power dissipation
17	$R_{TJC, ABS}$	QFN32L5		5	K/W	Thermal resistance junction to case
18	$R_{TJAL, ABS}$	QFN32L5		80	K/W	Thermal resistance junction to ambient, low conductivity
19	$R_{TJAH, ABS}$	QFN32L5		32	K/W	Thermal resistance junction to ambient, high conductivity
20	$T_{J, ABS}$		-40	150	°C	Junction temperature
21	$T_{STG, ABS}$		-40	150	°C	Storage temperature

3.2 Recommended Operating Conditions

Parameters are guaranteed within the range of recommended operating conditions unless otherwise specified.
All voltages are referred to ground (0V).
Currents flowing into the circuit have positive values.
The first electrical potential connected to the IC must be GND. (If not specified specify timing sequence of electrical contacts.)

No.	Symbol	Condition	Min.	Typ.	Max.	Unit	Description
1	V_{BAT_HV}		6	12	19	V	Battery supply voltage
2	V_{DD}		4.5	5.0	5.5	V	5V supply voltage
3	T_{AMB}		-40	25	85	°C	Ambient operating temperature

4 Detailed Electrical Specification

4.1 Supply Section

No.	Symbol	Condition	Min.	Typ.	Max.	Unit	Description
Battery Supply DC Characteristics							
1	I_{BAT}	All outputs unloaded		0.42	3	mA	Operating supply current
2	$I_{BAT,STBY}$	V_{DD}=5.0V Software standby initiated by SPI command		4.0	20	uA	Standby current [1)]
3	$I_{BAT,PWROFF}$	V_{DD}=0.0V		4.0	20	uA	Power-off current [1)]
4	$V_{BAT,LOW}$		4.1	4.6	5.1	V	Undervoltage detection threshold
5	$V_{BAT,L,HYS}$			150		mV	Undervoltage detection hysteresis
6	$V_{BAT,HIGH}$		19	21.5	24	V	Overvoltage detection threshold
7	$V_{BAT,H,HYS}$			400		mV	Overvoltage detection hysteresis
Battery Supply AC Characteristics							
1	$T_{DEBVB,OV,OFF}$		7	10	18	ms	Overvoltage shut-off debounce time
2	$T_{DEBVB,OV,ON}$		7	10	18	ms	Turn-on debounce time after overvoltage shut-off
3	$T_{DEBVB,OV,OFF}$		7	10	18	ms	Undervoltage shut-off debounce time

1) Standby and power-off current are specified for a maximum junction temperature of +85°C, assuming that the IC's power dissipation is negligible in these operating modes, so that T_J=T_{AMB}.

No.	Symbol	Condition	Min.	Typ.	Max.	Unit	Description
Digital/Analog Supply							
1	I_{DD}			2	6	mA	Operating supply current at V_{DD}
2	$I_{DD,STBY}$	V_{DD}=5V Software standby initiated by SPI command		200		µA	Standby current at V_{DD} 1)
3	$V_{DD,LOW}$		2.3	2.6	2.9	V	Undervoltage reset
4	V_{DDA3}	I_{DDA3}=-10mA	3	3.3	3.6	V	VDDA3 regulator output voltage
Overtemperature Shut-Off							
1	T_{SO}	Referred to junction temperature	150			°C	Overtemperature shut-off threshold
2	T_{HYS}			20		°C	Overtemperature turn-on hysteresis
Serial Peripheral Interface, SPI DC Characteristics							
1	V_{IL}		0.0		1.5	V	Input low voltage Pins CLK, CSB, RXD
2	V_{IH}		V_{DD}-1		VDD	V	Input high voltage Pins CLK, CSB, RXD
3	R_{PD}	Tested at V_{IN}=V_{DD}		125		kΩ	Pulldown resistance Pins CLK, RXD
4	R_{PU}	Tested at V_{IN}=0.0V		125		kΩ	Pullup resistance Pin CSB
5	$V_{OUT,L}$	I_{OUT}=0.5mA V_{DD}=4.5V		0.3	0.5	V	Low output voltage Pins TXD, CSOB
6	$V_{OUT,H}$	I_{OUT}=-0.5mA V_{DD}=4.5V	V_{DD} (t.b.d.)-0.6	V_{DD}-0.4		V	High output voltage Pins TXD, CSOB
7	$V_{OUT,L}$	I_{OUT}=0.5mA V_{DD}=4.5V		0.3	0.5	V	Low output voltage Pin DRB (open drain)
8	I_{LEAK}	DRB not active	-2	0.0	+2	µA	Leakage current Pin DRB (open drain)
Serial Peripheral Interface, SPI AC Characteristics							
1	$t_{SPI,CLKPER}$		0.5		1000	µs	Clock period Pin CLK
2	t_{SL}				no limit	-	Slope time Pin CLK
3	$t_{SPI,CLKH}$		100	$t_{SPI,CLKPER}$/2	$t_{SPI,CLKPER}$ -100	ns	High time Pin CLK
4	t_{SL}				no limit	-	Slope time Pins CSB, RXD
5	$t_{SL,R}$	10%-90% C_L=10pF		15	30	ns	Output rising slope time Pins TXD, CSOB
6	$t_{SL,F}$	10%-90% C_L=10pF		15	30	ns	Output falling slope time Pins TXD, CSOB
7	$t_{SL,R,DRB}$	10%-90% C_L=10pF R_{PU}=10kΩ		250		ns	Output rising slope time Pin DRB

No.	Symbol	Condition	Min.	Typ.	Max.	Unit	Description
8	$t_{SL,F,DRB}$	10%-90% C_L=10pF R_{PU}=10kΩ		15	30	ns	Output falling slope time Pin DRB
9	$t_{SPI,SU}$		100	$t_{SPI,CLKPER}$/2		ns	Setup time RXD before rising CLK
10	$t_{SPI,HO}$		100	$t_{SPI,CLKPER}$/2		ns	Hold time RXD after rising CLK
11	$t_{SPI,CSB}$		100	$t_{SPI,CLKPER}$/2		ns	Time before and after clock cycles, when CSB must be active
12	$t_{SPI,TXDD}$				50	ns	Output delay of TXD after CLK and CSB
13	t_{RDY}		5	10	30	ms	Ready time when leaving standby mode for activating the charge pump
Motor Driver Half Bridges DC Characteristics							
1	$V_{IN,REV}$		-0.3		V_{BAT_HV} +0.3	V	Input voltage
2	$R_{ON,12}$	V_{BAT_HV}=12V $\|I_{OUTx}\|$=220mA		1.25	2.5	Ω	On resistance
3	$I_{LEAK,0}$	V_{OUTx_HV}=0V	-5	0	5	µA	Leakage current in tristate mode
4	$I_{LEAK,18}$	V_{BAT_HV}=18V V_{OUTx_HV}=18V		100		µA	Input current in tristate mode
5	$I_{LIM,H}$	V_{BAT_HV}=12V	-1200 (t.b.d.)	-800 (t.b.d.)	-550	mA	High side current limitation
6	$I_{LIM,L}$	V_{BAT_HV}=12V	550	800 (t.b.d.)	1200 (t.b.d.)	mA	Low side current limitation
Motor Driver Half Bridges AC Characteristics							
1	$d_{VON/dt}$	20%-80% V_{BAT} R_{LOAD}=50Ω to PGND	0.25	0.6	1.1	V/µs	Turn on slew rate
2	$d_{VOFF/dt}$	20%-80% V_{BAT} R_{LOAD}=50Ω to PGND	-1.1	-0.6	-0.25	V/µs	Turn off slew rate
3	$t_{SO,OC1}$			500		µs	Overcurrent shut-off debounce time
Positioning By Means Of Ripple Detection DC Characteristics							
1	I_{MOT}	Gain=11_b NonLin=01_b	-15		200	mA	Motor current input range
2	I_{MOT}	Gain=10_b NonLin=10	-23		320	mA	Motor current input range
3	I_{MOT}	Gain=01_b NonLin=11_b	-37		540	mA	Motor current input range
4	I_{MOT}	Gain=11_b NonLin=11_b	-15		540	mA	Motor current input range
5	I_{MOT}	Gain=10_b NonLin=11_b	-23		540	mA	Motor current input range
6	$I_{MOT,GT7P}$	Gain=11_b NonLin=01_b	2	10	30	mA	Open load detection threshold

No.	Symbol	Condition	Min.	Typ.	Max.	Unit	Description
Amplitude Threshold For Pulses To Be Detected By Pulse Detector							
1	$I_{DR,NEG}$	Gain=11_b NonLin=01_b PulseTh=011_b PulseT=010_b $I_{MOT,DC}$=10mA Max. t_{FALL}=20µs Min. $t_{PULSEWIDTH}$=150µs			1.8	mA	Threshold of negative current drop amplitude [1]
2	$I_{DR,NEG}$	Gain=10_b NonLin=10_b PulseTh=011_b PulseT=010_b $I_{MOT,DC}$=16mA Max. t_{FALL}=20µs Min. $t_{PULSEWIDTH}$=150µs			2.8	mA	Threshold of negative current drop amplitude [1]
3	$I_{DR,NEG}$	Gain=01_b NonLin=11_b PulseTh=011_b PulseT=010_b $I_{MOT,DC}$=27mA Max. t_{FALL}=20µs Min. $t_{PULSEWIDTH}$=150µs			4.3	mA	Threshold of negative current drop amplitude [1]
4	t_{PL}	PulseT=010_b		100		µs	Pulse width threshold for pulses to be detected [1]
Min. Peak-Peak-Value Threshold Of Sine Wave Signals To Be Detected By Sine Wave Detector							
1	$I_{SIN,PP}$	Gain=11_b NonLin=01_b $I_{MOT,DC}$=10mA f_{SIN}=70Hz			1.7	mA	Threshold of sinusoidal peak-peak current [2]
2	$I_{SIN,PP}$	Gain=10_b NonLin=10_b $I_{MOT,DC}$=16mA f_{SIN}=70Hz			2.4	mA	Threshold of sinusoidal peak-peak current [2]
3	$I_{SIN,PP}$	Gain=01_b NonLin=11_b $I_{MOT,DC}$=27mA f_{SIN}=70Hz			4	mA	Threshold of sinusoidal peak-peak current [2]

1) Pulse current variations above the maximum values are mandatory for a safe operation. The listed maximum values are detector threshold values of the respective conditions. Otherwise a functionality of the pulse detector could not be guaranteed by ELMOS.

2) Sinusoidal peak-peak current variations above the maximum values are mandatory for a safe operation. The listed maximum values are detector threshold values of the respective conditions. Otherwise a functionality of the sine detector could not be guaranteed by ELMOS.

No.	Symbol	Condition	Min.	Typ.	Max.	Unit	Description
Motor control timing							
1	$t_{OFF,AR}$	Switch drivers to tristate mode	70	100	160	ms	Turn off delay after last pulse
2	$t_{BR,STALL}$	Both low side transistors on	140	200	320	ma	Break delay after motor stall

5 Functional Description

5.1 Supply Section

The device is powered by two supply voltages, VBAT_HV and VDD. VBAT_HV is the battery voltage behind a reverse protection diode, and VDD is the digital 5.0V supply, also needed for several analog functions. Both voltages are monitored internally.

From the 5.0V VDD supply input, a 3.3V supply voltage is generated by an internal linear voltage regulator. The pin VDDA3 represents the output of the regulator and at the same the supply for the analog part of the IC. An external buffer capacitor CVDDA3 shall be connected to VDDA3. The pin VDDD3 represents the supply for the digital part of the IC and shall be connected to VDDA3 by an external decoupling network, consisting of a resistor RF and a second buffer capacitor CVDDD3.

For all outputs in motor control mode, in case of an overvoltage or undervoltage on VBAT_HV, all outputs are switched into brake mode (low side drivers on). Ripple detection is still performed as long as VDD is present. All outputs, which are driving other loads than motors, are only switched off in case of overvoltage.

When VDD drops below the low voltage threshold all outputs are switched to tristate (high impedance) mode to avoid destruction in case of a short circuit. The internal charge pump will be turned off, and the device draws only standby current IBAT,STBY from the VBAT_HV supply.

When VDD is present, a standby mode for both VBAT_HV and VDD can be activated via an SPI telegram (see chapter 5.2.17).

VBAT_HV and VDD may be turned on and off in any sequence.

5.2 Serial Peripheral Interface, SPI

5.2.1 Power-On Command Sequence Of The IC

After power-on, the IC starts in standby mode. The first commands sent to the E910.72 have to define the configuration register and read and acknowledge the diagnostic error data. Otherwise the E910.72 stays in "Hardware-Error" mode, i.e., signal DRB is pulled down. The idea is, that if the configuration registers become corrupt or reset (during normal operation), it will be indicated by low DRB due to "Hardware-Error" mode.

The activation can be done in the following scheme:

1.Send "Wake up and read status" command to leave the standby mode of the IC.
2.Wait the ready time t_{RDY} after leaving the standby to allow the charge pump to power up. During this time all commands are ignored. The IC enters the error mode "Command overflow", if commands other than "NOP" commands are sent to the IC during this time.
3.Write the two configuration registers with proper values. !!!
4.Read out hardware error ("Configuration register error").
5.Acknowledge the hardware error, i.e. acknowledge that the configuration registers were not okay. The DRB signal now goes high.
6.The IC is now properly activated and can receive further commands.
Please refer chapter 5.2.21 for example commands.

Data from and to the µC is transferred by means of an SPI. Received data is translated into switching commands for all half bridge outputs, and into positioning information, in case of motor control. A single data telegram from the µC may consist of 1 byte or 3 bytes. 1 byte information is used to turn an individual output on or off, 3 bytes information is necessary to move a motor into a defined direction with a given number of commutation ripples. To stop a motor which is still moving takes a 1 byte command as well.

As shown in Fig. 3, to start a data transmission the input signal CSB (Chip Select Bar) first has to be pulled low. Synchronised by a clock signal on CLK data is transferred into a shift register in the IC. The first bit of the data stream defines whether a 1 byte or a 3 byte information will be sent. After the appropriate number of bits has been received the shift register is stopped, and the output CSOB (Chip Select Out Bar) is pulled low, which can be seen at last falling edge of clock CLK. This signal can be used to activate the next IC in a daisy chain cascaded configuration. Again the first bit of the following data stream defines whether a 1 byte or a 3 byte information will be sent to the next IC.
Status data, position information of a motor that has been moved as well as hardware error information like overcurrent or overtemperature are available on output pin TXD. At the rising edge of clock CLK the data and TXD and RXD are valid and can be sampled. The bit transmission of TXD and RXD occurs simultaneously. The telegram length is defined by the leading bit no. 10 transferred to RXD and may be 1 byte or 3 bytes. The first byte carries diagnostic information while the second and third byte, in case of position mode, consist of motor address, direction and actual number of ripple pulses to be counted during motor movement. In case of an hardware error they contain overcurrent, overtemperature, voltage error or other diagnostic information.
Be aware, that the maximum possible request for motor position is 2047 (211-1). But in this case an overflow in the results appears, due to additional pulses in the brake phase of the motor. Therefore the maximum recommended request for motor position is 2037, supposing not more than 10 pulses in the brake mode.

Also be aware, that the minimum possible request for a motor position is 1. The value 0 for a motor drive command is not allowed.

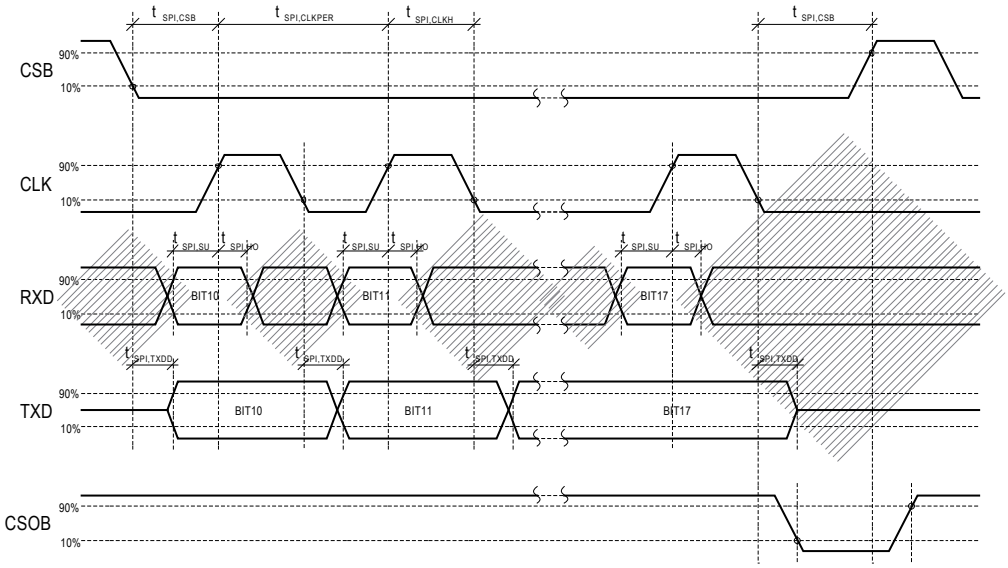


Figure 3: SPI timing for 1-byte transfer, transmission starts with CSB

Note: *On the rising edge of CLK, driven by µC, the transfer data RXD and TXD are valid and can be sampled.*

To read data from the IC without changing any output state the µC can send a telegram with the address 000b. The available data, with a length defined by the leading bit of the µC's telegram, will be output on pin TXD.

The output DRB "Data Ready Bar" indicates that data is available. It may be diagnostic information and/or position information of a motor after it has been stopped.

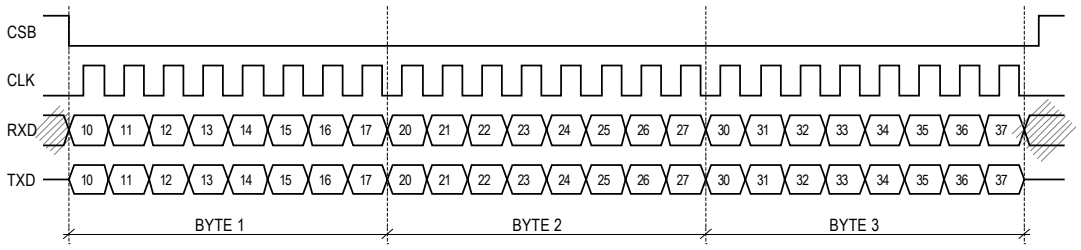


Figure 4: SPI timing for 1-byte transfer, transmission starts with CSB

Transmission in both directions starts with bit 10 and ends with bit 37.

5.2.2 Data Received From µC, Input RXD

Bit No.	Bit Name	Description
Byte No. 1 Of RXD Data In Case Of Direct Half Bridge Control [1)]		
10	Selection	0_b: Direct control of half bridges Length of telegram is 1 byte
11	SwitchStop	0_b: Output goes low 1_b: Output goes high
12	ErrPos	0_b: Position data of motor will be read in case of a 3 byte telegram 1_b: Hardware error will be read in case of a 3 byte telegram In case of a 1 byte telegram, the content of this bit does not care
13	Acknowledge	1_b: Reset either of error or position information, depending on bit 12
14	Address[2]	MSB of half bridge address
15	Address[1]	Second bit of half bridge address
16	Address[0]	LSB of half bridge address
17	Parity	Odd parity of first byte Content 00000000_b or 11111111_b leads to parity error
Byte No. 1 Of RXD Data In Case Of Direct Half Motor Control [2)]		
10	Selection	1_b: Motor control Length of telegram is 3 bytes if bit 11 is 0_b Length of telegram is 1 byte if bit 11 is 1_b
11	SwitchStop	1_b: Motor with the following address will be stopped, length of telegram is 1 byte
12	ErrPos	0_b: Position data of motor will be read in case of a 3 byte telegram 1_b: Hardware error will be read in case of a 3 byte telegram In case of a 1 byte telegram, the content of this bit does not care
13	Acknowledge	1_b: Reset either of error or position information, depending on bit 12
14	Address[2]	MSB of address of motor to be controlled. This address is independent of the motor adress to be read out in 5.2.12
15	Address[1]	Second bit of address of motor to be controlled. This address is independent of the motor adress to be read out in 5.2.12
16	Address[0]	LSB of address of motor to be controlled. This address is independent of the motor adress to be read out in 5.2.12
17	Parity	Odd parity of first byte Content 00000000_b or 11111111_b leads to parity error

1) Telegram ends after bit 17

2) Telegram ends after bit 17, if bit 11 is 1_b

Bit No.	Bit Name	Description
Bytes Nos. 2 And 3 Of RXD Data In Case Of Motor Control [3)]		
20	Direction	0_b: Half bridge with the lower number is switched to high level 1_b: Half bridge with the higher number is switched to high level
21	Position[10]	MSB of position command (2^{10})
22	Position[9]	2nd bit of position command (2^9)
23	Position[8]	3rd bit of position command (2^8)
24	Position[7]	4th bit of position command (2^7)
25	Position[6]	5th bit of position command (2^6)
26	Position[5]	6th bit of position command (2^5)
27	Parity	Odd parity of second byte Content 00000000b or 11111111b leads to parity error
30	Position[4]	7th bit of position command (2^4)
31	Position[3]	8th bit of position command (2^3)
32	Position[2]	9th bit of position command (2^2)
33	Position[1]	10th bit of position command (2^1)
34	Position[0]	LSB of position command (2^0)
35	reserved	
36	reserved	
37	Parity	Odd parity of third byte Content 00000000_b or 11111111_b leads to parity error
3 Bytes Configuration Register No. 1 [4)]		
10	Selection	1_b
11	SwitchStop	0_b
12	Write/Read	0_b: Configuration register is read by external µC 1_b: Configuration register is read and overwritten by external µC
13	Acknowledge	
14	Address[2]	1_b, MSB of address of configuration register no.1 (110_b)
15	Address[1]	1_b, second bit of address of configuration register no.1 (110_b)
16	Address[0]	0_b, LSB of address of configuration register no.1 (110_b)
17	Parity	Odd parity of first byte Content 00000000_b or 11111111_b leads to parity error
20	GainNorm[1]	MSB of gain of selected ripple counter(s) in normal mode
21	GainNorm[0]	LSB of gain of selected ripple counter(s) in normal mode
22	GainBreak[1]	MSB of gain of selected ripple counter(s) in break mode
23	GainBreak[0]	LSB of gain of selected ripple counter(s) in break mode
24	PulsThNorm[2]	MSB of pulse detector threshold of selected ripple counter(s) in normal mode
25	PulsThNorm[1]	Second bit of pulse detector threshold of selected ripple counter(s) in normal mode
26	PulsThNorm[0]	LSB of pulse detector threshold of selected ripple counter(s) in normal mode
27	Parity	Odd parity of second byte Content 00000000_b or 11111111_b leads to parity error
30	PulsThBreak[2]	MSB of pulse detector threshold of selected ripple counter(s) in break mode

3) Telegram ends after bit 37

4) Telegram ends after bit 37

Bit No.	Bit Name	Description
31	PulsThBreak[1]	Second bit of pulse detector threshold of selected ripple counter(s) in break mode
32	PulsThBreak[0]	LSB of pulse detector threshold of selected ripple counter(s) in break mode
33	reserved	
34	reserved	
35	MotorSel[1]	MSB of motor controller select bits 00_b: Configuration data valid for all motor control registers 01_b: Configuration data valid for motor control register no.1 10_b: Configuration data valid for motor control register no.2 11_b: Configuration data valid for motor control register no.3
36	MotorSel[0]	LSB of motor controller select bits
37	Parity	Odd parity of third byte Content 00000000_b or 11111111_b leads to parity error
3 Bytes Configuration Register No. 2 [5)]		
10	Selection	1_b
11	SwitchStop	0_b
12	Write/Read	0_b: Configuration register is read by external µC 1_b: Configuration register is read and overwritten by external µC
13	Acknowledge	
14	Address[2]	1_b, MSB of address of configuration register no.2 (111_b)
15	Address[1]	1_b, second bit of address of configuration register no.2 (111_b)
16	Address[0]	1_b, LSB of address of configuration register no.2 (111_b)
17	Parity	Odd parity of first byte Content 00000000_b or 11111111_b leads to parity error
20	NonLinNorm[1]	MSB of nonlinear shape function of selected ripple counter(s) in normal mode
21	NonLinNorm[0]	LSB of nonlinear shape function of selected ripple counter(s) in normal mode
22	NonLinBreak[1]	MSB of nonlinear shape function of selected ripple counter(s) in break mode
23	NonLinBreak[0]	LSB of nonlinear shape function of selected ripple counter(s) in break mode
24	PulsTNorm[2]	MSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in normal mode
25	PulsTNorm[1]	Second bit of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in normal mode
26	PulsTNorm[0]	LSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in normal mode
27	Parity	Odd parity of second byte Content 00000000_b or 11111111_b leads to parity error
30	PulsTBreak[2]	MSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in break mode
31	PulsTBreak[1]	Second bit of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in break mode
32	PulsTBreak[0]	LSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in break mode
33	reserved	
34	reserved	

5) Telegram ends after bit 37

Bit No.	Bit Name	Description
35	MotorSel[1]	MSB of motor controller select bits 00_b: Configuration data valid for all motor control registers 01_b: Configuration data valid for motor control register no.1 10_b: Configuration data valid for motor control register no.2 11_b: Configuration data valid for motor control register no.3
36	MotorSel[0]	LSB of motor controller select bits
37	Parity	Odd parity of third byte Content 00000000_b or 11111111_b leads to parity error

Address Bits	SwitchStop Bit	Selection Bit = 0_b (Direct Half Bridge Control)	Selection Bit = 1_b (Motor Control)
Address Correlation [6]			
001_b	0_b	OUT1_HV = Low	Motor 1 (OUT1_HV - OUT2_HV)
001_b	1_b	OUT1_HV = High	Stop motor 1
010_b	0_b	OUT2_HV = Low	Motor 2 (OUT3_HV - OUT4_HV)
010_b	1_b	OUT2_HV = High	Stop motor 2
011_b	0_b	OUT3_HV = Low	Motor 3 (OUT5_HV - OUT6_HV)
011_b	1_b	OUT3_HV = High	Stop motor 3
100_b	0_b	OUT4_HV = Low	Motor 4 (OUT2_HV - OUT3_HV)
100_b	1_b	OUT4_HV = High	Stop motor 4
101_b	0_b	OUT5_HV = Low	Motor 5 (OUT4_HV - OUT5_HV)
101_b	1_b	OUT5_HV = High	Stop motor 5
110_b	0_b	OUT6_HV = Low	Configuration register no.1
110_b	1_b	OUT6_HV = High	Invalid address, no reaction
111_b	0_b	Standby mode	Configuration register no.2
111_b	1_b	Software reset	Software reset

6) Address 000_b can be used to read data back from TXD without changing the state of any output or to wake up the IC.

5.2.3 Data Telegram Supervision

If the result of any of the parity checks is incorrect the complete telegram is ignored, and DRB gets activated.

The clock input CLK is checked during CSB low time for a minimum frequency of 1 kHz. In case the frequency is lower, the data is ignored and DRB gets activated. For supervision in standby mode, the oscillator is switched on after a falling edge on CSB and the supervision gets started. The first detection period is prolonged by the settling time of internal references, which causes a start up time of the oscillator in the range of a few 100µs.

Short pulses of CSB without any SPI clock CLK are not interpreted as invalid data, DRB does not go low. During the short pulse, the internal oscillator is switched on. If CSB goes high, the oscillator is switched off and the IC stays in standby mode.

5.2.4 Simultaneous And/Or Sequential Motor Control

5 different configurations are possible using all 6 half bridges for motor control:

1. Motor configuration MOT123: Motors 1, 2 and 3 are connected to OUT1/2, OUT3/4 and OUT5/6, respectively. All motors can be driven independently and simultaneously, no precautions to be taken in the µC.
2. Motor configuration MOT12345: Motors 1 through 5 are connected to OUT1/2, OUT3/4, OUT5/6, OUT2/3 and OUT4/5, respectively. All motors can only be driven sequentially.
3. Motor configuration MOT1234: Motors 1,2 and 5 are connected to OUT1/2, OUT3/4 and OUT2/3, respectively. Motor 3 is connected to OUT5/6. Motor 3 can be driven independently of all others, only one of motors 1, 2 and 4 can run at a time.
4. Motor configuration MOT1235: Motor 1 is connected to OUT1/2, motors 2, 3, and 5 are connected to OUT3/4, OUT5/6, and OUT4/5, respectively. Motor 1 can be driven independently of all others, only one of motors 2, 3, and 5 can run at a time. This configuration is functionally comparable to the motor configuration MOT1234.
5. Motor configuration MOT1345: Motors 1 and 4 are connected to OUT1/2 and OUT 2/3. Motors 3 and 5 are connected to OUT5/6 and OUT4/5, respectively. In case of this motor configuration the E910.72 supports two motor groups. The motors of that groups only allowed to be operate sequentially. In a synchronous mode a crosswise configuration (M1 combined with M3/M5 or M3 combined with M1/M4) has to be selected. An operation of motors M4 and M5 at the same time is not supported.

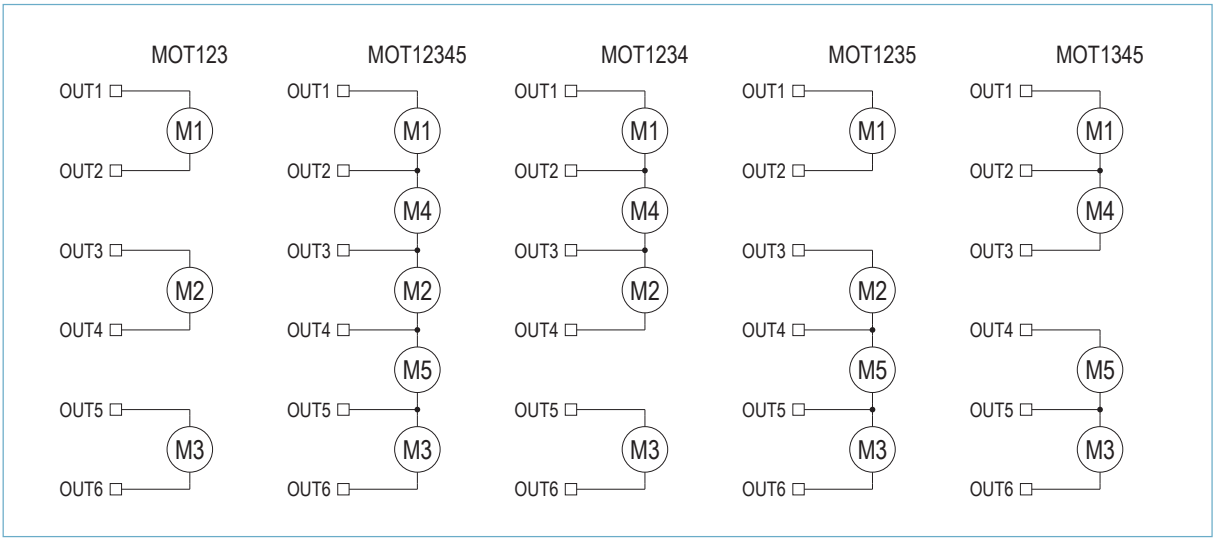


Figure 5: DC motor configuration overview

If any of the motors can only be driven sequentially this has to be considered by the µC software. This is an easy task when the configuration of motors is known. The DRB flag is set when a motor has reached its required position or diagnostic data is available. So the next one may be addressed only after the motor has come to a stop.

5.2.5 Selection Bit 10, Combination Of Motor Control And Half Bridge Control

All half bridge outputs, that have been directly addressed once by setting the "Selection" bit to 0_b, will stay in this direct access mode. Thus they will not be switched to tristate mode regardless of any motor control command.

The status will change when the same half bridge gets addressed by a motor control command. Status change works in both directions, the last valid command defines whether the half bridge output is under direct access or is part of a motor driver.

5.2.6 Motor Stop Bit

The "SwitchStop" bit allows halting a motor before it has reached its final position. The motor will be stopped after the next ripple has been detected (or timeout has been expired in case of motor stall). Pulses will be counted during braking, as in any normal case, and after no ripples have been detected for 100ms, DRB will be activated and the actual position is available via SPI.

No position command has to be transferred when bit 11 is set to 1_b, so the length of the data telegram is reduced to 1 byte.

5.2.7 Gain Bits

The gain bits GainNorm[1:0] or GainBreak[1:0], respectively, are used to match the input amplifier's gain with the motors connected to the IC independently for normal mode and for break mode:

Gain[1:0]	Gain Configuration	Motor Type
Gain bits encoding		
00_b	Low gain	Motor with less than 540mA maximum stall current
01_b	Low gain	Motor with less than 540mA maximum stall current
10_b	Medium gain	Motor with less than 320mA maximum stall current
11_b	High gain	Motor with less than 200mA maximum stall current

5.2.8 Pulse threshold bits

The pulse threshold bits PulsThNorm[2:0] or PulsThBreak[2:0], respectively, control the threshold voltage of the pulse detector independently for normal mode and for break mode. The threshold can be varied according to the following table:

PulsTh[2:0]	Pulse Threshold In %
Pulse Threshold Bits Encoding	
000_b	56%
001_b	70%
010_b	83%
011_b	100%
100_b	130%
101_b	170%
110_b	220%
111_b	280%

5.2.9 Pulse Length Bits

With the pulse length bits PulsTNorm[2:0] or PulsTBreak[2:0], respectively, the minimum pulse length t_{PL} of a pulse to be detected by the pulse detector can be controlled independently for normal mode and for break mode. Pulses with a shorter length are suppressed.

PulseT[2:0]	Typical Pulse Length t_{PL}
Pulse Length Bits Encoding	
000_b	60µs
001_b	80µs
010_b	100µs
01_b	120µs
100_b	140µs
101_b	160µs
110_b	180µs
111_b	Counter disabled

5.2.10 Nonlinearity Shape Function Of Nonlinear Amplifier

The nonlinear function of the input amplifier can be influenced by two bits NonLinNorm[1:0] or NonLinBreak[1:0], respectively, independently for normal mode and for break mode. The nominal value is 01_b for typical motors. With code 10_b motor current signals can amplified with one higher gain level than usual. With code 11_b motor current signals can amplified with two higher gain levels than usual, without going into saturation. With code 00_b the non-linearity is reduced.

NonLin[1:0]	Influence On Nonlinearity
Nonlinearity Bits Encoding	
00_b	Weak nonlinearity
01_b	Normal shape
10_b	Higher nonlinearity
11_b	Highest nonlinearity

5.2.11 Recommended Configuration For Different Type Of DC Motors

The following table shows the recommended configuration for different 12V DC motor types for flap control.

Parameter	Config. Bits	Asymmetrical Motor	Symmetrical Motor, High Current	Symmetrical Motor, Low Current
Recommended Configurations				
Gain in normal mode	GainNorm[1:0]	01_b	01_b	11_b
Gain in break mode	GainBreak[1:0]	11_b	10_b	11_b
Nonlinearity in normal mode	NonLinNorm[1:0]	01_b	01_b	01_b
Nonlinearity in break mode	NonLinBreak[1:0]	11_b	10_b	01_b
Pulse threshold in normal mode	PulseThNorm[2:0]	110_b	110_b	101_b
Pulse threshold in break mode	PulseThBreak2:0]	100_b	011_b	101_b
Pulse length in normal mode	PulseTNorm[2:0]	010_b	010_b	010_b
Pulse length in break mode	PulseTBreak[2:0]	010_b	010_b	010_b

Note: *The best configuration for a specific motor has to be proven by tests. Motors (including gearing) are not recommended, if they are turning for themself, when not driven, e.g. turning backward after breaking and surpassing a commutation point.IC.*

5.2.12 Data Sent To µC, Output TXD

The following table shows the recommended configuration for different 12V DC motor types for flap control.

Bit No.	Bit Name	Description
Byte No. 1 Of TXD Data		
10	InvalidData	1_b: Last data telegram from µC has been ignored due to parity error or f_{CLK} < 1kHz or CSB going high before the expected end of telegram
11	reserved	0_b
12	Busy	1_b: IC is not able to receive new data. Usually this bit is high for a period of typically 6µs after a command has been sent. This bit can be polled from the external µC.
13	CommandOverflow	1_b: At least one command which has been sent from the µC is ignored. This can happen, when - the bit Busy is active, while the command has been sent - a motor is running, while the motor controller receives a new command - a count value is not read and acknowledged by the µC before a new command is sent - a half bridge receives a direct command, while it is being used to drive a motor
14	HardwareError	1_b: Some hardware error has occurred, such as over-current or overtemperature
15	PositionData	1_b: Positioning data is available for reading out
16	reserved	0_b
17	Parity	Odd parity of first byte Content 00000000_b or 11111111_b leads to parity error

Bit No.	Bit Name	Description
Bytes Nos. 2 And 3 Of TXD Data When Reading Motor Position Counter		
20	Address[2]	MSB of address of motor to be read out
21	Address[1]	Second bit of address of motor to be read out
22	Address[0]	LSB of address of motor to be read out
23	MotorStall	Unexpected stop of motor due to stall condition
24	Position[10]	MSB of motor position counter (2^{10})
25	Position[9]	2nd bit of motor position counter (2^9)
26	Position[8]	3rd bit of motor position counter (2^8)
27	Position[7]	4th bit of motor position counter (2^7)
30	Position[6]	5th bit of motor position counter (2^6)
31	Position[5]	6th bit of motor position counter (2^5)
32	Position[4]	7th bit of motor position counter (2^4)
33	Position[3]	8th bit of motor position counter (2^3)
34	Position[2]	9th bit of motor position counter (2^2)
35	Position[1]	10th bit of motor position counter (2^1)
36	Position[0]	LSB of motor position counter (2^0)
37	Parity	Odd parity of second and third byte Content 0000_{hex} or $FFFF_{hex}$ leads to parity error
Bytes Nos. 2 And 3 Of TXD Data When Reading Hardware Error		
20	OverCurrent[5]	1_b: OUT6 has been switched off due to overcurrent
21	OverCurrent[4]	1_b: OUT5 has been switched off due to overcurrent
22	OverCurrent[3]	1_b: OUT4 has been switched off due to overcurrent
23	OverCurrent[2]	1_b: OUT3 has been switched off due to overcurrent
24	OverCurrent[1]	1_b: OUT2 has been switched off due to overcurrent
25	OverCurrent[0]	1_b: OUT1 has been switched off due to overcurrent
26	OverTemperature	1_b: All OUTx pins have been switched into tristate due to overtemperature
27	UnderVBAT_HV	1_b: All motors are stopped due to overvoltage of VBAT_HV and the count values are stored
30	OverVBAT_HV	1_b: All motors are stopped due to undervoltage of VBAT_HV and the count values are stored
31	OpenLoop	1_b: At least one pin OUTx is not connected externally, floating
32	Configuration-RegisterError	1_b: The configuration register is not or is badly initialised or it is corrupted due to external distortions
33	reserved	0_b
34	reserved	0_b
35	reserved	0_b
36	reserved	0_b
37	Parity	Odd parity of second and third byte Content 0000_{hex} or $FFFF_{hex}$ leads to parity error

Bit No.	Bit Name	Description
Bytes Nos. 2 And 3 Of TXD Data When Reading Configuration Register No. 1		
20	GainNorm[1]	MSB of gain of selected ripple counter(s) in normal mode
21	GainNorm[0]	LSB of gain of selected ripple counter(s) in normal mode
22	GainBreak[1]	MSB of gain of selected ripple counter(s) in break mode
23	GainBreak[0]	LSB of gain of selected ripple counter(s) in break mode
24	PulsThNorm[2]	MSB of pulse detector threshold of selected ripple counter(s) in normal mode
25	PulsThNorm[1]	Second bit of pulse detector threshold of selected ripple counter(s) in normal mode
26	PulsThNorm[0]	LSB of pulse detector threshold of selected ripple counter(s) in normal mode
27	reserved	0_b
30	PulsThBreak[2]	MSB of pulse detector threshold of selected ripple counter(s) in break mode
31	PulsThBreak[1]	Second bit of pulse detector threshold of selected ripple counter(s) in break mode
32	PulsThBreak[0]	LSB of pulse detector threshold of selected ripple counter(s) in break mode
33	reserved	0_b
34	reserved	0_b
35	MotorSel[1]	Origin of the configuration data: Upon each readout of this configuration register no.1 there is an increment of the motor select bits. If there was a writing to a motor controller, the readout address is set to this motor controller register. If there was a writing to motor controller 0 (writing to all motor controllers) the readout address is set to 0, too. This indicates that all motor controller have the same setting for configuration register 1.
36	MotorSel[0]	Origin of the configuration data
37	Parity	Odd parity of second and third byte Content 0000_{hex} or $FFFF_{hex}$ leads to parity error
Bytes Nos. 2 And 3 Of TXD Data When Reading Configuration Register No. 2		
20	NonLinNorm[1]	MSB of nonlinear shape function of selected ripple counter(s) in normal mode
21	NonLinNorm[0]	LSB of nonlinear shape function of selected ripple counter(s) in normal mode
22	NonLinBreak[1]	MSB of nonlinear shape function of selected ripple counter(s) in break mode
23	NonLinBreak[0]	LSB of nonlinear shape function of selected ripple counter(s) in break mode
24	PulsTNorm[2]	MSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in normal mode
25	PulsTNorm[1]	Second bit of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in normal mode
26	PulsTNorm[0]	LSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in normal mode
27	reserved	0_b
30	PulsTBreak[2]	MSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in break mode
31	PulsTBreak[1]	Second bit of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in break mode
32	PulsTBreak[0]	LSB of minimum pulse width to be detected as regular pulse of selected ripple counter(s) in break mode
33	reserved	0_b
34	reserved	0_b

Bit No.	Bit Name	Description
35	MotorSel[1]	Origin of the configuration data: Upon each readout of this configuration register no.2 there is an increment of the motor select bits. If there was a writing to a motor controller, the readout address is set to this motor controller register. If there was a writing to motor controller 0 (writing to all motor controllers) the readout adress is set to 0, too. This indicates that all motor controller have the same setting for configuration register 2.
36	MotorSel[0]	Origin of the configuration data
37	Parity	Odd parity of second and third byte Content 0000_{hex} or $FFFF_{hex}$ leads to parity error

5.2.13 Overtemperature Shut-Off

When overtemperature is detected, all half bridge outputs will be turned into tristate, and the Data Ready flag is set (output DRB goes low). As an indication, the overtemperature bit of byte no. 2 in hardware error mode is set to 1_b.

5.2.14 Over/Undervoltage Shut-Off

In case of overvoltage or undervoltage a moving motor is stopped, the currently counted number of ripples is stored, and the DRB flag is set. Outputs in half bridge control mode switch on again automatically after the power supply has gone back into normal operating range. No diagnostic information will be generated.

5.2.15 Open Load Detection

Open load detection in motor control mode is performed by the internal current threshold IMOT,GT7P in combination with the stall detection. When the half bridges to drive the motor are turned on, but no ripple pulses are detected for 200ms, this usually means that the motor is stalled. Motor current thus should be stall current. If in this case the motor current is lower than IMOT,GT7P threshold mentioned above, the interpretation is "Open Load".

5.2.16 Output DRB, Acknowledge Of Positioning And Diagnostic Data

The Data Ready Output pin DRB goes low whenever a required motor position is reached or diagnostic data is available. DRB is reset after the complete set of data has been transmitted via TXD, simultaneously with a valid data telegram received at the input RXD.

There are several conditions under which it is not possible to transmit data completely:
Positioning data of more than 1 motor is available
Positioning data is available, but received data telegram is only 1 byte long (Bit 10 is 0_b, bit 11 is 1_b)
New data has become valid after CSB has gone low and transmission has started
Received data telegram has been detected to be corrupted.
One or more of the configuration registers is badly/not initialised or corrupted.

In any of these cases DRB stays active (low) until data is completely transferred.

Positioning data and diagnostic data are reset if they have been successfully transferred to the µC and have been acknowledged by the µC. Acknowledge is performed by setting the Acknowledge bit (no. 13) to 1_b.
Pending error conditions like overtemperature prevent resetting of DRB signal even after acknowledge.
If a command is sent from the µC to activate an output that has been shut off, but diagnostic data has not yet been acknowledged, the command will be ignored and DRB is activated again. It is possible to reactivate any output OUTx with the same telegram that contains the acknowledge.

5.2.17 Standby Mode

Sending standby command to the IC switches the device into standby mode. All half bridge outputs are turned into tristate mode, charge pump and oscillator are switched off, and current consumption in the VBAT_HV supply is reduced to a value of $I_{BAT,STBY}$. The internal voltage regulator on VDD, which supplies the digital part, stays active and consumes a standby current IDD,STBY.
Sending a standby command while a motor is running sets the motor into break mode, i.e. both low side drivers are turned on. Ripples are counted until the motor has stopped, and DRB becomes zero. After a timeout of 100ms standby mode is activated, if in the meantime the µC did not initialise any other activity.
It takes a data telegram other than the standby or soft reset command to get back to normal operation. A delay of t_{RDY} is realised to allow the charge pump to power up before any output is activated.
After leaving the standby mode all half bridges stay in tristate mode, unless they get a activating command from the µC.
After power on, the IC starts in standby mode.

5.2.18 Software Reset

The µC can reset all registers of the chip by sending a Software Reset command. It contains address 111_b and Switch bit 1_b in a half bridge control telegram. The decoder is hard-wired and generates a reset signal for all registers. Reset signal remains until the next rising edge of CSB.
A software reset has the same effect as a power on reset due to the fact that both reset methods trigger the same reset generator (see. chapter 5.2.1).

5.2.19 Acknowledge

All data (diagnostic information or position data) indicated by an active DRB output have to be acknowledged by the µC. The IC stores the information, and even though the over-current or overtemperature condition may no longer be present, all data is available until reset by acknowledge.
Acknowledging the position of a motor allows the µC to send new positioning data for the same motor with the same SPI protocol.
If there is no position data available in the IC, in the case of a data transmission to the µC the address is 000_b and the position data is undefined (random).

5.2.20 Daisy Chain Configuration

Several ripple counter ICs can be connected in daisy chain configuration as shown in Fig. 6. Daisy chain is used to increase the number of available half bridge to control more than five motors.
In fact only the chip select signal CSB is connected in daisy chain configuration. All other signal are connected in parallel to all ICs and the µC. The data ready signal DRB is connected wired-or with an external pullup resistor R_{PU}.

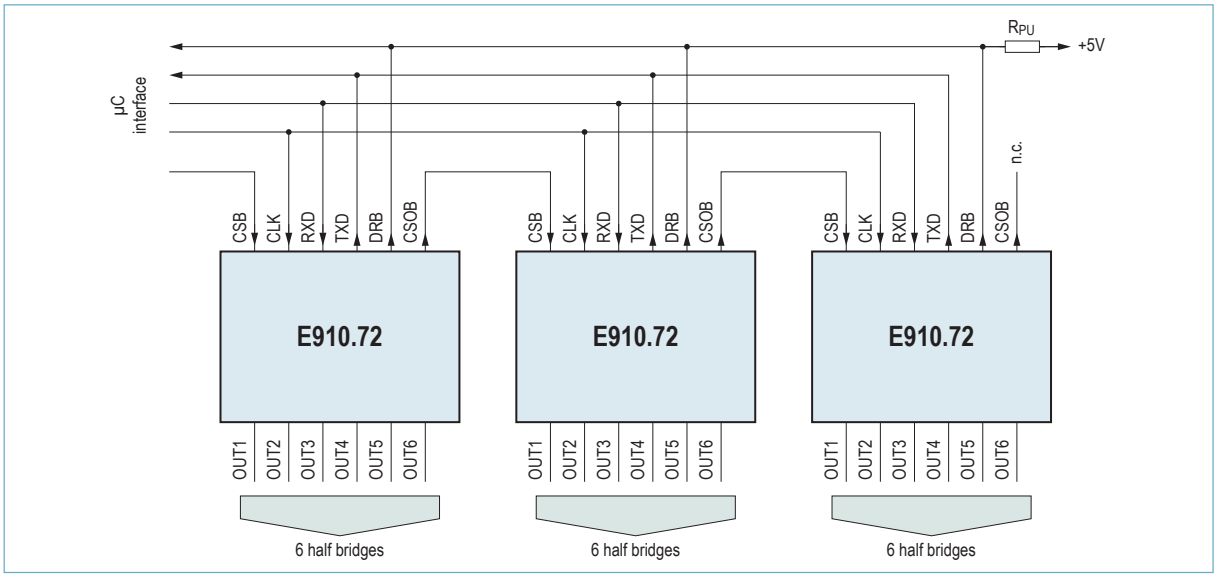


Figure 6: Daisy chain configuration

5.2.21 Examples Of Data Transfer From µC To E910.72 And Vice Versa

The following table contains typical commands sent to and received from the IC:

Command description	Command in hexa-decimal notation Bit order [10:17] or [10:17,20:27,30:37] 1)	Command in hexa-decimal notation Bit order [17:10] or [17:10,27:20,37:30]	Command in binary nota-tion Bit order [17:10] or [17:10,27:20,37:30]
Signal On RXD (From µC To IC)			
Software reset	0xF2	0x4F	0100 1111
Standby	0x70	0x0E	0000 1110
Wake up and read status	0x80	0x01	0000 0001
Write configuration register 1: GainNorm[1:0]=01_b GainBreak[1:0]=11_b PulsThNorm[2:0]=011_b PulsThBreak[2:0]=011_b Bosch Motor	0xB5 0x6E 0x86	0xAD 0x76 0x61	1010 1101 0111 0110 0110 0001

1) Table column in bit order [10:17] or [10:17,20:27,30:37] is only for ELMOS production test purpose

Command description	Command in hexa-decimal notation Bit order [10:17] or [10:17,20:27,30:37] 1)	Command in hexa-decimal notation Bit order [17:10] or [17:10,27:20,37:30]	Command in binary notation Bit order [17:10] or [17:10,27:20,37:30]
Write configuration register 2: NonLinNorm[1:0]=01_b NonLinBreak[1:0]=11_b PulsTNorm[2:0]=010_b PulsTBreak[2:0]=010_b Bosch Motor	0x75 0xAE 0x02	0xAE 0x75 0x40	1010 1110 0111 0101 0100 0000
Read hardware error (Conf. register error)	0x85 0x80 0x80	0xA1 0x01 0x01	1010 0001 0000 0001 0000 0001
Acknowledge hardware error	0x8C	0x31	0011 0001
Signal On TXD (From IC To µC)			
Parity error on last RXD transfer	0x01	0x80	1000 0000
Position data available	0x20	0x04	0000 0100
Position data of ripple detector no. 1 with 13 pulses	xxx	0x04 0x20 0x1A	0000 0100 0010 0000 0001 1010

1) Table column in bit order [10:17] or [10:17,20:27,30:37] is only for ELMOS production test purpose

5.3 Motor Driver Half Bridges

The IC features six half bridge driver outputs. Switching these drivers on and off is performed by SPI commands (see 5.2). Using an address scheme as shown in Chapter 5.2.2, the six half bridges can be used to drive 3 DC motors simultaneously, or up to 5 motors sequentially. In case outputs are not needed for DC motor control, they can be used to drive other kinds of loads like as well, such as relays.
Each half bridge output features bias-free switching, slew rate control, current limitation and overcurrent shut-off. Any half bridge output is shut off into tristate mode after current limitation has been continuously detected for a debounce time of typically 500µs. Output DRB is activated to indicate that diagnostic data is present. A corresponding SPI command has to be sent in order to turn the output on again.
A common overtemperature shut-off switches all outputs into tristate mode when a chip temperature of greater than the shut off temperature T_{SO} has been detected. Output DRB is activated to indicate that diagnostic data is present. After cooling down by the hysteresis T_{HYS}, the outputs are ready to be turned on again by an SPI command.

5.3.1 High Impedance State Of Half Bridge Outputs In Motor Control Mode

To brake a motor from movement and count pulses until it has actually stopped, it is necessary to switch on both low side transistors of the related half bridges. On the other hand to avoid unintended current flow through motors that are not addressed, it is mandatory to switch all half bridges, that are not involved in driving the addressed motor, into high impedance state (tristate). Therefore, each pair of half bridges switches back into tristate after a motor stop has been detected, i.e. 100ms after the last ripple has been detected in brake mode (both low side transistors on).

5.3.2 Short Circuit To External Battery Supply VBAT_EX

A diode in the supply line VBAT_EX to VBAT_HV is recommended for reverse battery protection. Thus the supply voltage of the IC is one diode forward voltage lower than the actual battery voltage VBAT_HV. If a short circuit of an half bridge output to the battery VBAT_EX occurs, the high side transistor will conduct current into the IC's supply, if it is turned on. If it is off, current will be conducted by the high side driver's reverse diode, which is connected in parallel to the external reverse voltage protection diode D1. A parasitic PNP bipolar transistor will also drive current into the IC's substrate. This current may cause significant power dissipation, and after some time the overtemperature shut off may switch all outputs into tristate mode. The IC's current consumption from VBAT_HV will go down below IBAT,STBY and the remaining power dissipation caused by the parasitic PNP transistor cannot damage the IC. To achieve this self-protection feature it is important that no additional current is drawn from the IC's battery supply. Therefore it is recommended to use a separate reverse voltage protection diode for each IC E910.72.

5.3.3 Driving Loads Other Than DC Motors

Half bridge outputs that are not used for DC motor control may drive other kinds of load such as relays or LEDs, as well. In case of overvoltage half bridge outputs are switched to 0, which means that low side transistors are switched on. This is to avoid bulk current being induced by inductive loads in case the output has been switched into tristate mode. Therefore, loads like relays have to be connected to ground and not to battery supply.
Due to some parasitic currents that may flow in case of ground shift, it is recommended to use the half bridge outputs only for relays, LEDs, and similar loads that are placed on the same printed circuit board (PCB).
Switching an output to high level is performed by setting the corresponding direction bit to 1b, for low level a 0b has to be transmitted. All functions related to ripple detection are switched off. Protection features for overcurrent, and overtemperature are the same as in motor control mode. Overvoltage leads to shut-off (i.e. switch off, low side driver active) of the output after a debounce time of typically 10ms. But other than in motor control mode, the output will be turned on again automatically when the voltage has returned to normal condition, after the same debounce time. Undervoltage does not switch off the outputs. Both, overvoltage and undervoltage do not activate output DRB and no diagnostic information is created.

5.4 Positioning By Means Of Ripple Detection

5.4.1 Block Diagram

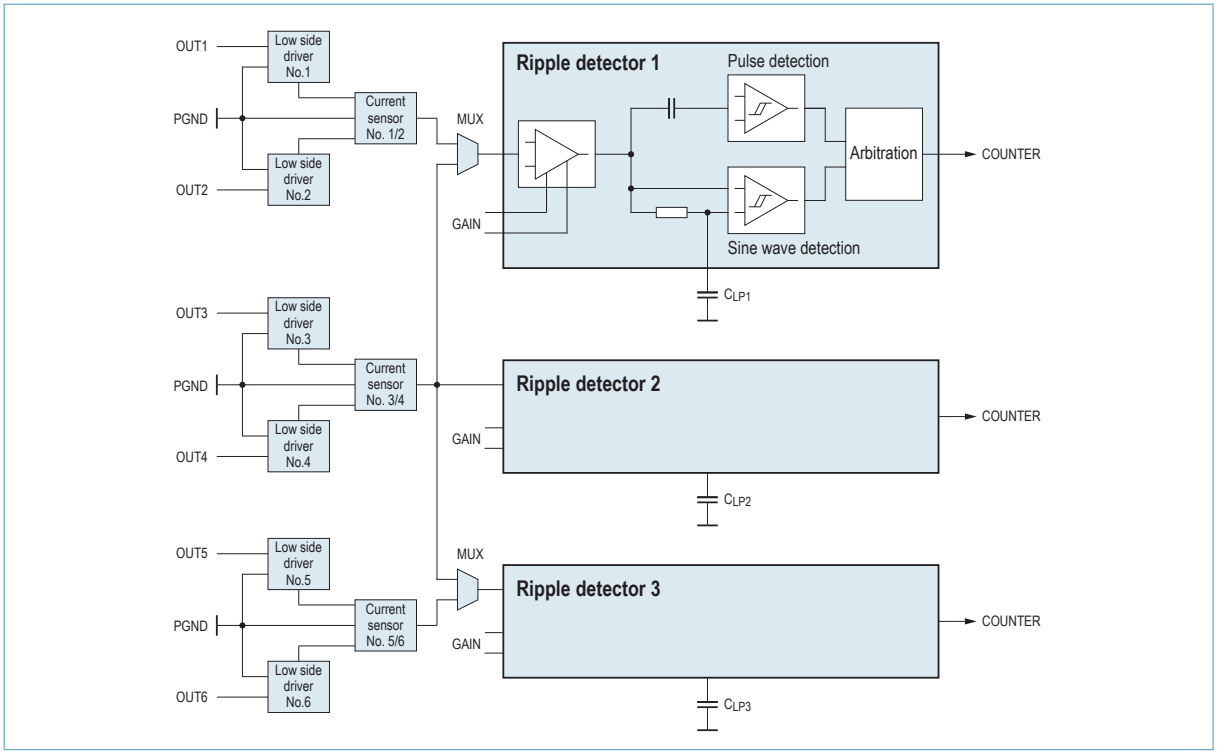


Figure 7: Block diagram of ripple detection

5.4.2 Functional Description Of Ripple Detection

Three independent ripple detection blocks are implemented in the IC, as shown in Fig. 7. This allows positioning of three DC motors simultaneously. Connections are: Motor 1 => OUT1/OUT2, Motor 2 => OUT3/OUT4, Motor 3 => OUT5/OUT6. It is also possible to operate up to 5 motors sequentially. Additional motors 4 and 5 are connected to OUT2/OUT3, and OUT4/OUT5, respectively. For this purpose input multiplexers (MUX) of Ripple Detection Blocks 1 and 3 provide selection of 2 half bridges each.
The current consumption of a DC motor from the supply voltage under constant power and load conditions is not constant, but features an AC component caused by the induced voltages of the motor windings and the current commutation to consecutive windings. The shape of this AC component depends very much on the construction of the motor. A common characteristic is the presence of a periodical signal with a frequency that is defined by the motor speed and the number of rotor windings, equal to the number n of commutator segments. If n is an even number, commutation of the brushes from one commutator segment to the next takes place simultaneously on both brushes. If n is an odd number, commutation occurs alternatively. Thus the ripple frequency f_{RIP} of the AC component is given by the following equations:

$f_{RIP}=s \cdot n$ if n is an even number
$f_{RIP}=2 \cdot s \cdot n$ if n is an odd number

where s is the motor speed in revolutions per second

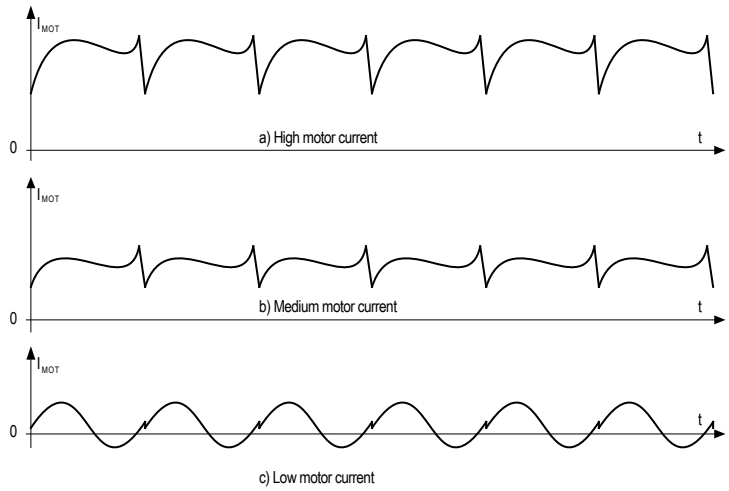


Figure 8: Typical motor current under different load conditions

Fig. 8 shows the typical current shape of a small, symmetrical DC motor with three rotor windings as used in HVAC actuators under different load conditions. It can be interpreted as the superposition of a sequence of inverse sinusoidal "peaks" (from 60° to 120°, i.e. ±30° around the amplitude value of the generator voltage), and exponential inrush curves defined by the L-R time constant of the motor windings.
At the moment of commutation current direction is changed in the winding which is connected to the two consecutive commutator segments involved. This change of direction is delayed due to the winding inductance, which leads to a very rapid current drop on every commutation, visible at high and medium motor currents.
When the average motor current becomes very small with even negative momentary values (see Fig. 8), this significant drop gets very small, and can even vanish completely. The reason is, that when the motor comes close to generator mode the momentary current during commutation becomes very small or even zero. This condition may occur in an HVAC system when air pressure on the flap is in the same direction as the flap movement.

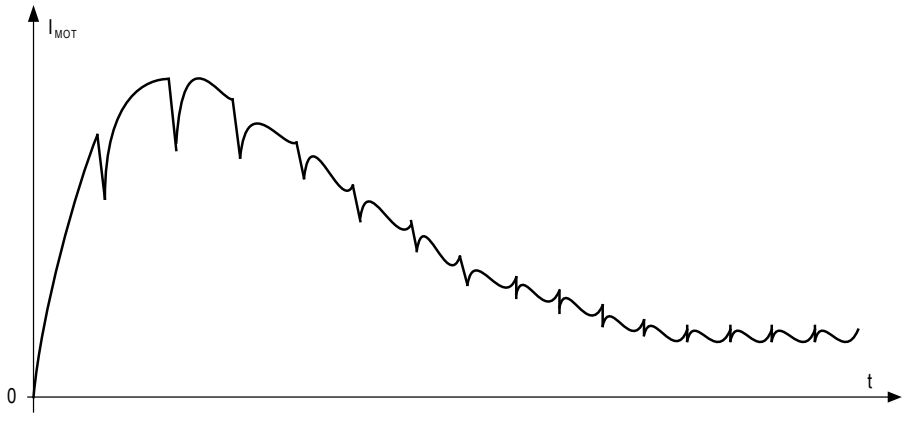


Figure 9: Typical motor current during start

When the motor gets started or braked, or when transients on supply voltage or load appear, the average motor current changes rapidly, and these transients can be higher than the ripple signal to be detected. These conditions are shown in Fig. 10 for a motor start as an example. What is still visible under these conditions are the rapid current drops on every commutation.
Based on the different signal shapes the ripple detection circuit features two different signal paths to realise safe recognition under all conditions. One signal path, called pulse detection, reacts on the rapid current drop, while the other signal path, called sine wave detection, reacts on AC components that are more sinusoidally shaped. An arbitration is implemented to avoid interference of the two paths.
Commutation points can only be detected, if the current signal shape fulfil the specification. For pulses a maximum fall time t_{FALL}, a minimum length $t_{PULSEWIDTH}$ of around $t_{PL,MAX}$ and a minimum drop amplitude $I_{DR,NEG,MAX}$ is necessary. For sine pulses a maximum sine frequency f_{SIN} and a minimum peak peak value $I_{SIN,PP,MAX}$ is necessary.

5.4.3 Current Measurement

Current is measured as voltage drop across the on resistance of a half bridge's low side driver. When the motor brakes, both low side drivers of a full bridge are turned on. The generator voltage of the motor reverses current. So to get a positive voltage for measurement, the detection input is switched to the other transistor.
It is necessary to adapt the gain of the input amplifier to the current that the specific type of motor draws from the supply. The highest possible gain that does not override the amplifier should be selected. Three different gain settings (low, medium, high) can be selected via SPI. For each motor an individual gain can be chosen in the related ripple detection block. Therefore, different types of motors can be connected to the IC. Motor stall current at maximum battery voltage (e.g. 18 V) must not exceed the values given in chapter 'Ripple Detection - DC Characteristics'.
During normal operation switching into brake mode is only possible immediately after a ripple signal has been detected by either the pulse detection or the sine wave detection. A debounce of typically 1ms after the rising edge of the digitised signal is implemented in order to avoid multiple pulses caused by commutator noise, as well as unintended counting on the transition from run to brake mode.

5.4.4 Stall Detection

If the motor gets stalled no ripple signals are detected. A timeout of typically 200ms is implemented to switch the motor off, i.e. into brake mode. A diagnostic signal "Motor Stall" is stored and can be read out together with the position information.

5.4.5 Actuator Positioning

The four actuator positioning parameters motor address, direction, number of counts and the gain have to be transferred via the SPI. The IC activates the corresponding two half bridges and counts commutation pulses until the required number is reached. The motor will then be braked by activating both low side drivers, still counting commutation pulses. Motor stop is detected when no ripple pulses have occurred for typically 100ms.

After the motor has stopped the output DRB is activated and the actual number of counts can be read back from the SPI. This number will normally be higher than the required one since in brake mode the motor delivers an unpredictable number of additional pulses. This number is relatively small, so there is no reason to try to correct it by moving the motor back. Some compensation can be implemented into the control unit by reducing the required

number of counts by an average value derived from statistical tests. Nevertheless, to keep the correct position it is mandatory to consider the real number of counts read back from the SPI.

Different fault conditions may occur during motor movement. In case of VBAT_HV over/under-voltage, and motor stall (no ripples for 200ms), low side switches of both half bridges will be turned on to brake the motor, and no pulses will get lost. Output DRB gets activated and the actual detected number of counts, eventually together with the diagnostic information "Motor Stall", are available via SPI. Overcurrent as well as overtemperature causes half bridges to be switched into tristate mode. Pulses that occur during motor run-out will thus not be detected. DRB will be activated and the last number of counts that has been detected is available together with the diagnostic information from which can be seen that the position might be incorrect.

6 Package Reference

This product is available in a Pb free, RoHS compliant, QFN32L5 plastic package. For dimension details refer to JEDEC MO-220 VHHD-4.

The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.

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