8-CHANNEL AIRBAG SQUIB DRIVER

E981.18

PRELIMINARY INFORMATION - AUG 01, 2011

RoHS compliant

Features

- 8 current limiting high & low side drivers
- Input operation range V_{UX} 8V to 35V
- Two squib current modes (LCM and HCM) selectable via SPI commands
- Short circuit protection
- Simultaneously firing of 4 loops possible, or 8 loops at Ux < 25
- Firing limitation counter
- Squib channel diagnostics and monitoring
- Independent voltage & squib supply voltage diagnostics
- Separate Low side and High side driver control
- Internal free running oscillator
- Test / select function for the drivers
- Serial interface (SPI synchronous communication) to µC (3.3V and 5V tolerant inputs)
- Power-On-Reset circuit

Applications

- Squib driver in a Restraint Diagnostic and control Module (RDM)
- Airbag Deployment

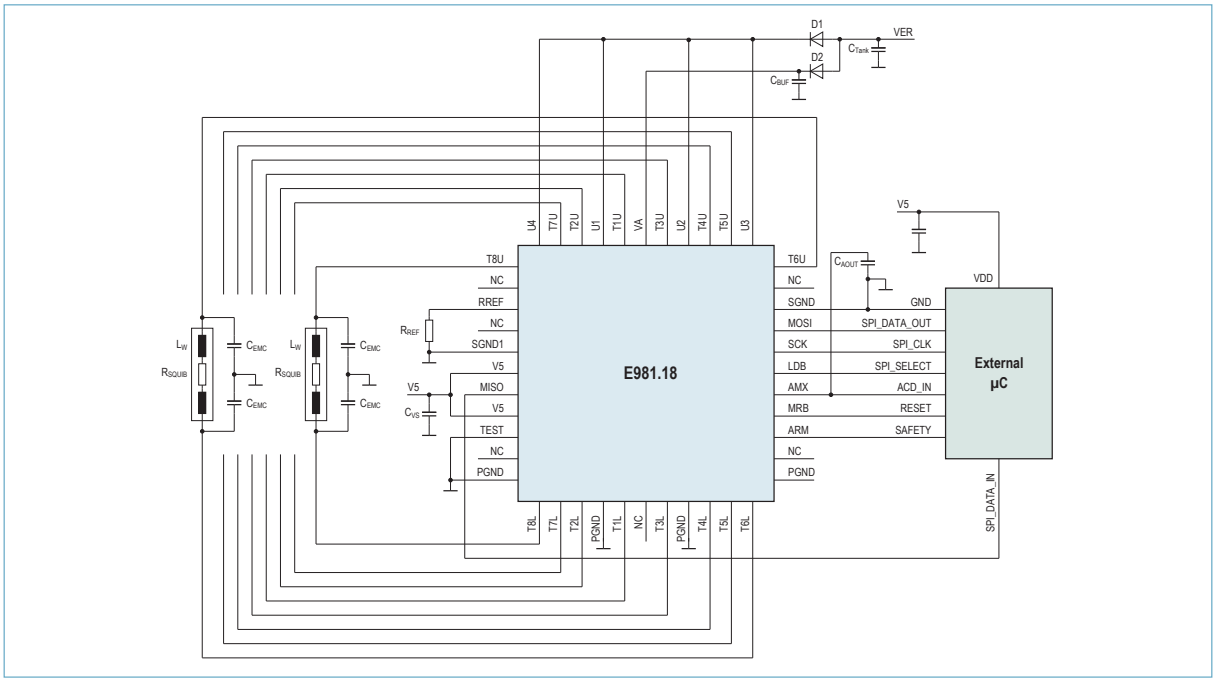
General Description

The Eight Channel Squib Driver E981.18 is designed specifically for automotive airbag applications. The IC provides individual control and diagnostics for 8 floating squibs. It has two sources of control, an arming sensor signal and a µC signal via the SPI bus. An active signal at the arming sensor input will activate all selected drivers, which have been enabled by the µC. During firing the squibs, the input voltage of the high side switch is limited to 25V for LCM and 35V in HCM by the system.

In order to limit the power dissipation of the driver stages, internal firing limitation counters (FTL) are implemented for each high side driver. Additionally an over voltage detection for all 8 LSD (VTxL) output voltages is provided to avoid a damage of the drivers in case of a short to battery during firing or during driver testing.

Ordering Information

Product ID	Temp. Range	Package
E981.18	-40°C to +95°C	QFN44L7



This document contains information on a pre-production product. ELMOS Semiconductor AG reserves the right to change specifications and information herein without notice.

1 Typical Application

1.1 Circuitry

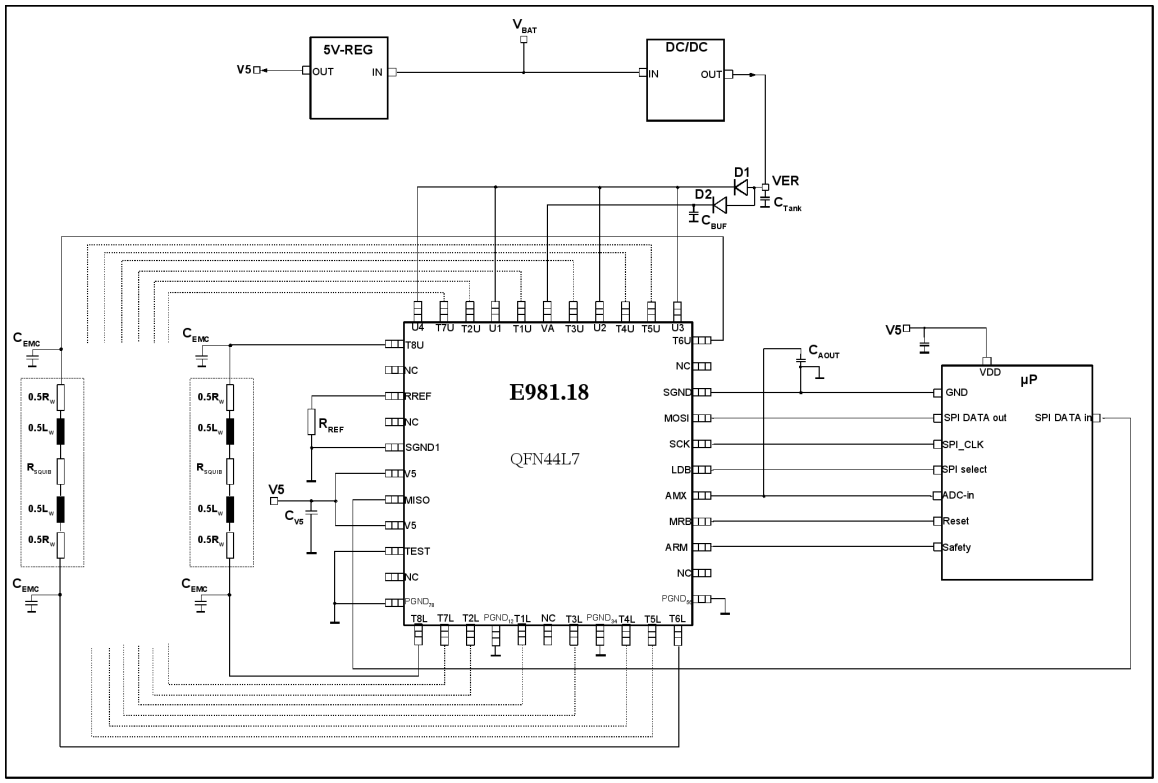


Fig. 1: Typical Application Diagram

1.2 External component list

Component	Functionality	Min	Typ	Max	Tolerances
C_{V5}	Block capacitance	10nF	47nF	TBD	+/-37%
C_{TANK}	Energy Reserve capacitor U_X		3.3mF		+/-37%
C_{AOUT}	Capacitance to buffer AOUT	10pF		1nF	+/-37%
C_{BUF}	Energy Reserve capacitor V_A		2.2µF	15µF	+/-37%
R_{REF}	Reference for squib resistance measurement		8.2Ω	10Ω	+/-3%
C_{EMCX}	EMC filtering for squib		10nF	470nF	+/-37%
R_W	wiring parasitic resistance	0	1Ω	3.5Ω	
L_W 1.)	wiring parasitic inductance	0	7µH	56µH	
R_{SQUIB}	Squib resistor before firing	1.7Ω	2.15Ω	2.5Ω	
D1, D2	Diode for reverse current protection		S1G		

Table 1 : Ratings for external components

1.) The max. loop inductance is limited to 56µH. It is valid for a closed loop and for an open loop condition during fault modes described in chapter 4.3.

2 Pinout

2.1 Pin Description

Nr	Name	Type	Pull	Description
1	T8U	O,HV		Upper side of squib line 8
2	NC			Not connected
3	RREF	O, A		External reference resistor for squib resistance measurements
4	NC			Not connected
5	SGND1			First Ground for diagnosis and control blocks
6	V5	S		Input supply voltage of 5V
7	MISO	O, D		Data output of the serial interface
8	V5	S		Input supply voltage of 5V, (redundant)
9	TEST	I, D		Allows activation of ELMOS test modes. Grounded in application.
10	NC			Not connected
11	$PGND_{78}$			Ground for squib lines 7 and 8
12	T8L	O,HV		Lower side of squib line 8
13	T7L	O,HV		Lower side of squib line 7
14	T2L	O,HV		Lower side of squib line 2
15	$PGND_{12}$			Ground for squib lines 1 and 2
16	T1L	O,HV		Lower side of squib line 1
17	NC			Not connected
18	T3L	O,HV		Lower side of squib line 3
19	$PGND_{34}$			Ground for squib lines 3 and 4
20	T4L	O,HV		Lower side of squib line 4
21	T5L	O,HV		Lower side of squib line 5
22	T6L	O,HV		Lower side of squib line 6
23	$PGND_{56}$			Ground for squib lines 5 and 6
24	NC			Not connected
25	ARM	I, D		Safing controller ARM input
26	MRB	I, D		μP reset of the whole IC
27	AMX	O, A		Diagnostic output
28	LDB	I, D		Load input of the serial interface
29	SCK	I, D		Clock input of the serial interface
30	MOSI	I, D		Data inputt of the serial interface
31	SGND2			Second Ground for diagnosis and control blocks
32	NC			Not connected
33	T6U	O,HV		Upper side of squib line 6
34	U3	S, HV		Energy reserve for squib lines 5 and 6
35	T5U	O,HV		Upper side of squib line 5

Nr	Name	Type	Pull	Description
36	T4U	O,HV		Upper side of squib line 4
37	U2	S, HV		Energy reserve for squib lines 3 and 4
38	T3U	O,HV		Upper side of squib line 3
39	VA	S, HV		Autarky supply for high side gate control
40	T1U	O,HV		Upper side of squib line 1
41	U1	S, HV		Energy reserve for squib lines 1 and 2
42	T2U	O,HV		Upper side of squib line 2
43	T7U	O,HV		Upper side of squib line 7
44	U4	S, HV		Energy reserve for squib lines 7 and 8
45	EDP			**E**xposed **D**ie **P**ad, to be connected to GND in application

Table 2: Pin Description

D = Digital, A = Analog, S = Supply, I = Input, O = Output, HV = High Voltage

2.2 Package Pinout

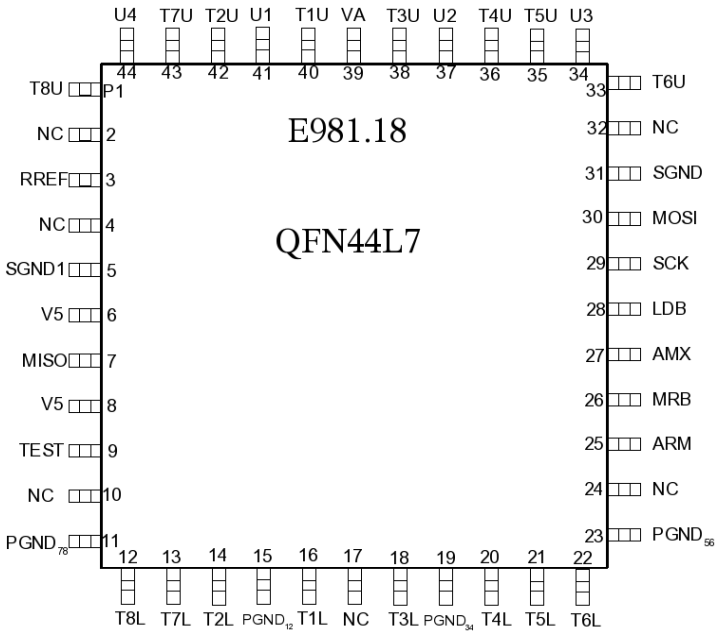


Fig. 2:Package Pinout

3 Block Diagram

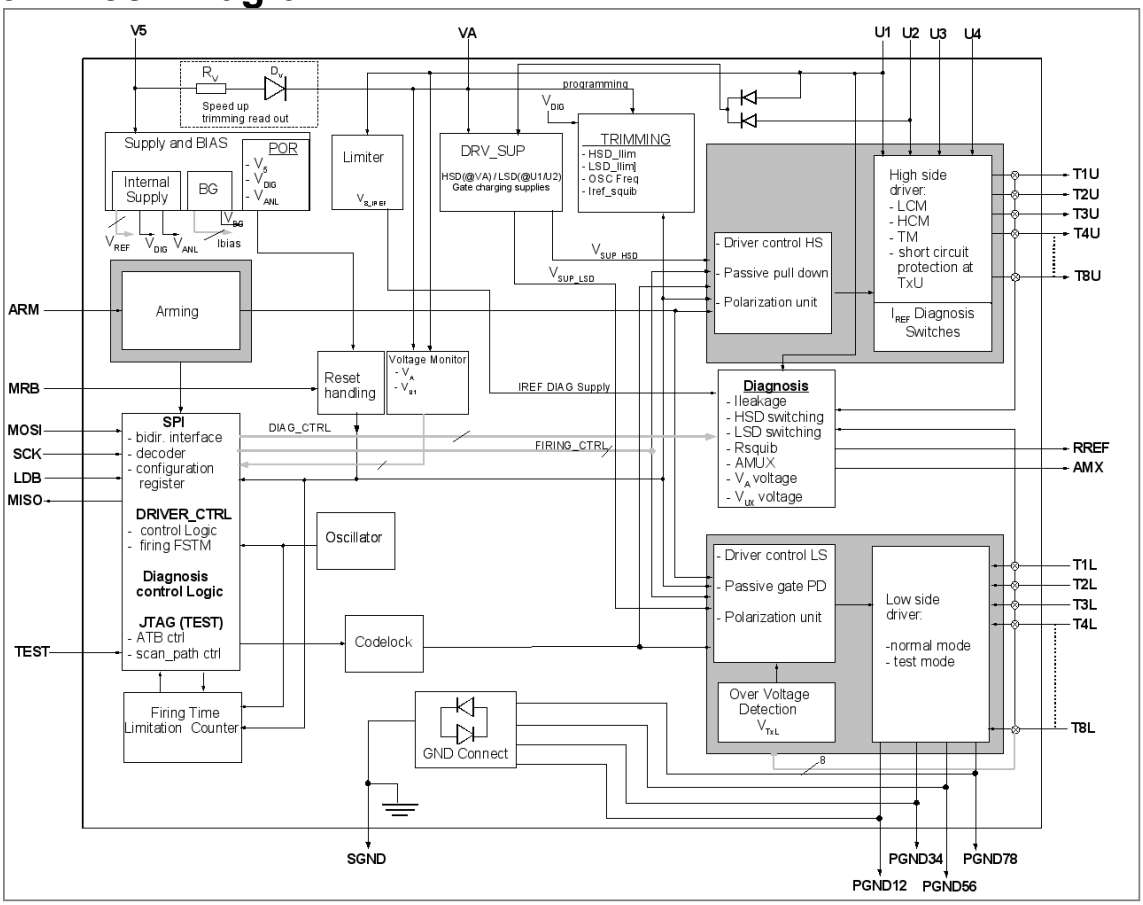


Fig. 3: Block Diagram

4 Operating Conditions

4.1 Absolute Maximum Ratings

Continuous operation of the device above these ratings is not allowed and may destroy the device. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values. An exceeding of this limits may cause a permanent damage of the device.

No.	Description	Condition	Symbol	Min	Max	Unit
1	Supply voltage	Continuous	V_{V5_DC}	-0.3	5.5	V
		Transient t<480ms	V_{V5_TRAN}	-0.5	6.5	V
2	Input voltage pins (MOSI, SCK, LDB, ARM, AMX, MRB, TEST)	Continuous	V_{LV_DC}	-0.3	5.5	V
		Transient t<480ms	V_{LV_TRAN}	-0.5	6.5	V
3	Output voltage pin (MISO)	Continuous	$V_{LV\_O\_DC}$	-0.3	5.5	V
		Transient t<480ms	$V_{LV\_O\_TRAN}$	-0.5	6.5	V
4	Input voltage pins (U1, U2, U3, U4, T1U,...,T8U, T1I,...,T8L, VA, RREF)	Continuous	$V_{HV\_IO\_DC}$	-0.3	40	V
		Transient t<480ms	$V_{HV\_IO\_TRAN}$	-0.5	40	V
5	Input voltage pins (PGND12, PGND34, PGND56, PGND78, SGND)	Continuous	V_{GND}	-0.3	0.3	V
6	Input current		I_{IN}	-10	10	mA
7	Power dissipation; P_{DISS_max} until θ_{J_max} exceeded	θ_A = +95°C;	P_{TOT_MAX}		3200	mW
8	Thermal resistance (junction to ambient)		$R\theta_{J\text{-}A}$ [1)]		17	K/W
9	Junction temperature		θ_{J_max}		150	°C
10	Relative humidity (non-condensing)		RH	5	85	%
11	Soldering temperature	maximum 10s	θ_{SOLDER}		260	°C
12	Operating temperaure		θ_{OPT}	-40	95	°C
13	Storage temperature		θ_{STG}	-40	100	°C

Table 3: Maximum Ratings

[1.)] **following remarks:**
1) Value is based on method according to JEDEC standard JESD-51-5
2) Value is based on situation, where the die-pad is soldered to the board
3) The value presented above is typical only. Actual thermal performance will depend on die-size, die-pad size and presence of hot spots.

The E981.18A is able to operate within specification for at least 15 squib driver activation's.

4.2 Recommended Operating Conditions

The following conditions apply unless otherwise stated. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.
A dropping below this minimum recommended conditions during normal device operation can lead to violations of all specified parameters, but the device will remain in a safe operating condition, which means no maximum limits will be exceeded. Whereas a firing of the squib, while the maximum recommended operation conditions are exceeded, can cause a permanently damage of the device.

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Supply voltage V5		V_{V5}	4.5		5.5	V
2	Autarky voltage V_A for high side drivers	$V_A>(V_{TxU}+8V)$, $4.5V<V_5<5.5V$	V_{VA}	12		35	V
3	Squib supply voltage Ux in diagnostic mode	Diagnostic mode, $4.5V<V_5<5.5V$	V_{Ux_DIAG}	8		35	V
4	Squib supply voltage Ux in LCM	Firing mode,no restriction of firing scenario, $4.5V<V_5<5.5V$	V_{ux_LCM} 1.) 2.)	8		25	V
5	Squib supply voltage Ux in HCM	Firing mode, no restriction of firing scenario, $4.5V<V_5<5.5V$	V_{ux_HCM2} 1.) 2.)	12		35	V
6	Ambient temperature		θ_{AMB}	-40		95	°C

Table 4: Recommended Operating Conditions

1.) The maximum T_{ON} time for the loop is limited by the firing time limiter values of the HSD, given in chapter 5.11.2. This means it is not mandatory to send a switch off CMD for the HSD. This in in opposite to the LSD, where a switch off CMD has to be sent.
The waiting time between two firing groups amounts 0µs.

2.) For the calculation of U_{xfire_MIN} following parameters have to be taken into account to ensure a sufficient firing current in application environment:

- R_{SQUIB} (including behavior over temperature)
- external line resistance of application in current path (U_X, TXL-TXU, GND) in following called $R_{parasitic}$
- $R_{ON\_LSD\_HCM/LCM}$, see chapter 5.12.1
- $R_{ON\_HSD\_HCM/LCM}$ see chapter 5.11.1
- So following expressions for U_{xfire_MIN} are valid:

$$\mathbf{U_{xfire\_MIN\_LCM} \geq max\{8V;\ (R_{ON\_HSD\_LCM}+R_{ON\_LSD\_LCM}+R_{SQUIB}+R_{parasitic})\cdot I_{TXU}\}}$$
$$\mathbf{U_{xfire\_MIN\_HCM} \geq max\{12V;\ (R_{ON\_HSD\_HCM}+R_{ON\_LSD\_HCM}+R_{SQUIB}+R_{parasitic})\cdot I_{TXU}\}}$$

It is obvious that this equation can not be fulfilled for all values of R_{SQUIB}, U_X and I_{TXU}. For example to ensure a correctly firing of the squib for the minimum voltage at U_X, the squib resistance R_{SQUIB} must not cover the full range of specification. This is illustrated in Figure 4 and 5 below.

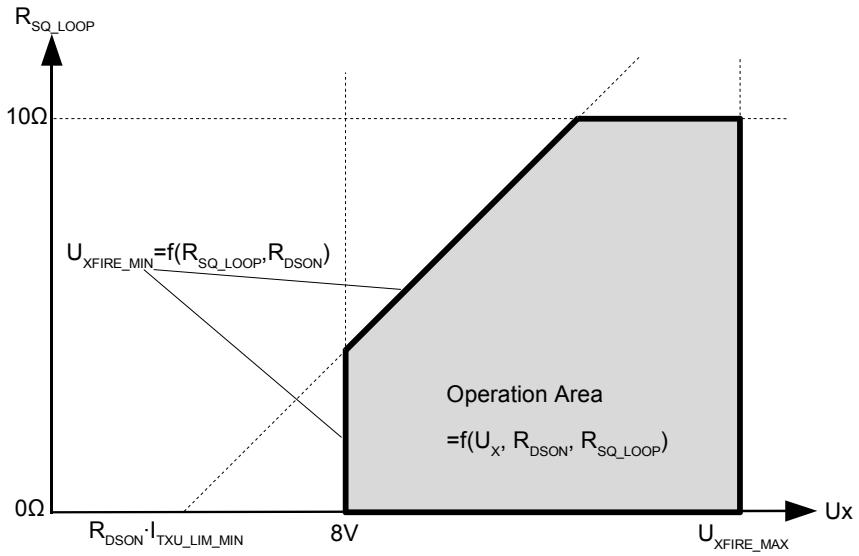


Fig. 4 V_{UX} operation range for LCM; $I_{TXU\_LIM\_MIN}$ =1.2A

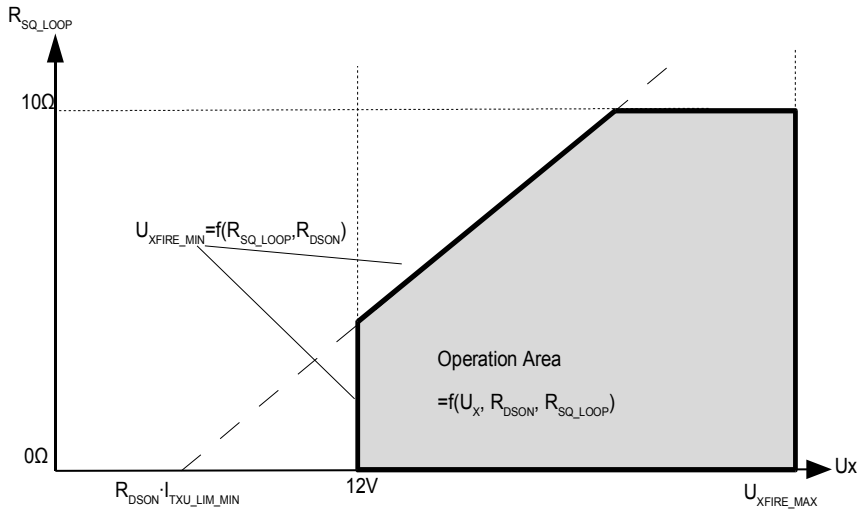


Fig. 5 V_{UX} operation range for HCM; $I_{TXU\_LIM\_MIN}$ =1.75A

Notes:
R_{SQ_LOOP} = R_{SQUIB} + $R_{PARASITIC}$
$R_{PARASITIC}$ = R_{WIRE} + R_{PWB}
R_{DSON} = R_{ON_HSD} +R_{ON_LSD}
$I_{TXU\_LIM\_MIN}$ = 1.2A (LCM) / 1.75A (HCM)

4.3 Squib loop and fault modes

Fig. 6 shows exemplarily the squib firing loop, the outputs stage of the IC, the PCB components generating the energy reserve voltage, the harness and finally the squib igniter.
After the deployment the connection of the squib feed and squib return lines can be a short to ground, an open pin configuration or any phase in between them. This means the driver output stage has to withstand a short to GND or a open pin state at any point of the squib loop. Additionally at any point of the loop a short to battery or to GND can occur in and outside of a firing event, due to a fault mode of the harness. For a fault mode outside of a firing event, the maximum pulse energy applied to the squib has to be limited, to avoid an inadvertent deployment. This is also valid if the IC is not supplied. The EMC capacitors by itself will contribute an energy of :
E_{CEMC}= 0.5 C_{EMC} U^2 during a fault mode, therefor the max. value for this capacitors has to be limited.
For a fault mode during a firing event no damage of the IC will occur.

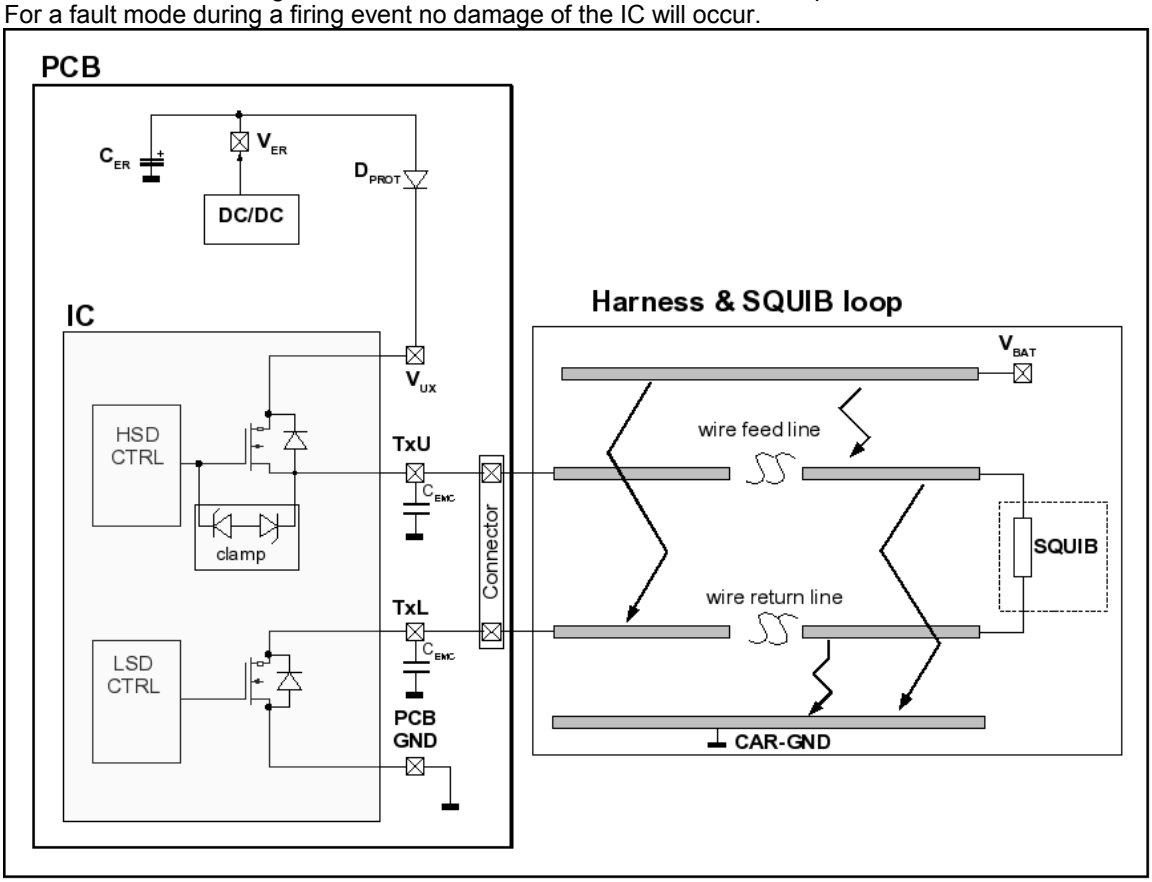


Fig. 6: Squib loop

The maximum values for leakage and pulse energy outside of a firing event are given in Table 5 below.

Currents flowing into the circuit pins have positive values.

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Pulse energy applied to the squib due to short circuit to GND outside of a firing event.	IC supplied / not supplied; C_{EMC_max}=138nF; $T_{ENRG\_PULSE\_max}$=120µs 1.)	$ENRG_{MAX}$ 2.)			112	µJ
2	Pulse energy applied to the squib due to short circuit to V_{BAT} outside of a firing event.	IC supplied / not supplied; C_{EMC_max}=138nF; V_{BAT_MAX}=18V; $T_{ENRG\_PULSE\_max}$=120µs 1.)	$ENRG_{MAX}$ 2.)			112	µJ
3	DC $I_{LEAKAGE}$ at TxU or TxL pins for a short circuit to GND or battery at any point of the squib line.	IC supplied / not supplied; V_{BAT_MAX}=18V.	$I_{LEAK\_SQBLINE2}$ 2.)	-25		+25	mA

Table 5: Fault mode characteristics

1) current peak pulse length for which the the energy has to be determined. Necessary because if the SC is applied during a driver activation under reduced test mode condition, there will be the nominal DC current superposed.
2) Not tested during production test at ELMOS. Guaranteed by design.

5 Detailed Electrical Specification

The following conditions apply unless otherwise stated. All potentials refer to GROUND (GND) unless otherwise specified. Currents flowing into the circuit pins have positive values.

5.1 Supply

- V5, external supply
- V_A, external supply
- V_{UX}, [x=1..4], external supply
- V_{DIG}, internal supply
- V_{ANL}, internal supply
- V_{LSDSUP}, internal supply

5.1.1 Terminal V5, external Supply voltage

External voltage pin V5 supplies:
- analogue output AMX
- Control unit for $I_{REFSQUIB}$ diagnosis switches
- internal 3.3V analogue supply V_{ANL}
- internal 3.3V digital supply V_{DIG}
- LV input and output pads
- V5 pin is equipped with a power on reset monitoring. For more details regarding global supply monitoring see chapter 5.3

No.	*Description*	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
1	Supply current I_{V5}	4.5V<V5<5.5V, all LSD and HSD disabled. Squib diagnosis disabled	I_{V5}			4.3	mA
2	Supply voltage V5		V_{V5}	4.5	5.0	5.5	V
3	Power On Reset	V_5 0V → 5V	POR_ON_{V5}	3.80		4.45	V
4	Power Off Reset	V_5 5V → 0V	POR_OFF_{V5}	3.60		4.25	V

Table 6: Terminal V5, DC characteristics

5.1.2 Terminal VA, external supply voltage

External voltage pin V_A provides the HSD gate charging currents during activation.
V_A is connected to the energy reserve voltage V_{ER} of the application by a diode. The pin must be buffered by a grounded capacitor C_{VA} to sustain minimum voltage level for a crash event after loss of battery. To ensure that all parameters derived directly from the HSD regulation loop, are in the required operating range, the voltage V_A must exceed a minimum threshold V_{A_EN}.
A more detailed description of the global supply monitoring is given in chapter 5.3.
The V_A pin is also used for the programming of the trimming array during **A**utomatic **T**est **E**quipment (ATE). To ensure a safe read out of the trimming array after power up in application, the voltage at VA must exceed the minimum threshold of $V_{A,READ\_TRM,EN}$. To speed up this, there is a forward diode connected between external V_5 and V_A pins. The principle is shown in the block circuitry in Fig. 3.
The voltage is visible at the analogue output AMX.

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	V_A voltage threshold	4.5V<V_5<5.5V; V_A: 0V → $V_{A,max}$	V_{A_EN}	10		12	V
2	Minimum V_A voltage needed for correct read out of the trimming block	4.5V<V_5<5.5V, V_A: 0V → $V_{A,max}$	$V_{A,READ\_TRM,EN}$	3.30		3.85	V
3	I(VA) without driver activation	8V<V_A<35V	I_{VA,DRV_off} 1.)			25	µA
4	Additional current I(VA) for each activated High Side Drive in normal modes (LCM or HCM)	4.5V<V_5<5.5V, V_A> [V(TxU)+8V]	$I_{VA,DRV\_on,NM}$ 2.)			150	µA
5	Additional current I(VA) for each activated High Side Drive in Test Mode (TM)	4.5V<V_5<5.5V, V_A> [V(TxU)+8V]	$I_{VA,DRV\_on,TM}$ 2.)			220	µA

Table 7: Terminal VA, external supply voltage

1) Static current consumption of the V_A-voltage divider and the V_A-Monitoring
2) For example during a parallel activation of all 8 HSD in LCM/HCM or in TM, the max. total V_A current consumption amounts:
   $I(V_A)_{MAX\_LCM/HCM}$ = (8x150µA) + 25µA= 1.225mA
   $I(V_A)_{MAX\_TM}$ = (8x220µA) + 25µA= 1.785mA

5.1.3 Terminal Ux [x=1..4], external voltage supply for deployment current

U_1..U_4 Firing current source supplies:

- U_1 supplies internal V_{8_IREF} voltage source providing internal $I_{REF40mA}$ current source for squib resistance measurement
- U_1/U_2 supply internal analogue supply voltage V_{LSDSUP} used for LSD gate charging
- U_x supplies passive gate pull down structures for each HSD

- U_1 voltage is provided with a supply monitoring. For more details regarding global supply monitoring see chapter 5.3
- The U_X voltages are visible at the analogue output AMX

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	I(U1) Quiescent current	8V<U_X<35V, X=[1] I_{REF} diagnosis disabled, all Driver switched off.	I_{U1}			500	µA
2	I(U2,U3,U4) Quiescent current	8V<U_X<35V, X=[2..4] I_{REF} diagnosis disabled, all drivers switched off,	I_{UX}, x=[2..4]			400	µA
3	Minimum V_{U1} voltage to ensure that V_{LSDSUP} and V_{8_IREF} are in normal operating range.	4.5V<V_5<5.5V;	V_{U1_EN}	7.2		8	V
4	Error of input current $\Delta I_{U1\text{-}RREF} = (I_{U1}\text{-}I_{RREF})/I_{U1}$	4.5V<V_5<5.5V; 8V< U1 < 35V; all drivers disabled; I_{REF} switched to R_{REF}	$\Delta I_{U1\text{-}RREF}$			2,5	%

Table 8: Terminal U_X , x=[1-4] external supply voltage used as fire current source

5.1.4 V_{DIG} internal 3.3V logic supply voltage

V_{DIG} is derived from external V_5 voltage and supplies:
- internal logic
- Power On reset
- 8 MHz oscillator
- trimming array

- V_{DIG} is equipped with a power on reset monitoring and visible at the analogue output AMX. For more details regarding global supply monitoring see chapter 5.3

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	V_{DIG} voltage range	4.5V< V_5 <5.5V	V_{DIG}	3.0	3.3	3.6	V
2	Power On Reset	V_{DIG}: 0V → 3.3V	POR_ON_{VDIG}	2.55		2.95	V
3	Power Off Reset	V_{DIG} :3.3V → 0V	POR_OFF_{VDIG}	2.45		2.85	V

Table 9: Internal Supply V_{DIG}

5.1.5 V_{ANL} internal 3.3V analogue supply voltage

V_{ANL} is derived from external V_5 voltage and supplies:

- Band-gap reference
- I_{DAC} for HSD and LSD reference currents
- I_{REF_SQUIB} current reference generation
- all internal bias voltages and currents

- V_{ANL} is equipped with a power on reset monitoring and visible at the analogue output AMX. For more details regarding global supply monitoring see chapter 5.3

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Voltage range V_{ANL}	4.5V<V_5 <5.5V	V_{ANL}	3.00		3.60	V
2	Power On threshold	V_{ANL} 0V → 3.3V	POR_ON_{VANL}	2.55		2.95	V
3	Power Off threshold	V_{ANL} 3.3V → 0V	POR_OFF_{VANL}	2.45		2.85	V

Table 10: Internal Supply V_{ANL}

5.1.6 V_{LSDSUP} internal 7.5V analogue supply voltage

V_{LSDSUP} is derived from external U_1/U_2 voltages and supplies:
- LSD gate charging unit
- The voltage is visible at the analogue output AMX

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Voltage range V_{SUPLSD}	$8V<V_{U1/U2}<35V$	V_{SUPLSD}	6,0		9,3	V

Table 11: Internal Supply V_{LSDSUP}

5.2 Terminal MRB, external Reset Pin

Low active, by this signal all internal registers are reset.

5.2.1 DC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input Low voltage	$4.5V<V_5<5.5V$	$V_{Di,L}$ MRB	0.8	-	-	V
2	Input High voltage	$4.5V<V_5<5.5V$	$V_{Di,H}$ MRB	-	-	2	V
3	Internal pull down resistor	$V_{MRB}<V_5$	R_{PD} MRB	30	50	70	kΩ

Table 12: Terminal MRB, DC

5.2.2 Dynamic characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Minimum active low pulse for the reset at pin MRB	$4.5V<V_5<5.5V$	T_{MRB} 1.) 2.)	3		5	µs

Table 13: Terminal MRB, AC

1.) MRB pulses with pulse length lower than T_{MRB} will not trigger a reset.
2.) tested by ATPG scan test during ELMOS production test.

5.3 Global Reset and voltage monitoring

The principle of the Power_on Reset concept and the supply monitoring is shown in Fig. 7.

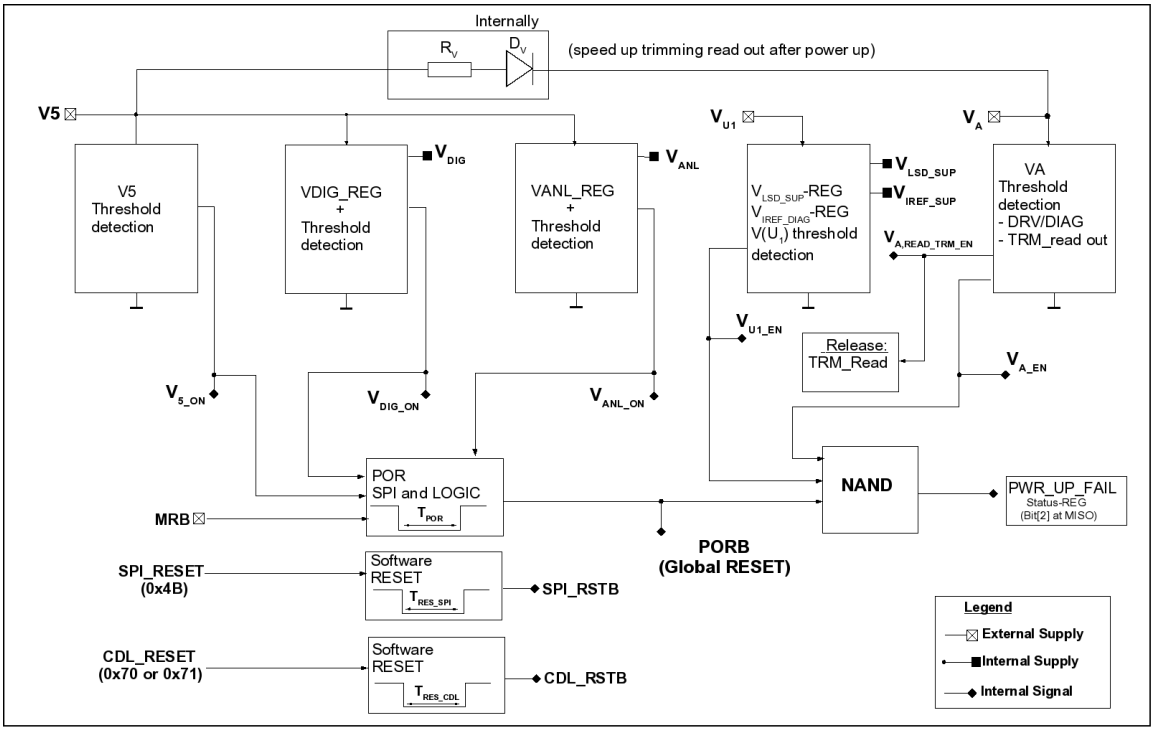


Fig. 7: Reset and supply monitoring

There exist several 4 ways to reset the ASIC.

1) internal **Global Power on Reset** with pulse length T_{POR} (see chapter 5.3.2) is triggered in case of under voltage condition at:
   - V_5 (external supply)
   - V_{DIG} (internal supply)
   - V_{ANL} (internal supply)
2.) external **Global Power on Reset by MRB**
   For both global reset mechanisms, all internal registers are set to default values. Also the FUSE Array read out procedure is restarted again.
3.) **CODELOCK Reset (0x70 or 0x71)**. Codelock close/open command generates a reset pulse (T_{RES_CDL}, see chapter 5.5.1) . All internal registers are reset by internal signal *CDL_RSTB* except the Codelock register itself, the SPI register, the AMX-switch S1 and the Deployment current mode adjustment (LCM/HCM). This is needed to be able to diagnosis the UNLOCK during application and to maintain the programmed Current Mode for the activation sequences.
4.) **SPI Reset (0x4B)** generates a reset pulse (T_{RES_SPI}, see chapter 5.3.2). With the help of this command all internal registers are reset by internal signal *SPI_RSTB* except the SPI registers and the Deployment current mode adjustment (HCM/LCM)

The reset values of all SPI-CMD registers, depending on the reset mechanism (POR/ SPI-Reset/ UNLOCK↑↓) is described in chapter 5.14.

The output of the supply monitoring of V_5, V_{ANL} and V_{DIG} are gated with the external reset signal MRB to one global **PORB** as sketched in Fig. 7.
To make the power up status of the IC visible for the external µP, the global **PORB,** the $\mathbf{V_{U1\_EN}}$ and the $\mathbf{V_{A\_EN}}$ are gated and summarized in a SPI status outputs register **PWR_UP_FAIL**. If a power-up fail event occurs, this bit is set to high level and frozen. By this the µP is able to read out the information in a later SPI timing, also when the under voltage event has disappeared again. The reset of this register has to be done with a clear CMD (see chapter 5.4.5).

To ensure a safe read out of the trimming array, V_A must reach the minimum required threshold $V_{A,READ\_TRM\_EN}$. To speed up this, there is a bypass built by a forward diode from V_5 to the V_A pin internally. To limit the forward current, charging the external C_{BUF} (see chapter 1.2), a Resistor R_V is implemented. R_V is in the range between 700Ω and 1850Ω. Consequently the duration after power up, when the fuse array read out will be started is given by the time constant $T=R_V\ C_{BUF}$.
If V_A drops during operation below the $V_{A,READ\_TRM\_EN}$ threshold, the read out of the FUSE Array is restarted again. The status of the FUSE-Read out is visible at the MISO output flag “FUSE-FAIL (Bit[3], see chapter 5.4.5).

5.3.1 POR and voltage monitoring DC characteristics

see chapter 5.1.1, 5.1.2, 5.1.4, 5.1.5, 5.1.6 and 5.2.1.

5.3.2 POR Dynamic, characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Global POR pulse length		T_{POR} 1) 2.)	10		30	µs
2	SPI reset pulse length	SPI-reset CMD	T_{RES_SPI} 1)		250 $(1/F_{OSC\_nom})*2$		ns

Table 14: Reset, AC

1) tested by ATPG scan test during ELMOS production test.
2) The POR reset pulse duration is derived from a not trimmed oscillator frequency F_{OSC_NC}, because the FUSE Array read out is started after the power on reset pulse disappears (see chapter 5.13 and 5.15 for more detailed information about oscillator and trimming read out).

5.4 SPI

Communication interface

5.4.1 Principle

The communication to the uP is provided by the 4 pin SPI interface.

- SCK: SPI clock
- LDB: SPI chip select, low active
- MOSI: SPI master out ↔ slave in, serial data input. 4 address bits + 4 bit data
- MISO: SPI slave out ↔ master in, serial data output, containing a 8 bit status frame

Fig. 8 shows the SPI block configuration, Fig. 9 shows the principle of the address and data mode transfer.

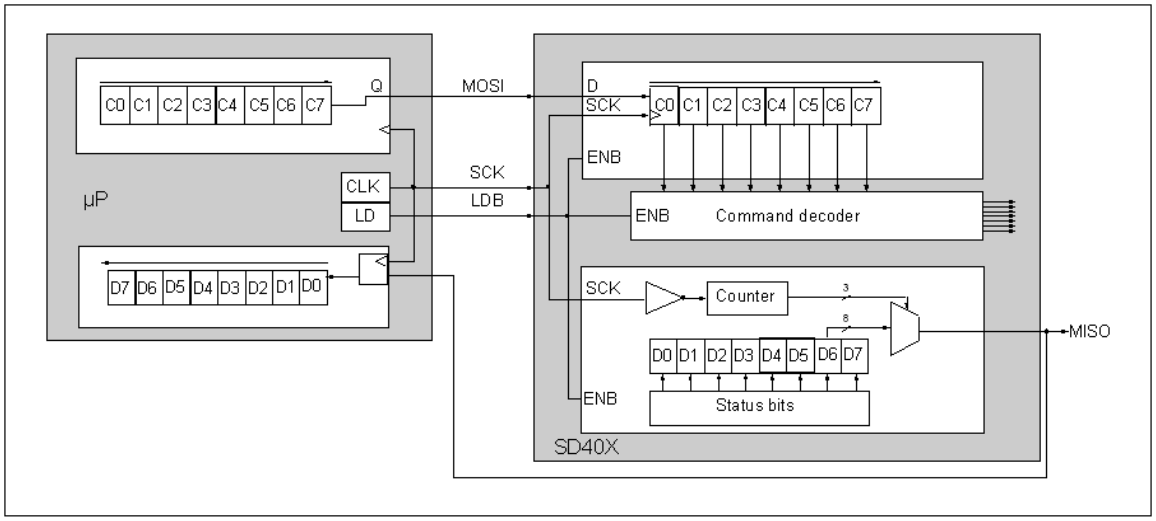


Fig. 8: SPI block diagram

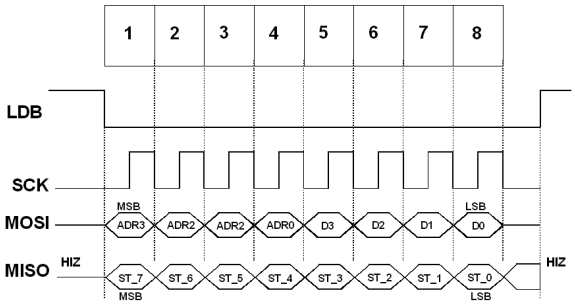


Fig. 9: SPI 8 bit transfer

Each transmission starts with a falling edge on LDB and ends with the rising edge. During the transmission command and data shift is controlled by SCK and LDB according to the following rules:

- Commands and data are shifted with MSB first and LSB last.
- Each bit on the MOSI line is sampled on the rising edge of SCK
- Each bit on the MISO line is shifted out on the falling edge of SCK
- A command is only executed on the rising edge of LDB when 8 **or 16** clock-cycles are counted during the last transmission.
- MISO becomes active during LDB='0' and is Tristate during LDB='1'

The 981.18 allows a 8 or 16 Bit data transfer. In case of a 16 Bit transfer, the last 8 bits are decoded and the first 8 bits are rejected. The 8 bit MISO output will be sent two times in this case.

5.4.2 SPI Terminal MOSI,SCK, DC

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input Low voltage	4.5V<V_5<5.5V	$V_{Di,L,MOSI,SCK}$	0.8	-	-	V
2	Input high voltage	4.5V<V_5<5.5V	$V_{Di,H,\ MOSI,SCK}$	-	-	2	V
3	Internal pull down resistor	4.5V<V_5<5.5V;	$R_{PD,MOSI/SCK}$	90	150	210	kΩ

Table 15: SPI Terminals MOSI,SCK

5.4.3 SPI Terminal LDB, DC

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input low voltage	4.5V<V_5<5.5V	$V_{Di,L}$ LDB,	0.8	-	-	V
2	Input high voltage	4.5V<V_5<5.5V	$V_{Di,H}$ LDB	-	-	2	V
3	Internal pull up resistor	4.5V<V_5<5.5V,	R_{PU_LDB}	90	150	210	kΩ

Table 16: SPI Terminal LDB

5.4.4 SPI Terminal MISO, DC

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Output Low voltage	I_{MISO} = +500uA; 4.5V<V_5<5.5V	$V_{Do,L}$ MISO	-	-	0.4	V
2	Output High voltage	I_{MISO} = -200uA, 4.5V<V_5<5.5V	$V_{Do,H}$ MISO	V_5 -0.4	-	-	V
3	High impedance output current during high level at pin LDB	4.5V<V_5<5.5V, 0<V_{MISO}<V_5	I_{LEAK} MISO	-2.5		+2.5	µA

Table 17: SPI Terminal MISO

5.4.5 Definition of 8 bit status frame at MISO

	Bit[7] MSB	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0] LSB
Status 8 Bit CMD	PAR	FE	SC_TXU	OV_TXL	FUSE_FAIL	PWR_UP_FAIL	TM	CM
RESET value	1	0	0	0	1	1	0	0

Table 18: SPI Terminal MISO, output frame

BIT[0;1]
CM = 0 =>LCM active (default)
CM = 1 =>HCM active
TM = 0 => no Test Mode Driver active
TM = 1 => Test Mode Driver active
Bit is set to 1, if either TEST_UP (SPI CMD 0xE3) or TEST_LOW (SPI CMD 0xEC) is selected. Which Driver Test mode is active (TESTDRH/TESTDRL) can be read out at the AMX Pin with according SPI CMD.

BIT[2]
PWR_UP_FAIL =0 =>Power up ok, all supplies in recommended operating range
PWR_UP_FAIL =1 =>Power up fails. If a Power-Up failure occurs the “1” Bit is frozen, to be visible for the µP. Register can be reset with according clear-CMD by SPI. After 1st power-up the bit remains at default H-level. If the power up has been finished successfully, the bit will change to L-level after the clear-CMD is set.

BIT[3]
FUSE_FAIL = 0 => Read out of Trimming array finished and OK
FUSE_FAIL = 1 = Read out of Trimming array not finished or erroneous (Parity check fails). The Fuse Read out will be repeated 16 times. if the last run ends erroneous the internal state machine stops with a permanently failure flag.

BIT[4]
OV_TXL=0 => no over voltage at all TXL (OV_TXL)
OV_TXL=1 => an over voltage at one or more TXL (OV_TXL) has occurred. Bit is frozen after occurring. Register can be reset with according clear-CMD by SPI
BIT[5]
SC_TXU=0 => no short circuit to GND at all TXU(SC_TXU)
SC_TXU=1 => short circuit to GND at one or more TXU(SC_TXU) has occurred. Bit is frozen after occurring. Register can be reset with according clear-CMD by SPI
BIT[6]
FE=Frame error: wrong Master command received (frame Bit length differs from 8 or 16Bit).
BIT[7]
PAR=Output Frame Parity BIT (safety); odd-Parity chosen.

5.4.6 SPI, dynamic characteristics for Inputs MOSI,SCK, LDB

General condition:4.5<V5<5.5V

No.	Description	Condition	Symbol	Min	Max	Unit
1	SPI clock (SCK) operating frequency		f_{SCK} 2.)	-	8.08	MHz
2	SPI clock (SCK) period	SPI: Period SPI clock, 40% < duty cycle < 60%	t_{SCK} 2.)	123.7	-	ns
3	Clock (SCK) high time		t_{SCKH} 2.)	48.8	-	ns
4	Clock (SCK) low time		t_{SCKL} 2.)	48.8	-	ns
5	Clock (SCK) fall time		t_{fall} 2.)	5.5	13	ns
6	Clock (SCK) rise time		t_{rise} 2.)	5.5	13	ns
7	Data input setup time	SPI: Time from changing MOSI (10%, 90%) to ↑ SCK(90%) . Data setup time	t_{setup} 2.)	37	-	ns
8	Data input hold time	SPI: Time from ↑ SCK (90%) to changing MOSI (10%,90%)	t_{hold} 2.)	49	-	ns
9	Enable (LDB) lead time	SPI: Time from ↓ LDB (10%) to ↑ SCK (90%)	t_{LDB_lead} 2.)	61.8	-	ns
10	Enable (LDB) lag time	SPI: Time from ↓ SCK (10%) to ↑ LDB (90%)	t_{LDB_lag} 2.)	61.8	-	ns
11	Sequential transfer delay	Time between SPI cycles, LDB at high level (90%)	t_{td} 1.)	750	-	ns
12	Input capacitance	Pins MOSI/LDB/SCK	C_{DI} 3.)		5	pF

Table 19: SPI inputs, dynamic characteristic

1) minimum time length necessary to fulfill timing related to the Codelock and SPI reset pulse length.
2) These timings are given by the MCU. The IC`s SPI circuit is designed to be fully operational under these worse case timings. SPI functionality test at WC timings is done during production test.
3) Not tested during production test, guaranteed by design.

5.4.7 SPI, dynamic characteristics, Output MISO

General condition:4.5<V5<5.5V

No.	Description	Condition	Symbol	Min	Max	Unit
1	Data output access time MISO	C_{MISO}≤50pF; SPI: Time from ↓ LDB (10%) to data active from high-impedance state at MISO	t_a 1)	-	43	ns
2	Data output (MISO) valid after SCK	C=<50pF; SPI: Time from ↓ SCK (10%) to next data valid at MISO (90%)	t_V 1) 2.)	-	30	ns

No.	Description	Condition	Symbol	Min	Max	Unit
3	Data output (MISO) lag time	C=<50pF;	t_{MISO_lag} 1)	0	-	ns
4	Data output (MISO) disable time	C_{MISO}≤50pF; SPI: Time from↑ LDB (90%) to high impedance state at MISO	t_{dis} 1) 3.)	-	50	ns
5	Input capacitance	MISO-Pin in Tristate (LDB at Logic High level)	C_{DI} 4.)		5	pF

Table 20: SPI output, dynamic characteristic

1.) tested by appropriate SPI-protocols during production test.
The definition of the parameters is illustrated in Fig. 10
2.) SCK input 2.4V/0.4V; MISO 10% / 90% of V5
3.) Measurement condition: 1k Pull-Up resp. Pull-down resistor on pin MISO. Measurement from 90%LDB to 10%MISO rise, resp. 90% MISO fall
4.) Not tested during production test, guaranteed by design.

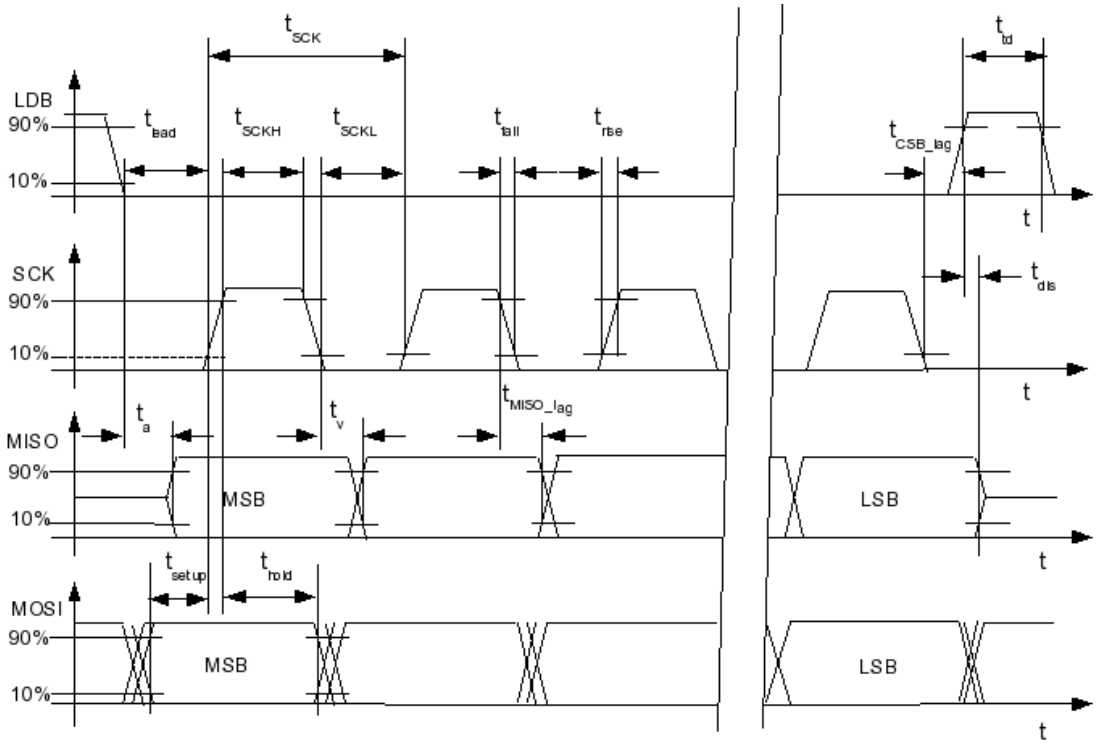


Fig. 10 SPI dynamic parameter definition

5.5 CODELOCK

- Internal TIMER to enable HSD and LSD for the $T_{TIMEOUT}$ duration.

UNLOCK:
Unlock command starts the codelock timer to enable the activated high and low side drivers. When the codelock timeout is reached after $T_{timeout}$, the low side and high side drivers are disabled. Additional UNLOCK commands during $T_{timeout}$ are extending $T_{timeout}$ by resetting the timer.
LOCK:
Lock command closes the codelock via SPI and disables the high side and low side drivers.
To close the codelock before the timeout, the command CODELOCK LOCK can be used.
On each rising or falling edge of *Unlock_Out* signal the following initialization is done:

- A Reset pulse is generated for T_{res_cdl}
- Reset of most of the SPI registers (see SPI CMD-List in chapter 5.14 for more details)

5.5.1 CODELOCK, Dynamic Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Fire codelock Timeout		$T_{TIMEOUT}$ [1)]	150		250	ms
2	Codelock reset pulse length		T_{RES_cdl} [1)]		$\frac{250}{(1/F_{OSC\_nom})*2}$		ns

Table 21: CODELOCK, AC

[1)] tested by ATPG scan test during ELMOS production test.

5.6 Terminal ARM

"ARMING" sensor signal, high active.
The codelock enable line is masked by the external input „ARM" according to the following rules:

- ARM = logic 1 enable line unaffected
- ARM = logic 0 enable line masked (driver disabled)

In positive logic it exists a logical AND between the enable and the arm line. For safety reasons the required pulldown at the ARM input is built up with a resistance.

5.6.1 ARM, DC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input Low voltage	$4.5V<V_5<5.5V$	$V_{Di,L}$ ARM	0.8	-	-	V
2	Input High voltage	$4.5V<V_5<5.5V$	$V_{Di,L}$ ARM	-	-	2	V
3	Internal pull down resistor	$4.5V<V_5<5.5V$;	R_{PD_ARM}	30	50	70	kΩ

Table 22: Terminal ARM, DC

5.6.2 ARM, dynamic characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input capacitance		C_{ARM} 1)			5	pF

Table 23: Terminal ARM, AC

1) not tested during production test, guaranteed by design.

5.7 HSD and LSD Control Modules

The high side driver block and the low side driver block are physically separated.
The driver control is managed by two driver control modules. One governs all the high side drivers and one all the low side drivers.

5.7.1 HSD Control Module

The HSD control can be separated into two different modes:
- Deployment Mode (HCM/LCM)
- HSD Test Mode with reduced current level (TEST_UP Mode)

The principle of the HSD control module is shown in pictures Fig. 11 below.

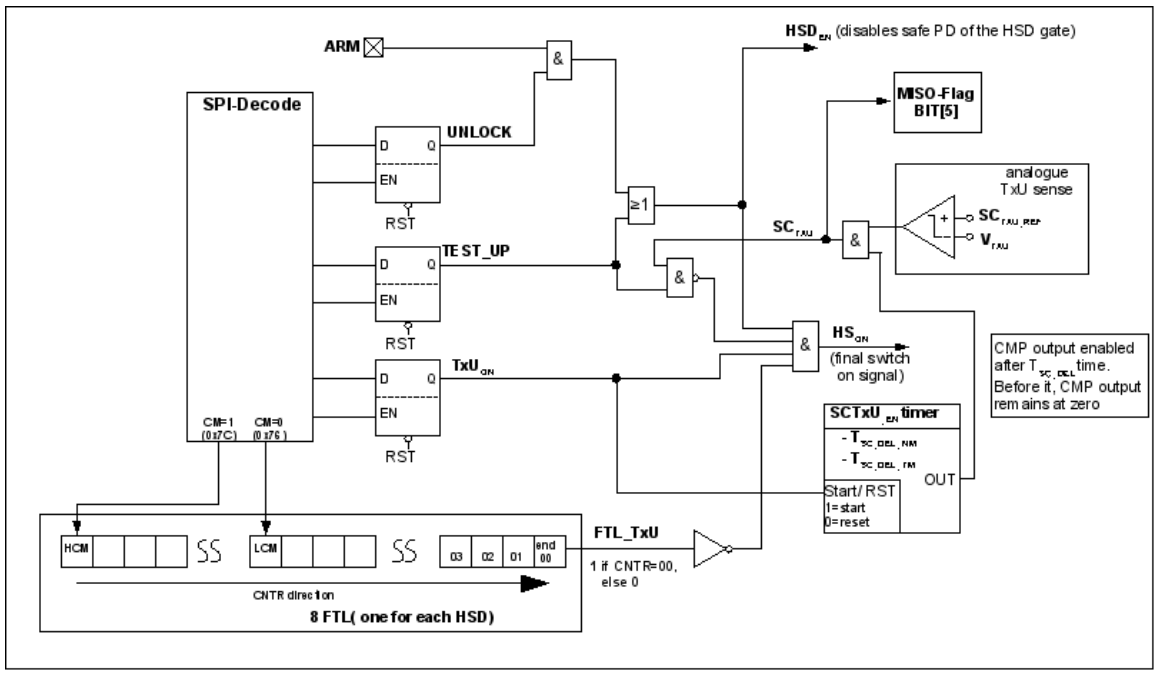


Fig. 11 HSD CTR-Module

The HSD control loop consists of:
- external *ARM* signal.
- *UNLOCK* Latch set by SPI CMD (Reset conditions are given in chapter 5.14).
- *TEST_UP* Latch set by SPI CMD (Reset conditions are given in chapter 5.14); TEST_UP allows the activation of HSD in Test Mode (current limit reduced) independently of ARM and CODELOCK signals.
- TxU_{ON} Latch set by SPI CMD; one for each driver (Reset conditions are given in chapter 5.14).
- SC_{TxU} signal coming from the driver output stage, which detects a short circuit to GND at the TxU pins.
- *FTL_TxU* signal coming from the Firing Time Limiter, one for each driver.

TxU Short circuit detection:
The short circuit comparator is enabled when the HSD is active.
In normal mode, as the LSD is activated prior the HSD, the SC comparator is enabled after a delay $T_{SC\_DEL\_NM}$, in order to let the HSD conducting a minimum current to allow the TxU pin exceeding the SC comparator threshold. Then, if during deployment, a SC condition is detected, the SC_TxU flag is set in the MISO register (but the HSD is not deactivated).
In Test Mode, in order to reduced as much as possible the energy provided to the squib in case in intermittent SC to GND, the SC comparator is activated without any delay ($T_{SC\_DEL\_TM}$ = 0µs). As soon as a SC condition is detected, the SC_TxU flag is set in the MISO register and the HSD is deactivated.
The timing diagram is shown in Fig. 12

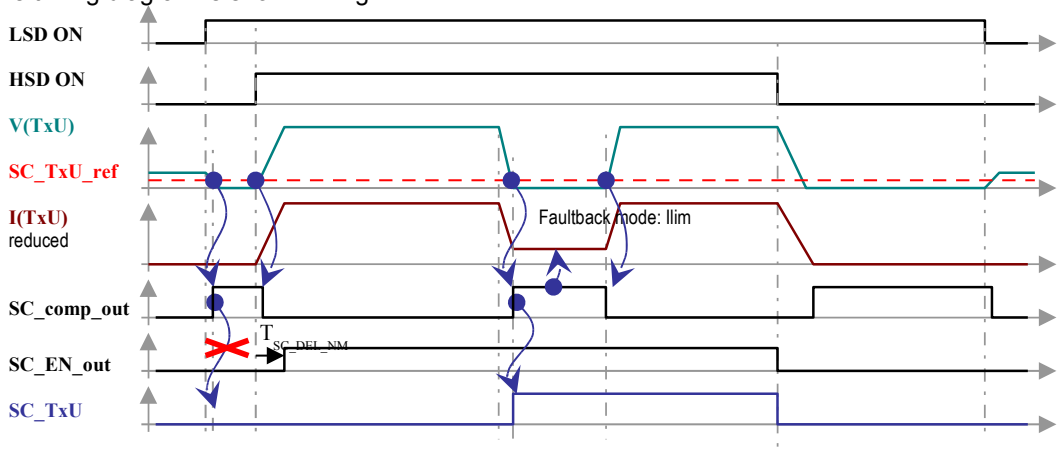


Fig. 12 Timing diagram SC detection for deployment mode

All 8 SC_{TxU} signals are summarized in one MISO status Bit. (see chapter 5.4.5).
The parameter $T_{SC\_EN\_NM}$ is given in *5.11.2.*

Firing Time Limiter (FTL):
The Firing Time Limiter (FTL) is realized as a backward counter. The start value is given by the according current mode (LCM/HCM), configurable by SPI. The Counter is active during Deployment mode and Test-Up Mode. During TEST-Up Mode, the counter value is coupled to the selected current modes (SPI CMD's 0x76 or 0x7C), too. The principle of the state transitions of the counter is sketched in Fig. 13.

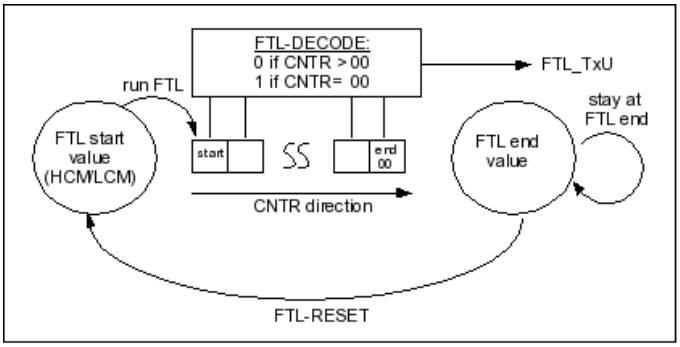


Fig. 13 FTL state transition

The FTL RESET can be done by:
- CODELOCK Reset pulse (0x70 or 0x71, see chapter 5.3) or
- SPI Reset pulse (0x4B, see chapter 5.3) or
- SPI TxU_off CMD or
- Global power on reset pulse (see chapter 5.3) or
- SPI FTL_RESET CMD (0xE7,no driver have to be activated here. CMD is rejected during "UNLOCK"-state)

The FTL is started by:
- SPI TxU_on CMD :
  The counter starts by the *run_FTL* signal, which is activated with the according *HSD_ON* CMD from the SPI decoder. The counter activation is independent from an active or not active state of *ARM* or *UNLOCK*. It is only started by the HSD driver activation CMD in normal deployment mode or in Test-Up Mode
- SPI FTL_ACTIVATE CMD (0xE5) for test purpose without a driver activation.
  (CMD is rejected during "UNLOCK"-state)

After reaching the counter end value (00), the FTL output is switched to logic high level and remains there until a FTL RESET is explicitly triggered. The counter is not re-started if additional TxU_on CMD's are sent.

For test purpose, all 8 FTL outputs are summarized in a "OR" and an "AND" combination. These two logical outputs can be switched to the AMX output by the S1 Multiplexer (see 5.10). There are two methods to check the FTL-timer in application:
- in TEST_UP-MODE by activating each HSD individually with reduced I_{LIM} and observe the AMX output switching from logical low to high level. For a single transistor activation the FTL_OR output has to be selected. Whereas for a parallel activation of all 8 HSD (two CMD's needed here) the FTL_AND combination can be selected to determine the longest FTL-Counter value.
- in FTL_TEST modes (0xE5). Here all 8 FTL's are activated at the same time. Observing the AMX transition from logical low to high level exhibits the maximum (FTL_AND) or the minimum (FTL_OR) Counter time. In this mode no driver activation is necessary.

The FTL_OR and FTL_AND output scheme is given in Fig. 14 below:

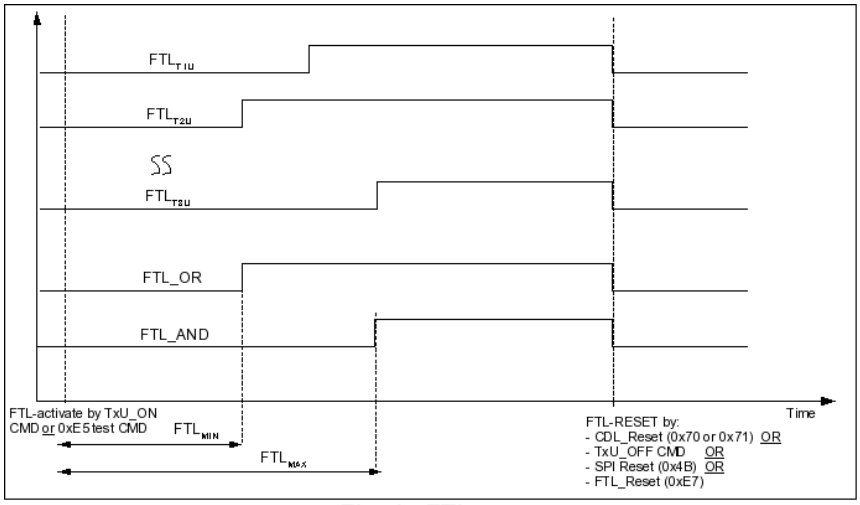


Fig. 14 FTL test

To activate the HSD in deployment mode, following signals have to be set:
- CODELOCK to be opened by SPI CMD (0x71)
- ARM pin to be set to logical high level
- Finally switching on the driver by the according SPI CMD (TxU_ON)

The driver will be switched off automatically by FTL or can be switched off externally by µP with the according TxU_OFF CMD by SPI. A short circuit event at the TxU during switch on phase, will not disable the HSD, but reduce the current limitation value. After the SC disappears again, the current limitation value is regulated to the nominal, intended value again (for more details see chapter 5.11). The short circuit event is visible at the MISO output frame in this case.

To activate the HSD in TEST_UP-Mode following signals have to be set:
- TEST_UP to be set by SPI CMD (0xE3)
- Finally switching on the driver by the according SPI CMD

The driver will be switched off automatically by FTL or can be switched off externally by µP with the according TxU_OFF CMD by SPI in TEST_UP mode, too. To limit the energy applied to the Squib during transient short circuit to GND, the HSD will be switched off immediately, if the TxU drops below the threshold SC_{TxU_REF} (see chapter 5.11.1). If the SC event disappears again, as during pulsed short circuit to GND, the driver will be activated again until the FTL timer or a SPI Driver off CMD deactivates the HSD. The short circuit event is visible at the MISO output frame in this case, too.

5.7.2 LSD Control Module

The LSD control can be separated into two different modes:
- Deployment Modes (NM)
- Switch Test Mode with reduced current level (TEST_LOW Mode)

The principle of the HSD control module is shown in pictures Fig. 15 below.

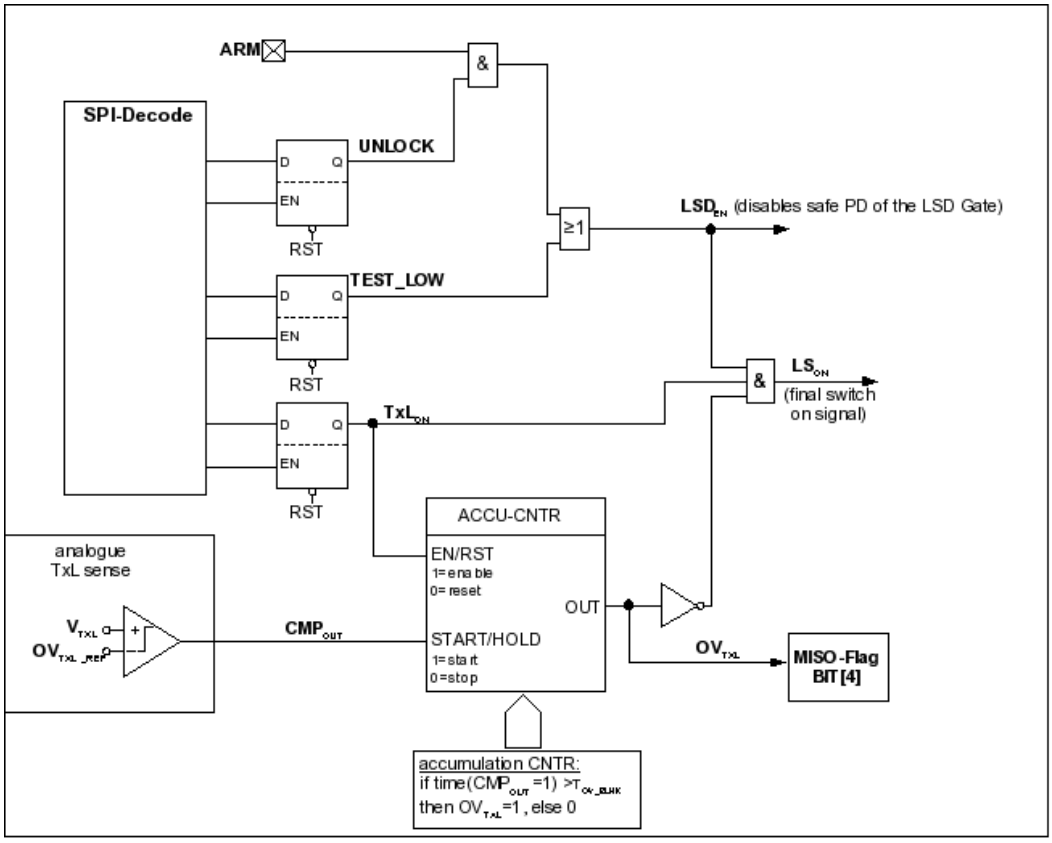


Fig. 15 LSD CTR-Module

The LSD control loop consists of:

- external *ARM* signal.
- *UNLOCK* Latch set by SPI CMD (Reset conditions are given in chapter 5.14).
- *TEST_LOW* Latch set by SPI CMD (Reset conditions are given in chapter 5.14), allow the activation of the LSD in Test Mode (with reduced I_{LIM}), independently of ARM and UNLOCK signals.
- TxL_{ON} Latch set by SPI CMD; one for each driver (Reset conditions are given in chapter 5.14).
- OV_{TxL} signal coming from the over voltage detection at the TxL.

TxL Short circuit detection:
In Normal Mode (deployment), the over voltage detection will shut off the driver after a specified time $T_{OV\_BLNK\_TXL\_NM}$, and set the flag OV_{TXL} in MISO register. To withstand pulsed short circuits to battery, there is a timer implemented, counting the time duration, in which the TxL voltage exceeds the over voltage detection threshold OV_{TxL_REF}. The timer is enabled with the TxL_{ON} CMD and is reset with a TxL_{OFF} CMD. The start and stop function of the Counter is then directly triggered by the comparator output. CMPOUT=high means the Counter is running, whereas CMPOUT=low means the Counter is halted but not reset and will be started from same position again if the CMPOUT goes to high again. Thus a thermal overload of the LSD will be avoided if more than one TxL_{ON} CMD's are sent, like it is done for overlapping switch on scenarios of different channels.
In Test-Low Mode, in order to reduced as much as possible the energy provided to the squib in case of intermittent SC to battery, the over voltage detection will shut off the LSD driver as soon as an OV condition is detected ($T_{OV\_BLNK\_TXL\_TM}$ = 0µs), and the OV_{TxL} flag is set in the MISO register.
The Low Side Driver remains in Off state, even if the OV condition disappears again.

The over voltage flags of all 8 channel are summarized in one MISO status register (BIT[4], see chapter 5.4.5 for a more detailed description).

To activate the LSD in deployment mode, following signals have to be set:
- CODELOCK to be opened by SPI CMD (0x71)
- ARM pin to be set to logical high level
- Finally switching on the driver by the according SPI CMD (TxL_ON)

Important: No automatically switch off available for the LSD. The driver has to be switched off externally by µP with the according SPI CMD.

To activate the LSD in TEST_LOW-Mode following signals have to be set:
- TEST_LOW to be set by SPI CMD (0xEC)
- Finally switching on the driver by the according SPI CMD

To limit the pulse energy applied to the squib during transient short circuits to battery in Test Mode the $T_{OV\_BLNK\_TM}$ is set to 0µs. By this the LSD will be kept switched off also if the driver activation in TEST_LOW Mode coincides with a static short circuit to battery. The short circuit event is visible at the MISO output frame in this case.

5.7.3 General considerations for test mode activation TEST_UP/ TEST_LOW

Activating of TEST_UP or TEST_LOW mode will set an internal signal *TM* , like sketched in Fig. 16 below. This internal signal reduces the internal current references for the HSD and LSD current limitation units to the test-mode level. Additionally this signal is used to limit the maximum gate voltage of all HSD during a TEST_UP activation. (see chapter 5.11).

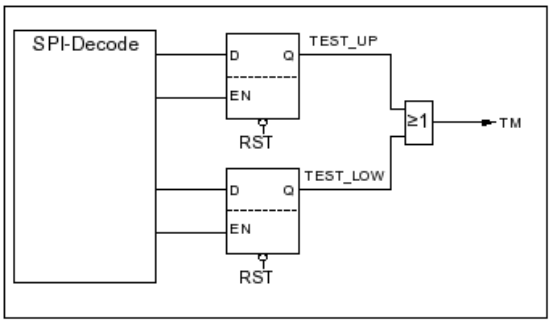


Fig. 16 Internal TM signal

It is not possible to activate the HSD and LSD switch test at the same time. They are locking each other by hardware.
Sending SPI TEST_Up after SPI TEST_Low, the Test mode is switched from the low side to the high side drivers and vice versa.
It is not possible to override low side and high side drivers at the same time. This implies that the (*TEST_UP|TEST_LOW)* register contents can be (0|0),(0|1),(1|0) but never (1|1). The registers can be switched to the analogue output AMX by the according SPI CMD (see more detailed description in chapter 5.14 (SPI-CMD list) and chapter 5.10 (Diagnosis via AMX pin).

5.8 Recommended firing sequence

The following timing diagrams in Fig. 17 shows exemplarily the recommended sequence for firing a single squib.
A synchronous firing of two or more groups of squibs and delayed firing of two or more groups of squibs is also possible. (see 4.2 for maximum allowed SOA conditions).

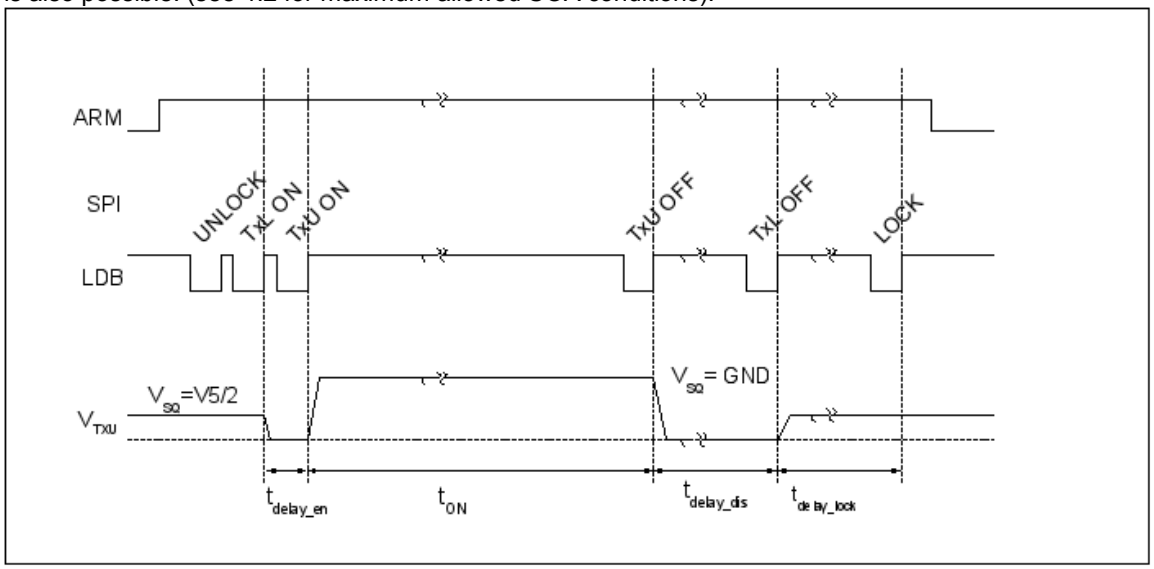


Fig. 17 LSD CTR-Module

It's required to activate at first the LS-driver and to disable at first the HS-driver. Because the Firing Time Limiter (FTL) will automatically switch off the HSD, it is not mandatory to sent the HSD switch off command. For the LSD a switch off CMD is mandatory.

It's allowed to fire on any channel independently (activating or disabling the driver channels, while the fire current is already flowing on other channels). The time t_{delay_dis} (time between TxUoff and TxLoff) has to be at least > 200µs, to ensure a safe shut off of the HSD first. The time t_{delay_en} (time between TxLon and TxUon) has to be ≥ 2µs. The delay t_{delay_lock} between the TxLoff CMD and the *LOCK* CMD has to be greater than $T_{off\_del,NM}$ specified in 5.12.2, item 3.

It is not recommended to activate or deactivate finally the drivers via the pins ARM or MRB, or by the SPI-CMD's *LOCK*/*UNLOCK* or *SPI_RESET,* because here the internal slew rate control of the drivers is not active. This can lead to high transients, when firing into inductive loads.

If the *ARM*-Pin is delayed after the TxU_ON CMD, there is no enlargement of the FTL duration. The FTL-counter is only triggered by TxU_On CMD, not by the ARM low to high transition.

5.9 Reference Resistance RREF & Squib resistance diagnosis

- External pin used for squib resistance reference measurement
- internal reference current source I_{REF_SQUIB} can be switched to RREF or the TxU pins with S4 multiplexor by according SPI CMD's. (see chapter 5.10)
- $I_{REF40mA}$ current source supplied by external U1-pin via 8V limiter V_{8_IREF}
- Diagnosis loop closed by activated LSD in TEST_LOW Mode.
- External squib difference voltage to be amplified by AMX amplifier and switched to AMX output Pin.
- external RREF voltage to be amplified by AMX amplifier and switched to AMX output Pin.
- Possibility to detect an open PGND connection caused by bond wire demolition or open pin.

The principle of the squib resistance diagnosis is shown in Fig. 18.

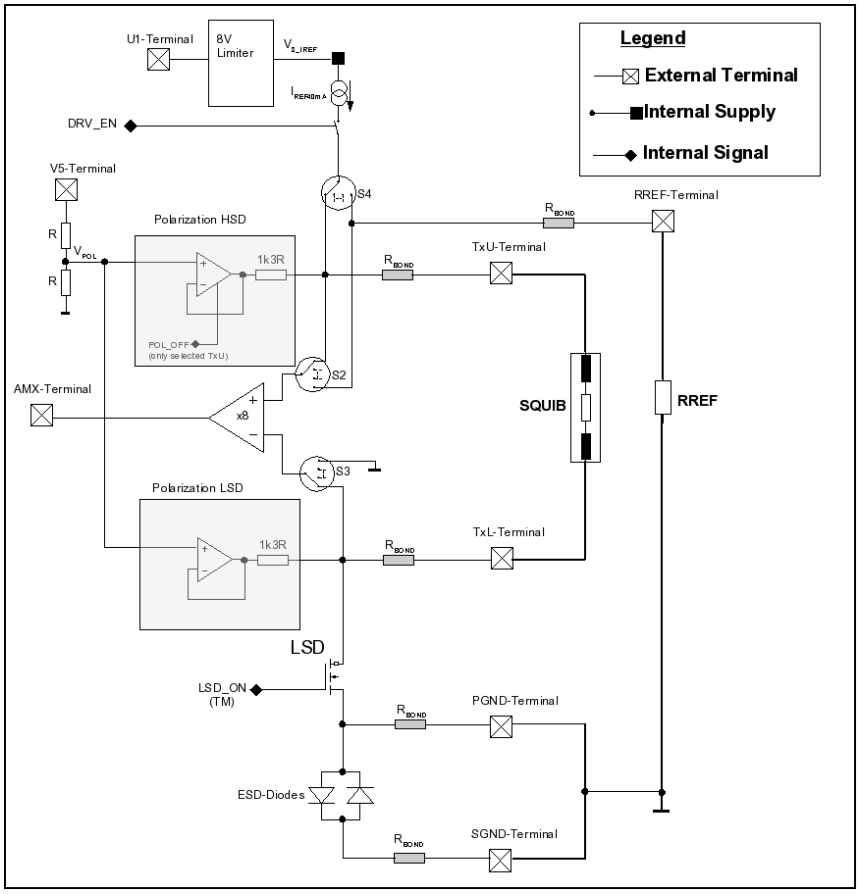


Fig. 18 Squib resistance diagnosis

Measurement principle:

The $I_{REF40mA}$ reference current source can be switched by multiplexor S4 to the external pin *RREF* or to the squib-lines *TxU.* The current loop in the squib-path can be closed by activating the Low Side Driver (LSD) connected to the according *TxL* pin under test mode (TM) condition. The current limitation of the LSD in TM is always larger than the internal 40mA current source. **Because of the over voltage detection at the TxL pins in TM ($T_{OV\_BLNK\_TxL\_TM}$=0, see chapter 5.12.2) it is mandatory to activate first the LSD and then the current source at the according TxU pin. Otherwise the OV condition at the TxL pin will prevent the driver activation.**

The current loop of the external reference resistor *RREF* is given by the grounded structure itself.

The difference voltage drop of *RREF* and of the squib-resistors can be switched by the multiplexors S2 and S3 to the internal amplifier. The amplifier output is visible at the *AMX*-pin.

For the voltages at the amplifier inputs following equations are valid:

1) $I_{REF40mA} \rightarrow$ RREF; $V_+ \rightarrow$ RREF; $V_- \rightarrow$ GND : $(V_+ - V_-) = I_{REF40mA} \cdot (R_{BOND\_RREF} + RREF)$
2) $I_{REF40mA} \rightarrow$TxU; $V_+ \rightarrow$ TxU; $V_- \rightarrow$ TxL : $(V_+ - V_-) = I_{REF40mA} \cdot (R_{BOND\_TxU} + R_{BOND\_TxL} + R_{SQUIB})$
   with R_{BOND_MAX}=100mΩ, given by design, not tested during production test.

At all *TxU* and *TxL* pins, polarization units are connected inside the IC, used for the leakage measurements and to avoid floating nodes at the squib feed and squib return lines. These polarization units consists of a buffer, forcing a bias voltage over a 1.3kΩ resistor to the *TxL* and *TxU* lines. Due to the fact that the LSD activation in TM will cause a CMIR of the measurement close to GND-level, the polarization buffer at the HSD would contribute an additional error current into the squib.

To eliminate this, the buffer of the selected *TxU* is disabled automatically by the same SPI-CMD, which activates the $I_{REF40mA}$ at the selected channel (see chapter 5.14 for the SPI-CMD-list).

The buffer output current of the TxL polarization unit will shift the CMIR range of the measurement, but will not influence the difference voltage measurements. Consequently the buffer at the TxL is not disabled.

Detection of an open Power Ground (PGND):

The 40mA current source can be used to detect a bond wire demolition at each LSD *PGND* pin. In this case the ESD diode between internal PGND pad and system Ground (SGND) will trace the $I_{REF40mA}$ current source. Each LSD Source Pin is only connected by a bond-wire to the according external PGND pin. There is no galvanic path to system ground *SGND* via substrate. Due to ESD protection each LSD Source pin has got a own protection circuitry of one diode in forward and one diode in backward direction to the system ground *SGND*. This is sketched in Fig. 18, too. Consequently the voltage drop at the TxL pin will be enlarged by a voltage U_D (0.3V..0.9V) of the ESD forward diode, if the bond wire is missing. Each TxL voltage can be switched to the AMX buffer by the according SPI-CMD. (see chapter 5.14). Thus following equations are valid for PGND connected and PGND not connected:

1) $V- = V_{AMX} = I_{REF40mA} \cdot (R_{ON\_LSD})$ for PGND connected

2) $V- = V_{AMX} = I_{REF40mA} \cdot (R_{ON\_LSD} + U_D)$ for PGND not connected

R_{ON_LSD} is given in chapter 5.12.1, here the TxL and PGND bond wires are included.

5.9.1 Squib resistance diagnosis, DC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Current at Squib resistance diagnosis	V_{RREF}<1V, V_{U1}>8V	$I_{REFSquib}$	-45		-30	mA
2	Load regulation error at squib resistance diagnosis.	V_{RREF}<1V, V_{U1}>8V	$\Delta I_{REF/TxU,LOAD}$	0		0.4	%
3	Channel error at squib resistance diagnosis.	[V_{RREF},V_{TxU}]<1V, V_{U1}>8V	$\Delta I_{REF,TxU}$	-1		+1.0	%

Table 24: Terminal RREF

- $\Delta I_{REF/TxU,LOAD}$ means maximum current error in percent between in output voltage range V_{RREF},V_{TXU}=[0V..1V]
- $\Delta I_{REF,TxU}$ means maximum current error in percent between the current reference switched to the output RREF and the current reference switched to the TxU outputs. Error results from residue leakage currents of the disabled polarization buffers at the output stages.

5.9.2 Squib resistance diagnosis, AC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Slew rate (10%-90%) for $I_{REF40mA}$ activation	V_{U1}>8V	$I_{REFSquib\_SR\_ON}$ 1.)			50	mA/µs
2	Slew rate (90%-10%) for $I_{REF40mA}$ deactivation	V_{U1}>8V	$I_{REFSquib\_SR\_Off}$ 1.)	-50			mA/µs

Table 25: $I_{REF40mA}$, AC

1.) ATE tested between 5mA and 30mA

5.10 AMX output and Diagnosis

The central unit of the diagnosis consists of an analog multiplexer(AMX), which selects a multitude of absolute and differential measurements within the output stage of the ASIC, a differential amplifier with the amplification A and an output buffer (AMX). The measured voltages are sent to the analog output (AMX), which is connected to one of the A/D inputs on the external µC. The multiplexer is represented by the six switches S1, S2, S3 and S4. The block circuitry is shown in Fig. 19.

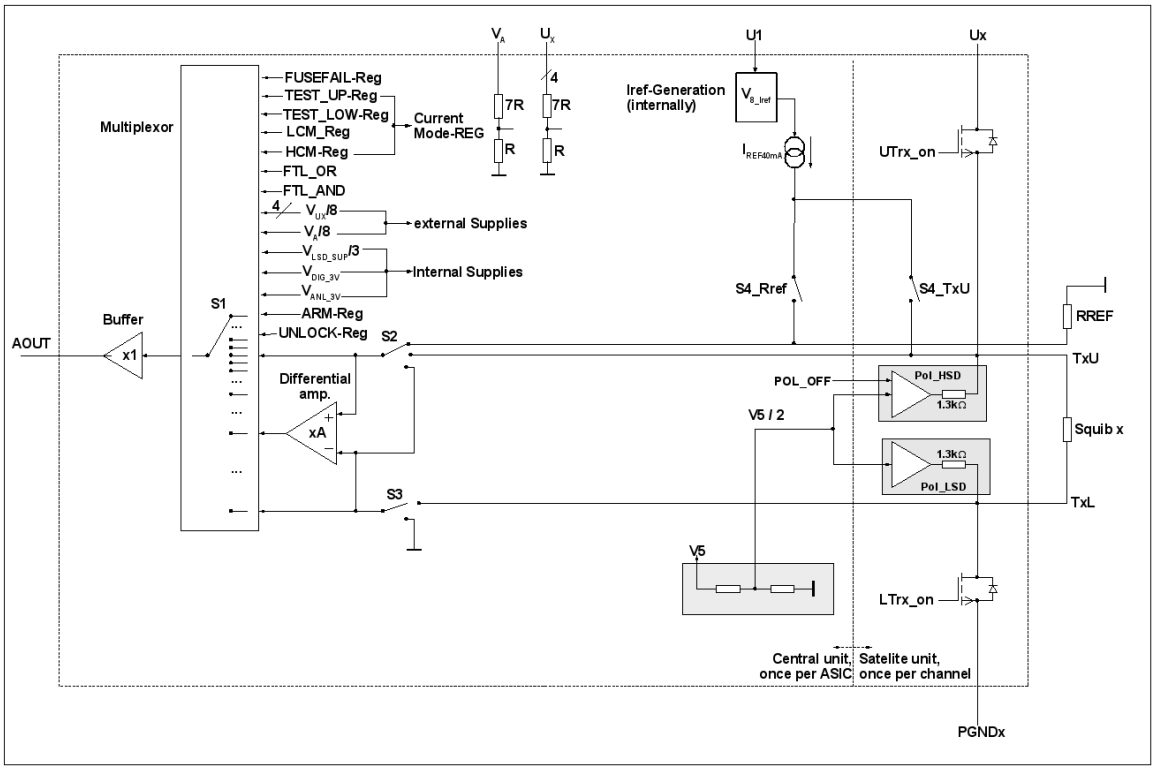


Fig. 19 Diagnosis block diagram

The following measurements can be performed during application:

- Leakage to ground/plus measurement
- Squib resistance measurement
- Lower transistor measurement
- Upper transistor measurement
- Arming measurement
- Unlock out measurement
- Internal and external supply measurement
- Firing Time Limiter (FTL) Test
- Read out of critical internal register values

5.10.1 Multiplexor S1-S4

Diagnosis signals visible at AMX pin

1.)Signals at multiplexer S1:

1. FUSEFAIL_REG: Logic_H ⟶ Error in trimming ARRAY
2. TEST_LOW_REG: Logic_H ⟶ Test lower side active
3. TEST_UP_REG: Logic_H ⟶ Test upper side active
4. LCM_REG: Logic_H ⟶ Low Current Mode (LCM) active
5. HCM_REG: Logic_H ⟶ High Current Mode (HCM) active
6. FTL_OR: Logic **OR** combination of all 8 Firing Time Limiter (FTL). If at least one timer has reached its CNTR end value, signal switched to logic high

	level. Otherwise maintains at logic low level (see Fig. 14 in chapter 5.7.1)
7. FTL_AND:	Logic **AND** combination of all 8 Firing Time Limiter (FTL). Switched to logic high level only if all 8 CNTR's end values are reached. Otherwise output maintains at logic low level. (see Fig. 14 in chapter 5.7.1).
8. V_{UX}/8, x=[1..4]:	V_{UX} with attenuation of 8
9. V_A/8:	V_A with attenuation of 8
10. V_{LSDSUP}/3:	V_{LSDSUP} with attenuation of 3
11. V_{DIG}:	internal digital supply V_{DIG}
12. V_{ANL}:	internal analogue supply V_{ANL}
13. ARM_REG:	Logic_H ⟶ ARM is active
14. UNLOCK_REG:	Logic_H ⟶ UNLOCK is active
15. S2	Positive input of AMX Amplifier
16. S3	Negative Input of AMX Amplifier
17. $(V_+ - V_-) \cdot$ GAIN	Output of the AMX Amplifier

2.)Signals at multiplexer S2, V_+ non inverting input of the amplifier:

1. TxU, [x=1..8]:	output voltages at the HSD
2. R_{REF}:	positive pin of external R_{REF} resistor
3. V_-:	short non inverting input of the amplifier

3.)Signals at multiplexer S3, V_- inverting input of the amplifier:

1. TxL, [x=1..8]:	output voltages at the LSD
2. SGND:	connection to system ground

3.)Signals at multiplexer S4, 40 mA $I_{REFSQUIB}$ reference current source:

• IRREF:	$I_{REFSQUIB}$ to Pin RREF
• TxU:	$I_{REFSQUIB}$ to HSD outputs TxU, according TxU polarization buffer is disabled, too

5.10.2 Terminal AMX in Buffer Mode, DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Buffer Offset voltage	4.5V<V_5<5.5V; V_{IN} ≤ 100mV	V_{OS1,AMX_Buffer}	-30		30	mV
2	Buffer Offset voltage	4.5V<V_5<5.5V; V_{IN} > 100mV	V_{OS2,AMX_Buffer}	-20		20	mV
3	Buffer Output voltage range	-10µA<I_{LOAD}<+10µA	V_{Out,AMX_Buffer}	0.02		V_5-0.4	V
4	AMX leakage in Tristate 1.)	4.5V<V_5<5.5V; V_{AMX}<V_5	I_{Leak,AMX_Buffer}	-2.5		+2.5	µA
5	Buffer input voltage range	4.5V<V_5<5.5V	V_{IN,AMX_Buffer}	0.00		1	V_5
6	Buffer output impedance 1.)	4.5V<V_5<5.5V, -100µA<I_{AMX}<+100µA	R_{OUT,AMX_Buffer}	0.00		2.5	kΩ

Table 26: AMX in Buffer Mode

1) Valid in Buffer and amplifier mode

5.10.3 Terminal AMX in Buffer Mode, AC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	AMX settling time with 10mV error	4.5V<V_5<5.5V; Load at AMX: 100pF||R>1MΩ;	$T_{SET,\ Buffer}$ 1) 2.)			25	µs

Table 27: AMX in buffer mode, AC

1.) Not tested during production test, guaranteed by design.
2.) Settling time considers the propagation delay of the switches and the transition from HiZ to Low impedance.

5.10.4 Terminal AMX in Differential Amplifier Mode, DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	AMX Differential amplification	4.5<V_5<5.5V	A_{AMX_Amp}	7.80	8.00	8.20	
2	AMX DC Offset in amplification mode	4.5<V_5<5.5V	V_{DC,AMX_Amp}	0.40	0.60	0.80	V
3	AMX Output offset drift in amplification mode	4.5<V_5<5.5V; CMIR=[0V..1V]	V_{OS,AMX_Amp}	-15		15	mV
4	AMX Output voltage range in amplification mode	4.5<V_5<5.5V, -100µA<I(AMX)<+100µA	V_{OUT,AMX_Amp}	0.2		V_5 -0.4V	V
5	AMX Common Mode Input range in amplification mode	4.5<V_5<5.5V	$CMIR_{AMX\_Amp}$	0.00		1.00	

Table 28: AMX in differential amplifier mode, DC

5.10.5 Terminal AMX in Differential Amplifier Mode, AC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	AMX settling time with 10mV error	4.5V<V_5<5.5V; Load at AMX: 100pF||R>1MΩ	T_{SET, AMX_Amp} 1) 2.)			50	µs

Table 29: AMX in differential amplifier mode, AC

1) Not tested during production test, guaranteed by design
2) Settling time considers the propagation delay of the switches and the transition from HiZ to Low impedance.

5.10.6 AMX Diagnosis outputs,DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	AMX Buffer mode,internal 3.3V digital supply voltage	4.5V<V_5<5.5V, R_{AMX}>500kΩ	$V_{DIG,S1}$	3.0		3.6	V
2	AMX buffer mode,internal 3.3V analogue supply voltage	4.5V<V_5<5.5V, R_{AMX}>500kΩ, all Driver off	$V_{ANL,S1}$	3.0		3.6V	V
3	AMX buffer mode,internal Logic output high level	4.5V<V_5<5.5V, R_{AMX}>500kΩ	$V_{LOG\_H,S1}$	2.4			V
4	AMX buffer mode,internal Logic output low level	4.5V<V_5<5.5V, R_{AMX}>500kΩ	$V_{LOG\_L,S1}$			0.2	V
5	AMX Buffer mode,internal supply voltage V_{LSDSUP}	4.5V<V_5<5.5V, V_{U1} >8V R_{AMX}>500kΩ	$V_{LSDSUP/3,S1}$	6.0/3		9.3/3	V
6	Attenuation of U_X measurement	4.5V<V_5<5.5V, x=[1..4], R_{AMX}>500kΩ	$A_{UX/8}$	7.6	8.0	8.4	
7	Attenuation of VA measurement	4.5V<V_5<5.5V, R_{AMX} >500kΩ	$A_{VA/8}$	7.6	8.0	8.4	

Table 30: AMX Diagnosis

5.11 Terminal TXU, High Side Driver Outputs

- Provide HSD deployment current regulation output (configurable in LCM, HCM and test mode)
- Internal polarization voltage and impedance for leakage detection
- Short circuit to GND detection. The TxU short circuit detection is active during normal mode and test mode. The SC_{TXU} threshold is given in 5.11.1. The TxU SC-comparator output is propagated to the logic. After the time T_{SC_DEL} is exceeded, the SC event is latched in a register an can be read out at the SPI output. For a register reset a clear CMD must be set. (see chapter 5.14).
  SC to GND protection in TM:
  To provide a fast switch off during TM in case of a short to GND, the Driver gates will be pulled down immediately, when the TxU voltage drops below the SC threshold. Additionally the HSD gate voltage is clamped to V_{TXU_TM} during TM to minimize the short circuit pulse energy.
  SC to GND protection in NM (deployment):
  In case of short to GND during deployment, the current limitation loop will enter the “fallback” mode: the current limitation value will be reduced to reduce the PDISS of the driver. The “fallback” mode is triggered by an overdrive of the inner loop regulation, sketched by the signal “sat” in Fig. 20. while the voltage at the TxU pins drops below the nominal operating range given by the product of the the min. squib resistance and the HSD I_{LIM_MIN},. The different shapes of the HSD current regulation for different short circuit events to GND are sketched in Fig 23 below. The reduction of I_{LIM_TxU} is possible because the squib resistance is shorted by a parasitic short to GND at the TxU pin.
- 8 separate Firing Time Limiter (FTL) limit the maximum HSD switch on time, if the HSD switch off command is missing. Each counter (CNTR) is started with the according TxU_{ON} signal, triggered by the SPI switch on CMD. After reaching the counter limit, the internal FTL_TxU signal is switched to logic high level and the according HSD is switched off. The counter value is coupled to the adjusted current mode (LCM/HCM). For test purpose all 8 FTL outputs can be **or** and **and** combined and are visible at the AMX pin with the according SPI CMD set (see chapter 5.14).

Fig. 20 shows the principle of the HSD Ilim control unit.

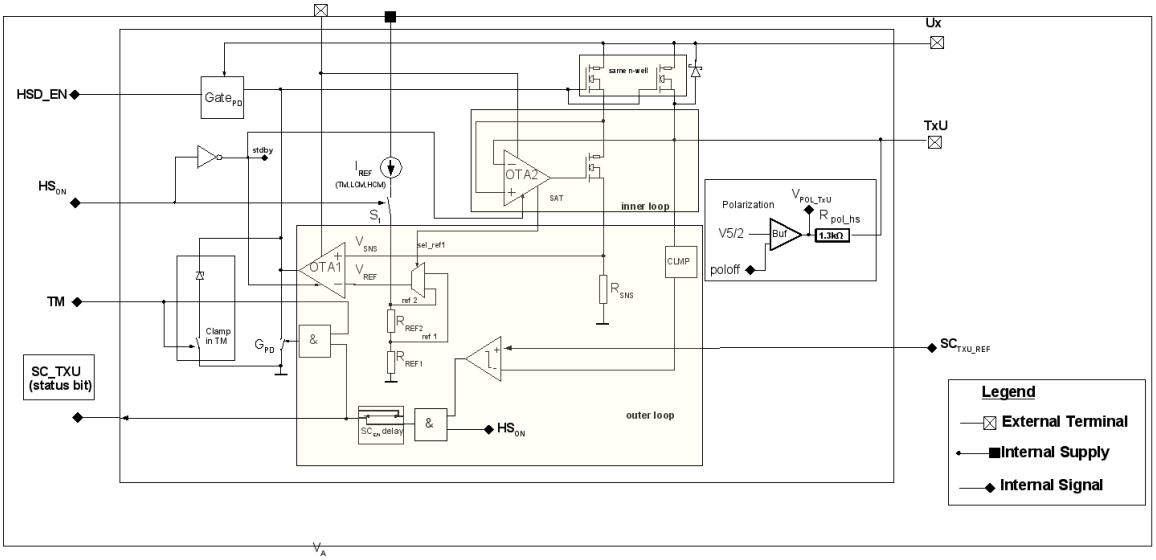


Fig. 20 TXU (HSD) Ilim-control block circuitry

Each driver is provided with a passive gate pull down structure unit, disabled during activation, and a gate to source clamping. The passive gate structure is a redundant (safety) feature of the HSD control module.
Both is sketched in Fig. 21 and Fig 22 below.
The HSD locking is suspended only if the internal *PORB* reset signal is at high level (see chapter 5.3). Additional either the TEST_UP mode have to be selected by an according SPI CMD or the *UNLOCK* and the *ARM* signals have to be at high level. In the first case the HSD can be activated under Test Mode conditions, where all complement Low side drivers are locked. In the second case the diver can be activated under normal firing conditions by an according SPI CMD.

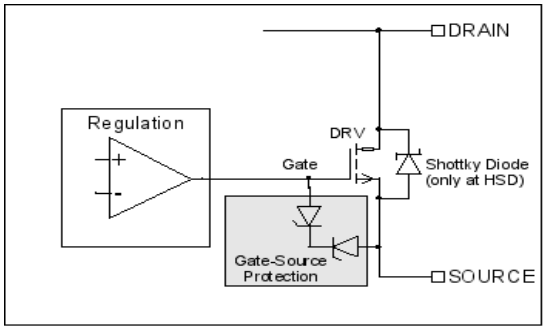


Fig. 21: Gate-source clamping

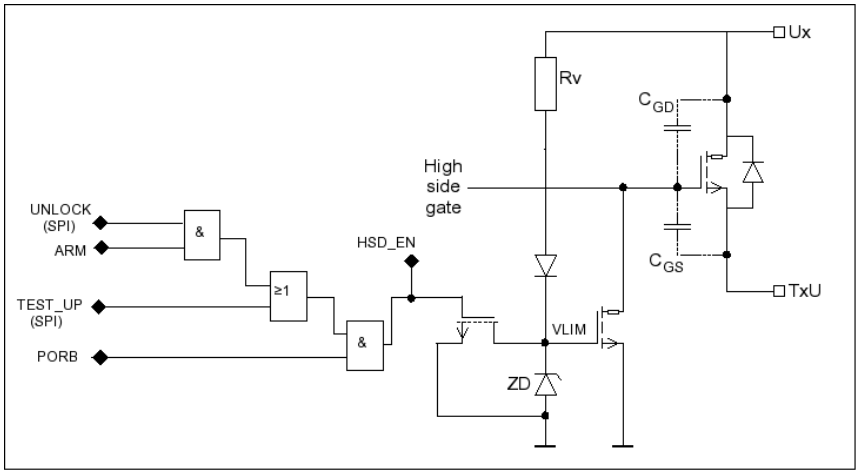


Fig 22 passive Gate PD structure

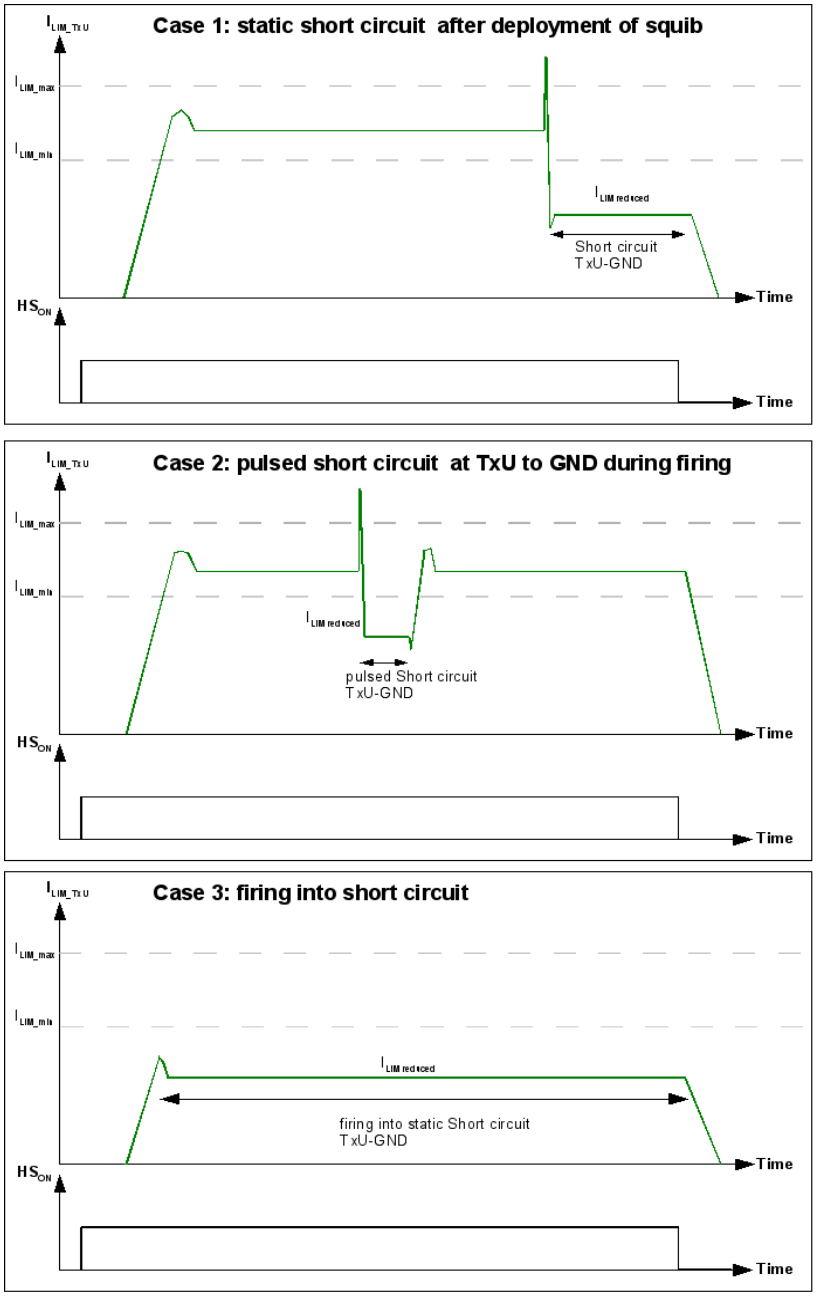


Fig 23 Reduced HSD_{ILIM} during SC to GND

5.11.1 TXU, DC Characteristics

Following general condition must be fulfilled unless otherwise stated:
- $V_A \geq (V_{txU}+8V)$ & $V_A \geq 12V$
- $4.5V<V_5<5.5V$
- $1.7\Omega < R_{SUIB} < 6\Omega$

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Internal polarization voltage	Driver and $I_{REF40mA}$ off $0 \leq V_{txU} \leq V_5$	V_{POL_TxU} 1.)	0.475		0.525	V_{V5}
2	Bias impedance TxU	Driver and $I_{REF40mA}$ off	R_{BIAS}	910	1300	1690	Ω
3	HSD Ron in LCM	I(TxU)=-1.2A for 2ms	Ron_{LCM} 2)	0.2		1.1	Ω
4	HSD Ron in HCM	I(TxU)=-1.75A for 500µs	Ron_{HCM} 2)	0.2		1.3	Ω
5	Current Limitation in HCM	12V<Ux<35V, V(TxU)>2V	$Ilim_{HCM}$	-2.52		-1.77	A
6	Current Limitation in LCM	8V<Ux<25V, V(TxU)>2V	$Ilim_{LCM}$	-1.82		-1.22	A
7	Current Limitation in TM	8V<Ux<35V, V(TxU)>2V	$Ilim_{TM}$	-150		-50	mA
8	Leakage on High Side Switch	Driver off,V_{POL_TxU} disabled, V_{UX}<35V & V(TxU) > 0V	$Ileak_{TxU}$	-100		+100	µA
9	TxU short circuit detection	HCM,LCM,TM, $8V<U_X<35V$	SC_{TXU_REF}	1.1	1.5	1.9	V
10	TXU voltage range during Test Mode	TM active, $8V<U_X<35V$	V_{TXU_TM}	5.1		10	V

Table 31: Terminals TxU x=[1..8] DC characteristics

1) guaranteed by design, internally signal tested by open TxU pin.
2) R_{DSON} are specified for the external package pins; so bond wire impedance's are included.

5.11.2 TXU, Dynamic Characteristics

Following general condition must be fulfilled unless otherwise stated:
- $V_A \geq (V_{txU}+8V)$ & $V_A \geq 12V$
- $4.5V<V_5<5.5V$
- Range for R_{SUIB}, C_{EMC}, R_W and L_W given in chapter 1.2.

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	HSD Slew rate for activating/deactivating in LCM	V_{UX}>8V	$SR_{TxU,LCM}$	10		200	mA/µs
2	HSD Slew rate for activating/deactivating in HCM	V_{UX}>12V	$SR_{TxU,HCM}$	10		200	mA/µs
3	HSD activation delay in LCM.	V_{UX}>8V, Delay between ↑LDB and I_{lim}>1.2A	$T_{on\_del,LCM}$			120	µs
4	HSD activation delay in HCM	V_{UX}>12V, Delay between ↑LDB and I_{lim}>1.75A	$T_{on\_del,HCM}$			120	µs
5	HSD deactivation delay in LCM.	V_{UX}>8V, Delay between ↑LDB and I_{lim}<100mA	$T_{off\_del,LCM}$			120	µs
6	HSD deactivation delay in HCM	V_{UX}>12V, Delay between ↑LDB and I_{lim}<100mA	$T_{off\_del,,HCM}$			140	µs
7	HSD activation delay in Test Mode	Delay between ↑LDB and V_{TxU}>4.5V	$T_{on\_del,TM}$ 3.)			120	µs
8,1	TxU short circuit enable delay in normal mode, controlled by the logic. Time to consider the delay between switch on CMD and HSD_{ILIM} in specified range.	LCM, HCM Time between ↑LDB (HSD_{ON}) and SC-CMP output valid for the logic	$T_{SC\_DEL\_NM}$ 1.)	163 $(1/F_{OSC\_max})$ *128*11		208 $(1/F_{OSC\_min})$ *128*12	µs
8,2	TxU short circuit enable delay in Test Mode. No delay due to limit max. pulse energy applied to squib during fault modes.	TM, Time between ↑LDB (HSD_{ON}) and SC-CMP output valid for the logic	$T_{SC\_DEL\_TM}$ 2.)		0		µs
9,1	Firing time limiter in Test Mode if current mode register is set to LCM; one for each HSD, controlled by the logic.	Time between ↑LDB (HSD_{ON}) and internally switch off	$FTL\_TxU_{TM\_LCM}$	2.128 $(1/F_{OSC\_max})$ *128*143	2.288 $(1/F_{OSC\_nom})$ *128*143	2.491 $(1/F_{OSC\_min})$ *128*144	ms

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
9,2	Firing time limiter in Test Mode if current mode register is set to HCM; one for each HSD, controlled by the logic.	Time between ↑LDB (HSD_{ON}) and internally switch off	$FTL\_TxU_{TM\_HCM}$	625 ($1/F_{OSC\_max}$) *64*84	672 ($1/F_{OSC\_nom}$) *64*84	736 ($1/F_{OSC\_min}$) *64*85	µs
10	Firing time limiter in LCM, one for each HSD, controlled by the logic.	Time between ↑LDB (HSD_{ON}) and internally switch off	FTL_TxU_{LCM}	2.128 ($1/F_{OSC\_max}$) *128*143	2.288 ($1/F_{OSC\_nom}$) *128*143	2.491 ($1/F_{OSC\_min}$) *128*144	ms
11	Firing time limiter in HCM, one for each HSD, controlled by the logic.	Time between ↑LDB (HSD_{ON}) and internally switch off	FTL_TxU_{HCM}	625 ($1/F_{OSC\_max}$) *64*84	672 ($1/F_{OSC\_nom}$) *64*84	736 ($1/F_{OSC\_min}$) *64*85	µs

Table 32: Terminal TxU x=[1..8] Dynamic characteristics

1) Tested by ATPG scan test during ELMOS production test
2) If TEST_UP Mode is activated directly into a short circuit, no output current will be delivered from the driver. If the SC is applied dynamically during an activated driver under TEST_UP mode, the HSD gate will be discharged immediately.
3) The T_{ON}-delay is also valid for the visibility at the analogue output AMX, when the switches are set before the HSD activation in TM.

The definition of the dynamic parameters related to slew rate and delay's is illustrated also Fig. 24 in below.

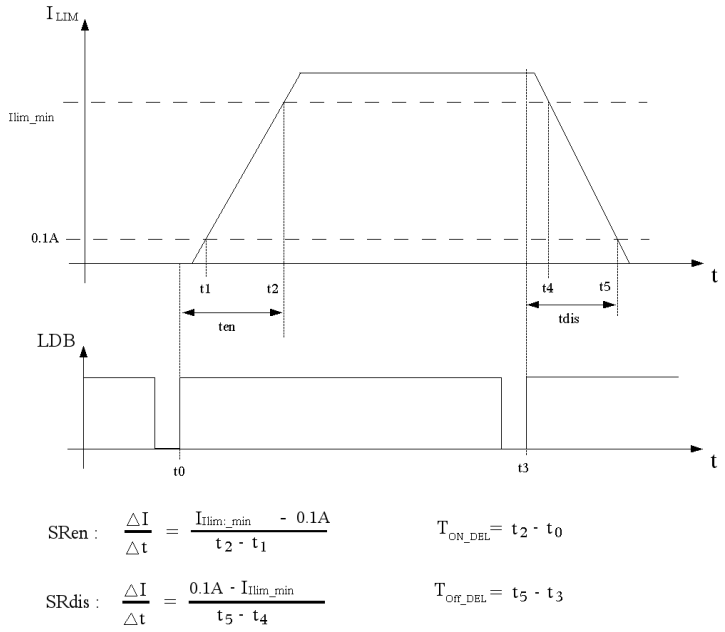


Fig. 24 Definition of dynamic parameters

5.12 TXL, Low Side Driver Outputs

- TxL terminal is connected to LSD drain pin.
- Provide LSD deployment current output (configurable in Normal Mode and Test Mode)
- Internal polarization voltage and impedance for leakage detection
- TxL over voltage detection with blank-out timer T_{OV_BLNK} and LSD switch off (short to battery protection). The OV detection is active during LSD activation in normal mode and in test mode. In test mode an over voltage event at TxL will switch off the driver immediately to minimize the applied energy at the squib. In normal modes HCM and LCM the minimum switch on delay of the LSD has to be bridged. The counter is triggered with an OV condition and is halted if OV condition disappears. (→ pulsed shorts to V_{BAT}). The OV event is latched and frozen in a register and can be read out at the SPI output (see chapter 5.4.5). For a register reset a clear CMD must be set (see chapter 5.14).

Fig. 25 shows the principle of of the LSD Ilim regulation loop.

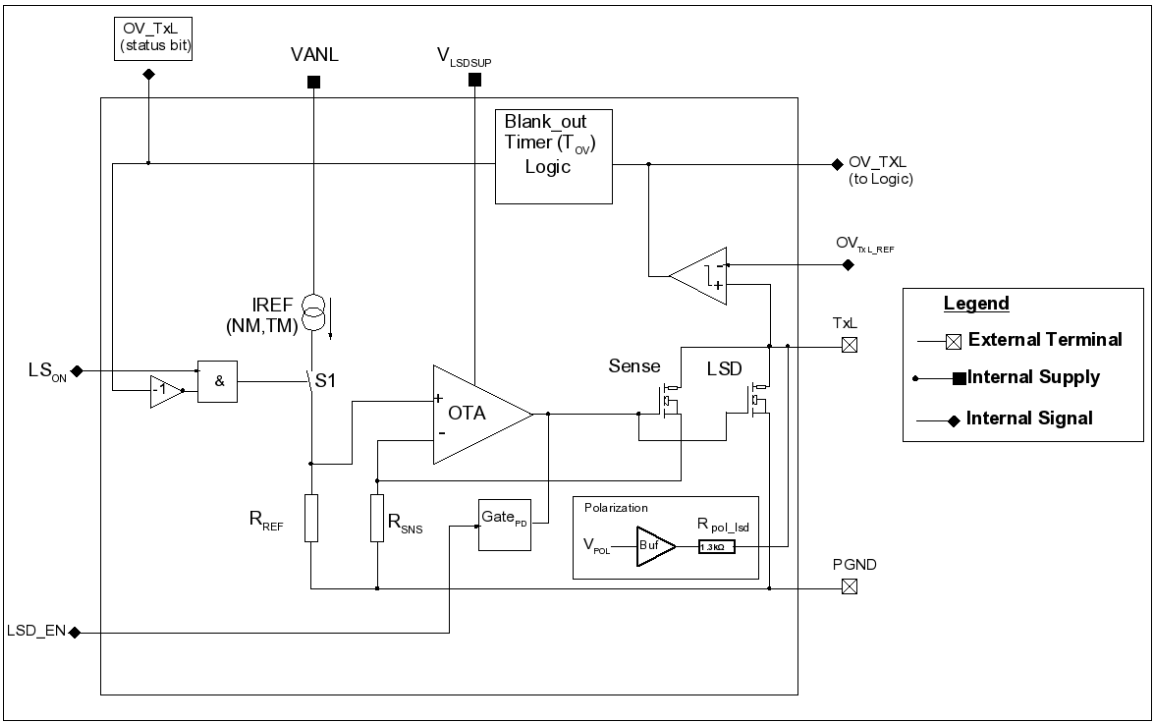


Fig. 25 TXL (LSD) Ilim control block

Each Low side driver is provided with a passive gate pull down structure unit, disabled during activation, and a gate to source clamping. The passive gate structure is a redundant (safety) feature of the LSD control module.
Both is sketched in Fig. 26 and Fig. 27. The LSD locking is suspended only if the internal *PORB* reset signal is at high level (see chapter 5.3). Additional either the TEST_LOW mode have to be selected by an according SPI CMD or the *UNLOCK* and the *ARM* signals have to activated. In the first case the LSD can be activated under Test Mode conditions, where all complement High side drivers are locked. In the second case the Low side driver can be activated under normal, firing conditions by an according SPI CMD.

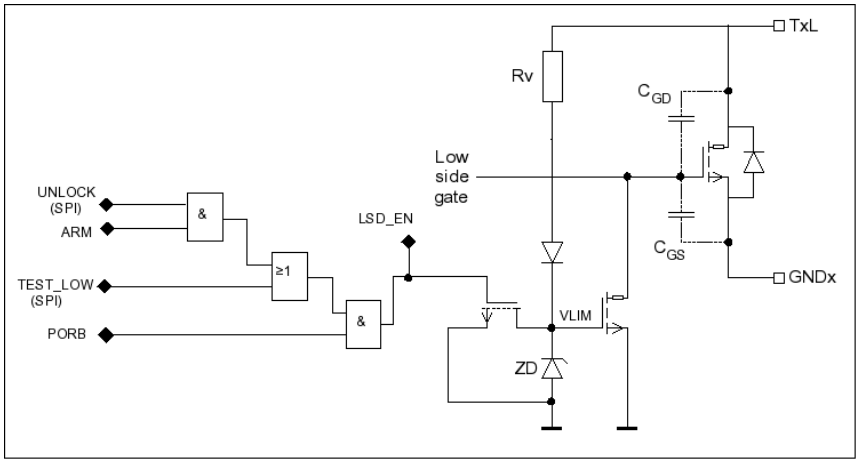


Fig. 26 LSD: Passive Gate PD

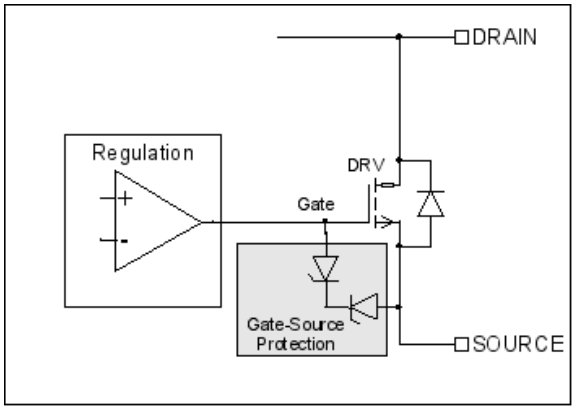


Fig. 27 LSD: LSD gate protection

5.12.1 TXL, DC characteristics

Following general condition must be fulfilled unless otherwise stated:
- V_{U1}≥8V (to ensure V_{LSDSUP} in operating range)
- 4.5V<V_5<5.5V

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Internal polarization voltage	Driver and $I_{REF40mA}$ off 0≤ V_{TxL} ≤ V_5	V_{POL_TxL} 1.)	0.475		0.525	V_{V5}
2	Bias impedance TxL	Driver and $I_{REF40mA}$ off	R_{BIAS}	910	1300	1690	Ω

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
3	LSD Ron in LCM	I(TxL)=-1.2A for 2ms	Ron_{LCM} 2.)	0.2		2.1	Ω
4	LSD Ron in HCM	I(TxL)=-1.75A for 500µs	Ron_{HCM} 2.)	0.2		2.3	Ω
5	Current Limitation in Normal Mode	$I_{LIM\_LSD} > I_{LIM\_HSD}$, $V_{TXL} > (I_{LIM\_LSD} * R_{DSON\_LSD})$	I_{LIM_NM}	2		3.2	A
6	Current Limitation in Test Mode	$2V<V_{TXL}<6V$ or $6V<V_{TXL}<18V$ for $T_{ON} < T_{OV\_BLNK}$	I_{LIM_TM}	50		150	mA
8	Leakage on Low Side Switch	Driver off, V_{POL_TxL} disabled, $0V< V_{TxL}<35V$	$Ileak_{TxL}$	-100		+100	µA
9	Over voltage detection threshold	$T_{OV} > T_{OV\_BLNK}$	OV_{TXL_REF}	6		8	V

Table 33: Terminals TxL, x=[1..8]

1.) guaranteed by design, internally signal tested by open TxL pin.
2.) R_{DSON} are specified for the external package pins; so bond wire impedance's are included.

5.12.2 TXL, Dynamic Characteristics

Following general condition must be fulfilled unless otherwise stated:
- V_{U1}>8V (to ensure V_{LSDSUP} in operating range)
- $4.5V<V_5<5.5V$
- Range for R_{SUIB}, C_{EMC}, R_W and L_W given in chapter 1.2.

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	LSD slew rate for activating/deactivating in Normal Mode	$V_{TXL} > (I_{LIM\_LSD} * R_{DSON\_LSD})$	$SR_{TxL,NM}$	10		350	mA/µs
2	LSD activation delay in Normal Mode.	$V_{TXL} > (I_{LIM\_LSD} * R_{DSON\_LSD})$, delay between ↑LDB and I_{lim}>2.0A	$T_{on\_del,NM}$ 2.)			120	µs
3	LSD deactivation delay in Normal Mode	$V_{TXL} > (I_{LIM\_LSD} * R_{DSON\_LSD})$ delay between ↑LDB and Ilim<100mA	$T_{off\_del,NM}$			250	µs
4	LSD activation delay in Test Mode	Time between ↑LDB and V_{TXL} voltage <0.5V	$T_{on\_del,TM}$			100	µs
5,1	Over voltage blank out timer, one for each LSD; valid for LCM and HCM	$V_{TXL} > OV_{TXL}$, timer is halted if OV condition disappears	$T_{OV\_BLNK\_TxL\_NM}$ 1.)	122 / $(1/F_{OSC\_max})$ *32*33		147 / $(1/F_{OSC\_min})$* 32*34	µs

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
5,2	Over voltage blank out timer, one for each LSD; valid for TM	V_{TXL}> OV_{TXL}	$T_{OV\_BLNK\_TxL\_TM}$		0		µs

Table 34: Terminal TxL x=[1..8] Dynamic characteristics

1.) Tested by ATPG scan test during ELMOS production test
2.) The T_{ON}-delay is also valid for the visibility at the analogue output AMX, when the switches are set before the LSD activation in TM.

The definition of the dynamic parameters related to slew rate and delay's is illustrated in Fig. 28 below.

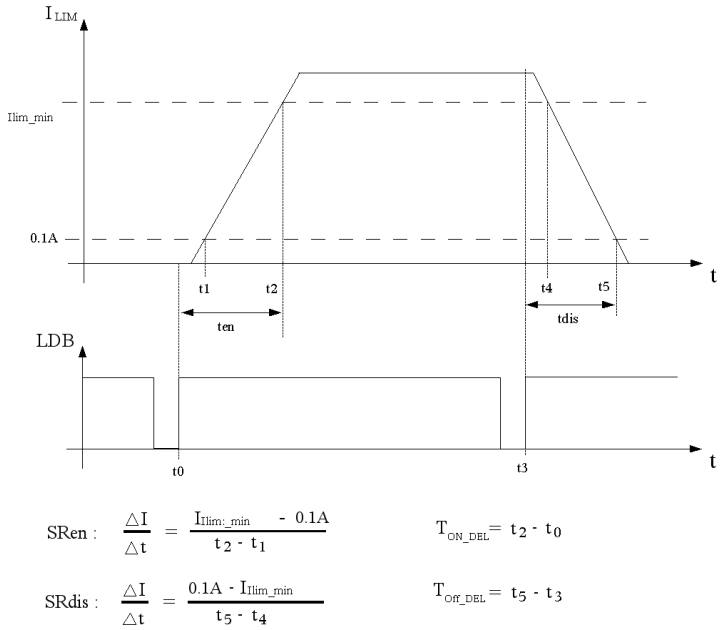


Fig. 28 Definition of dynamic parameters

5.13 Internal 8MHz oscillator

- internal free running oscillator
- supplied by internal V_{DIG} supply voltage
- calibrated parameter (see chapter 5.15)

5.13.1 OSC, Dynamic characteristics

No.	*Description*	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
1	Calibrated oscillator frequency, valid after successfully trimming read out.	4.5V<V_5<5.5V	F_{OSC_C}	7.4		8.6	MHz
2	Not calibrated oscillator frequency, valid during and after not successfully trimming read out.	4.5V<V_5<5.5V	F_{OSC_NC} 1.)	6.0		10.8	MHz

Table 35: Internal 8MHz Oscillator, AC

1) not tested during production test, guaranteed by design. Parameter is influencing time duration of the trimming array read out process. After this the oscillator is running in the calibrated mode.

5.14 SPI command code

- 8 Bit word divided into 4 bit address and 4 bit data
- [1)]ELMOS Test mode is entered by according SPI CMD **and** logic high level at Pin TEST. In application the TEST pin must be connected to GND.

Code[HEX]	*Address*	*Data*	*Description*	*POR*	*SPI-Reset*	*Unlock Out↑↓*
0x00-0x0F						
0x00	0 0 0 0	0 0 0 0	No operation (NOP)			
0x01-0x0B			ELMOS Test Modes [1)]			
0x0C			ELMOS Test Mode deactivates all polarization buffer outputs. This mode is used for the TxU and TxL leakage measurements to avoid buffer pull-up and pull down currents [1)]			
0x0D			ELMOS Test Mode deactivates OVTxL shut off at the LSD and disables the FTL-timer. To reset this test mode, the TEST-pin has to be connected to GND again. [1)]			
0x0E			ELMOS Test Mode entering the JTAG test mode [1)]			
0x0F			No operation (NOP)			
0x10-0x1F	0 0 0 1		HSD activation/deactivation T1U-T4U			
	0 0 0 1	- - - 0	deactivate T1U	●	●	●
	0 0 0 1	- - - 1	activate T1U			
	0 0 0 1	- - 0 -	deactivate T2U	●	●	●
	0 0 0 1	- - 1 -	activate T2U			
	0 0 0 1	- 0 - -	deactivate T3U	●	●	●
	0 0 0 1	- 1 - -	activate T3U			
	0 0 0 1	0 - - -	deactivate T4U	●	●	●
	0 0 0 1	1 - - -	activate T4U			
0x20-0x2F	0 0 1 0		HSD activation/deactivation T5U-T8U			
	0 0 1 0	- - - 0	deactivate T5U	●	●	●
	0 0 1 0	- - - 1	activate T5U			

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
	0 0 1 0	- - 0 -	deactivate T6U	●	●	●
	0 0 1 0	- - 1 -	activate T6U			
	0 0 1 0	- 0 - -	deactivate T7U	●	●	●
	0 0 1 0	- 1 - -	activate T7U			
	0 0 1 0	0 - - -	deactivate T8U	●	●	●
	0 0 1 0	1 - - -	activate T8U			

Table 36: CMD code for 0x00-0x2F, TxU activation/deactivation

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x30-0x3F	0 0 1 1		MUX S1 CTRL			
0x30	0 0 1 1	0 0 0 0	AMX → HiZ	●	●	
0x31	0 0 1 1	0 0 0 1	AMX → U1/8			
0x32	0 0 1 1	0 0 1 0	AMX → U2/8			
0x33	0 0 1 1	0 0 1 1	AMX → U3/8			
0x34	0 0 1 1	0 1 0 0	AMX → U4/8			
0x35	0 0 1 1	0 1 0 1	AMX → V+			
0x36	0 0 1 1	0 1 1 0	AMX → (V+ - V-) A_{AMX_Amp}			
0x37	0 0 1 1	0 1 1 1	AMX → V-			
0x38	0 0 1 1	1 0 0 0	AMX → ARM Signal			
0x39	0 0 1 1	1 0 0 1	AMX → UNLOCK-REG			
0x3A	0 0 1 1	1 0 1 0	AMX → GND			
0x3B	0 0 1 1	1 0 1 1	AMX → GND			
0x3C	0 0 1 1	1 1 0 0	AMX → GND			
0x3D	0 0 1 1	1 1 0 1	AMX → GND			
0x3E	0 0 1 1	1 1 1 0	AMX → V_{DIG}			
0x3F	0 0 1 1	1 1 1 1	AMX → FUSEFAIL-Reg			
0x40-0x4F	0 1 0 0		MUX S1 CTRL/SPI Reset			
0x40	0 1 0 0	0 0 0 0	AMX → V_{LSDSUP}/3			
0x41	0 1 0 0	0 0 0 1	AMX → VA/8			
0x42	0 1 0 0	0 0 1 0	AMX → V_{ANL}			

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x43	0 1 0 0	0 0 1 1	AMX → FTL_AND logic high level: all CNTR's limits reached. Otherwise logic low level visible at the AMX			
0x44	0 1 0 0	0 1 0 0	AMX → FTL_OR logic low level: all CNTR's still running. Otherwise logic high level visible at the AMX			
0x45	0 1 0 0	0 1 0 1	AMX → LCM-Reg			
0x46	0 1 0 0	0 1 1 0	AMX → HCM-Reg			
0x47	0 1 0 0	0 1 1 1	AMX → TESTDRL-Reg			
0x48	0 1 0 0	1 0 0 0	AMX → TESTDRH-Reg			
0x49	0 1 0 0	1 0 0 1	AMX → GND			
0x4A	0 1 0 0	1 0 1 0	AMX → GND			
0x4B	0 1 0 0	1 0 1 1	SPI-Reset			
0x4C	0 1 0 0	1 1 0 0	AMX → GND			
0x4D	0 1 0 0	1 1 0 1	CLR_STAT → clear MISO Status bits: (PWR_UP,OV_TxL,SC_TxU)			
0x4E	0 1 0 0	1 1 1 0	AMX → GND			
0x4F	0 1 0 0	1 1 1 1	AMX → GND			

Table 37: CMD code for 0x30-0x4F

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x50-0x5F	0 1 0 1		MUX S2 CTRL (V+)			
0x50	0 1 0 1	0 0 0 0	V+ → V-	•	•	•
0x51	0 1 0 1	0 0 0 1	V+ → T1U			
0x52	0 1 0 1	0 0 1 0	V+ → T2U			
0x53	0 1 0 1	0 0 1 1	V+ → T3U			
0x54	0 1 0 1	0 1 0 0	V+ → T4U			
0x55	0 1 0 1	0 1 0 1	V+ → T5U			
0x56	0 1 0 1	0 1 1 0	V+ → T6U			
0x57	0 1 0 1	0 1 1 1	V+ → T7U			
0x58	0 1 0 1	1 0 0 0	V+ → T8U			
0x59	0 1 0 1	1 0 0 1	V+ → RREF			
0x5A	0 1 0 1	1 0 1 0	V+ → HiZ			

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x5B	0 1 0 1	1 0 1 1	V+ → HiZ			
0x5C	0 1 0 1	1 1 0 0	V+ → HiZ			
0x5D	0 1 0 1	1 1 0 1	V+ → HiZ			
0x5E	0 1 0 1	1 1 1 0	V+ → HiZ			
0x5F	0 1 0 1	1 1 1 1	V+ → HiZ			

Table 38: CMD code for 0x50-0x5F, MUX-S2 CTRL

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x60-0x6F	0 1 1 0		MUX S4 CTRL ($I_{REFSQUIB}$)			
0x60	0 1 1 0	0 0 0 0	Disable I_{REF}	•	•	•
0x61	0 1 1 0	0 0 0 1	I_{REF} → T1U & Polarization at T1U disabled [1)]			
0x62	0 1 1 0	0 0 1 0	I_{REF} → T2U & Polarization at T2U disabled [1)]			
0x63	0 1 1 0	0 0 1 1	I_{REF} → T3U & Polarization at T3U disabled [1)]			
0x64	0 1 1 0	0 1 0 0	I_{REF} → T4U & Polarization at T4U disabled [1)]			
0x65	0 1 1 0	0 1 0 1	I_{REF} → T5U & Polarization at T5U disabled [1)]			
0x66	0 1 1 0	0 1 1 0	I_{REF} → T6U & Polarization at T6U disabled [1)]			
0x67	0 1 1 0	0 1 1 1	I_{REF} → T7U & Polarization at T7U disabled [1)]			
0x68	0 1 1 0	1 0 0 0	I_{REF} → T8U & Polarization at T8U disabled [1)]			
0x69	0 1 1 0	1 0 0 1	I_{REF} → RREF			
0x6A	0 1 1 0	1 0 1 0	Disable I_{REF}			
0x6B	0 1 1 0	1 0 1 1	Disable I_{REF}			
0x6C	0 1 1 0	1 1 0 0	Disable I_{REF}			
0x6D	0 1 1 0	1 1 0 1	Disable I_{REF}			
0x6E	0 1 1 0	1 1 1 0	Disable I_{REF}			
0x6F	0 1 1 0	1 1 1 1	Disable I_{REF}			

Table 39: CMD code for 0x60-0x6F, MUX-S4 CTRL

[1)] deactivation of the polarization unit necessary to eliminate the additional pull-up current from the buffer.

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x70-0x7F	0 1 1 1		CODELOCK/ current mode programming (LCM/HCM)			
0x70	0 1 1 1	0 0 0 0	Lock CMD	●	●	
0x71	0 1 1 1	0 0 0 1	UNLOCK CMD			
0x72	0 1 1 1	0 0 1 0	NOP			
0x73	0 1 1 1	0 0 1 1	NOP			
0x74	0 1 1 1	0 1 0 0	NOP			
0x75	0 1 1 1	0 1 0 1	NOP			
0x76	0 1 1 1	0 1 1 0	SET LCM (only possible during locked state)	●		
0x77	0 1 1 1	0 1 1 1	NOP			
0x78	0 1 1 1	1 0 0 0	NOP			
0x79	0 1 1 1	1 0 0 1	NOP			
0x7A	0 1 1 1	1 0 1 0	NOP			
0x7B	0 1 1 1	1 0 1 1	NOP			
0x7C	0 1 1 1	1 1 0 0	SET HCM (only possible during locked state)			
0x7D	0 1 1 1	1 1 0 1	NOP			
0x7E	0 1 1 1	1 1 1 0	NOP			
0x7F	0 1 1 1	1 1 1 1	NOP			

Table 40: CMD code for 0x70-0x7F; Codelock and CM programming

•

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0x80-0x8F	1 0 0 0		LSD activation/deactivation T1L-T4L			
0x80-0x8F	1 0 0 0	- - - 0	deactivate T1L	●	●	●
0x80-0x8F	1 0 0 0	- - - 1	activate T1L			
0x80-0x8F	1 0 0 0	- - 0 -	deactivate T2L	●	●	●
0x80-0x8F	1 0 0 0	- - 1 -	activate T2L			
0x80-0x8F	1 0 0 0	- 0 - -	deactivate T3L	●	●	●
0x80-0x8F	1 0 0 0	- 1 - -	activate T3L			
0x80-0x8F	1 0 0 0	0 - - -	deactivate T4L	●	●	●
0x80-0x8F	1 0 0 0	1 - - -	activate T4L			
0x90-0x9F	1 0 0 1		LSD activation/deactivation T5L-T8L			
0x90-0x9F	1 0 0 1	- - - 0	deactivate T5L	●	●	●
0x90-0x9F	1 0 0 1	- - - 1	activate T5L			
0x90-0x9F	1 0 0 1	- - 0 -	deactivate T6L	●	●	●
0x90-0x9F	1 0 0 1	- - 1 -	activate T6L			
0x90-0x9F	1 0 0 1	- 0 - -	deactivate T7L	●	●	●
0x90-0x9F	1 0 0 1	- 1 - -	activate T7L			
0x90-0x9F	1 0 0 1	0 - - -	deactivate T8L	●	●	●
0x90-0x9F	1 0 0 1	1 - - -	activate T8L			

Table 41: CMD code for 0x80-0x9F, TxL activation/ deactivation

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0xA0-0xAF	1 0 1 0		MUX S3 CTRL (V-)			
0xA0	1 0 1 0	0 0 0 0	V- → GND	•	•	•
0xA1	1 0 1 0	0 0 0 1	V- → T1L			
0xA2	1 0 1 0	0 0 1 0	V- → T2L			
0xA3	1 0 1 0	0 0 1 1	V- → T3L			
0xA4	1 0 1 0	0 1 0 0	V- → T4L			
0xA5	1 0 1 0	0 1 0 1	V- → T5L			
0xA6	1 0 1 0	0 1 1 0	V- → T6L			
0xA7	1 0 1 0	0 1 1 1	V- → T7L			
0xA8	1 0 1 0	1 0 0 0	V- → T8L			
0xA9	1 0 1 0	1 0 0 1	V- → HiZ			
0xAA	1 0 1 0	1 0 1 0	V- → HiZ			
0xAB	1 0 1 0	1 0 1 1	V- → HiZ			
0xAC	1 0 1 0	1 1 0 0	V- → HiZ			
0xAD	1 0 1 0	1 1 0 1	V- → HiZ			
0xAE	1 0 1 0	1 1 1 0	V- → HiZ			
0xAF	1 0 1 0	1 1 1 1	V- → HiZ			

Table 42: CMD code for 0xA0-0xAF, MUX-S3 CTRL

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0xB0-0xBF	1 0 1 1		NOP			
0xC0-0xCF	1 1 0 0		NOP			
0xD0-0xDF	1 1 0 1		NOP			

Table 43: CMD code for 0xB0-0xDF, CMD's not used

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0xE0-0xEF	1 1 1 0		DRV Test/ FTL-Test			
0xE0	1 1 1 0	0 0 0 0	TEST OFF	•	•	•
0xE1	1 1 1 0	0 0 0 1	TEST OFF			
0xE2	1 1 1 0	0 0 1 0	TEST OFF			
0xE3	1 1 1 0	0 0 1 1	TEST_UP			
0xE4	1 1 1 0	0 1 0 0	TEST OFF			
0xE5	1 1 1 0	0 1 0 1	FTL_activation (only possible during locked state) 1.)			
0xE6	1 1 1 0	0 1 1 0	TEST OFF			
0xE7	1 1 1 0	0 1 1 1	FTL_RESET (only possible during locked state) 1.)	•	•	•
0xE8	1 1 1 0	1 0 0 0	TEST OFF			
0xE9	1 1 1 0	1 0 0 1	TEST OFF			
0xEA	1 1 1 0	1 0 1 0	TEST OFF			
0xEB	1 1 1 0	1 0 1 1	TEST OFF			
0xEC	1 1 1 0	1 1 0 0	TEST_LOW			
0xED	1 1 1 0	1 1 0 1	TEST OFF			
0xEE	1 1 1 0	1 1 1 0	TEST OFF			
0xEF	1 1 1 0	1 1 1 1	TEST OFF			

Table 44: CMD code for 0xE-0xEF, TEST DRV/ FTL-Test activation/deactivation

1) This means a 0xE5 or 0XE7 CMD's will be rejected, while the device is in state “UNLOCKED”. Necessary to avoid reset of FTL during a firing sequence. Otherwise SOA violation of the driver possible.

Code[HEX]	Address	Data	Description	POR	SPI-Reset	Unlock Out↑↓
0xF0-0xFE	1 1 1 1		ELMOS Test Mode			
0xFF	1 1 1 1	1 1 1 1	Not used			

Table 45: CMD code for 0xF-0xFF

5.15 Trimming

The calibration of the IC is performed with the ELMOS standard FUSE-Array cell by the ELMOS ATE (**A**utomatically **T**est **E**quipment) during Final part production test.

5.15.1 Parameter Table

The calibrated parameters and the default values are listed in Table 46 below.

#Bits	Description	Symbol	Trimming Bits	Default values [1)]
3	Current limitation of HSD in HCM	HSD_{ILIM} HCM [2)]	[0,1,2], [2]=MSB	[0,0,0]
3	Current limitation of HSD in LCM	HSD_{ILIM} LCM [2)]	[3,4,5], [5]=MSB	[0,0,0]
3	Current limitation of HSD in TM	HSD_{ILIM} TM [2)]	[6,7,8], [8]=MSB	[0,0,0]
3	Current limitation of LSD in Normal Mode	LSD_{ILIM} NM [2)]	[9,10,11], [11]=MSB	[0,0,0]
3	Current limitation of LSD in Test Mode	LSD_{ILIM} TM [2)]	[12,13,14], [14]=MSB	[0,0,0]
4	Adjustment of internal 8 MHz OSC	OSC8MEG_FREQ [2)]	[15,16,17,18], [18]=MSB	[0,0,0,1]
4	Adjustment of internal reference current source	IREF_BIAS [2)]	[19,20,21,22], [22]=MSB	[0,0,0,1]
1	Odd Parity of Bit [0..23]	PAR	[23]	[0]

Table 46: Trimming Bits

1.) Defaults values are valid during a global power on reset phase (see chapter 5.3), during the read out process of the FUSE Array or if the read out has finished with an error. The default value of the parity bit (bit[23]) is set to low level to obtain a FUSE_FAIL status (see chapter 5.4.5), if the read out has finished with an error.

2.) If the Fuse Array read out fails, the spec parameters of the High side and Low side driver currents in HCM, LCM and Test mode, the oscillator frequency and the 40mA reference current source can be violated in both directions.

5.15.2 Trimming read out time duration

$V_{A,}$> 3.85V or V5>4.5V

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	OTP cell ready; Trimming read out successfully finished after power up or external RESET	1st read out successfully, OTP_CLK running with not calibrated F_{OSC_NC} base timing. (see chapter 5.13)	$T_{TRM\_READY\_1}$	70	100	150us	µs
2	OTP cell ready; Trimming read out finished after power up or external RESET	1st read out not successfully. Read out is repeated 16 times. OTP_CLK running with not calibrated F_{OSC_NC} base timing. (see chapter 5.13)	$T_{TRM\_READY\_16}$			2400	µs

Table 47: Fuse array read out time duration. If time is not exceeded the FUSE fail bit is set.

5.16 Terminal TEST

The TEST pin is used for entering ELMOS test modes only. In application the pin has to be connected to GND.

5.16.1 TEST, DC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Input Low voltage	4.5V<V_5<5.5V	$V_{Di,L}$ TEST	0,8	-	-	V
2	Input High voltage	4.5V<V_5<5.5V	$V_{Di,L}$ TEST	-	-	2	V
3	Internal pull down resistor	4.5V<V_5<5.5V;	R_{PD} TEST	30	50	70	kΩ

Table 48: Terminal TEST, DC

6 Qualification

6.1 Qualification Reference

Qualification is done according to AECQ100.

7 Package

7.1 Marking

7.1.1 Top side

E981.18A
XXX#IYWW*@

in which

E / M / T	Series product / Prototype / Test circuit
918.18	ELMOS ASSP project number
A	Design version
XXX	Lot number
#	Assembly code
I (optional)	Wafer fabrication site
YWW	Year and work week of assembly
*	Mask revisions status
@	Only for internal use

8 Storage, handling, packing and shipping

8.1 Storage

Storage conditions should not exceed those given in chapter 4.1 (Absolute maximum ratings).

8.2 Handling

Devices are sensitive to damage by electrostatic discharge (ESD) and should only be handled at an ESD protected workstation.

8.3 Packing

Material shall be packed for shipment as follows:
- Tape on reel
- Moisture sensitivity: level 3

WARNING – Life Support Applications Policy

ELMOS Semiconductor AG is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing ELMOS Semiconductor AG products, to observe standards of safety, and to avoid situations in which malfunction or failure of an ELMOS Semiconductor AG Product could cause loss of human life, body injury or damage to property. In development your designs, please ensure that ELMOS Semiconductor AG products are used within specified operating ranges as set forth in the most recent product specifications.

General Disclaimer

Information furnished by ELMOS Semiconductor AG is believed to be accurate and reliable. However, no responsibility is assumed by ELMOS Semiconductor AG for its use, nor for any infringements of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of ELMOS Semiconductor AG. ELMOS Semiconductor AG reserves the right to make changes to this document or the products contained therein without prior notice, to improve performance, reliability, or manufacturability .

Application Disclaimer

Circuit diagrams may contain components not manufactured by ELMOS Semiconductor AG, which are included as means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information in the application examples has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of ELMOS Semiconductor AG or others.

Contact Information

Headquarters
ELMOS Semiconductor AG
Heinrich-Hertz-Str. 1 • D-44227 Dortmund (Germany) ✆ +492317549100 ✉: sales@elmos.de
🌍: www.elmos.de

Regional Sales and Application Support Office Munich
ELMOS Semiconductor AG
Am Geflügelhof 12 • 85716 Unterschleißheim/Eching ✆ +49893183700

Sales Office France
ELMOS FRANCE SAS
9/11 allée de l'Arche • La Défense • 92671 Courbevoie cedex (France) ✆ +33149971591

Sales and Application Support Office North America
ELMOS NA. Inc.
32255 Northwestern Highway, Suite 45 • Farmington Hills, MI 48334 ✆ +12488653200

Sales and Application Support Office Korea and Japan
ELMOS Korea
Dongbu Root building, 16-2, Suite 509, • Sunae-dong, Bundang-gu,
Seongnam-shi, Kyonggi-do (Korea) ✆ +82317141131

Sales and Application Support Office China
ELMOS Semiconductor Technology (Shanghai) Co., Ltd.
57-01E, Lampl Business Centre, 57F, The Exchange • 1486 Nanjing W Rd.
(299 Tongren Rd) • JingAn Shanghai • P.R.China 200040 ✆ +862161717358

Sales and Application Support Office Singapore
ELMOS Semiconductor Singapore Pte Ltd.
60 Alexandra Terrace • #09-31 The Comtech • Singapore 118502 ✆ +6566351141