

## Six-Channel LED Driver with Integrated Fault Protection

### Features

- ▶ Drives six strings of LEDs, up to 30mA each
- ▶ Phased PWM dimming
- ▶ Pin-programmable dimming frequency or synchronizable to an external signal
- ▶ PWM dimming to very low duty cycles
- ▶ ±1.5% typical current and 0.5% duty cycle matching
- ▶ Optional crystal oscillator for precision dimming frequency
- ▶ Outputs rated to 56V
- ▶ Robust protection against under voltage, over voltage, open/shorted strings, over current, and over temperature. Good strings remain lit.
- ▶ Programmable boost converter frequency
- ▶ 10µA maximum input current in shutdown state
- ▶ Resistor-programmable full-scale LED current
- ▶ 24-Lead 4×4 QFN package

### Applications

- ▶ Multi-string solid-state lighting applications
- ▶ Portable LED backlighting applications

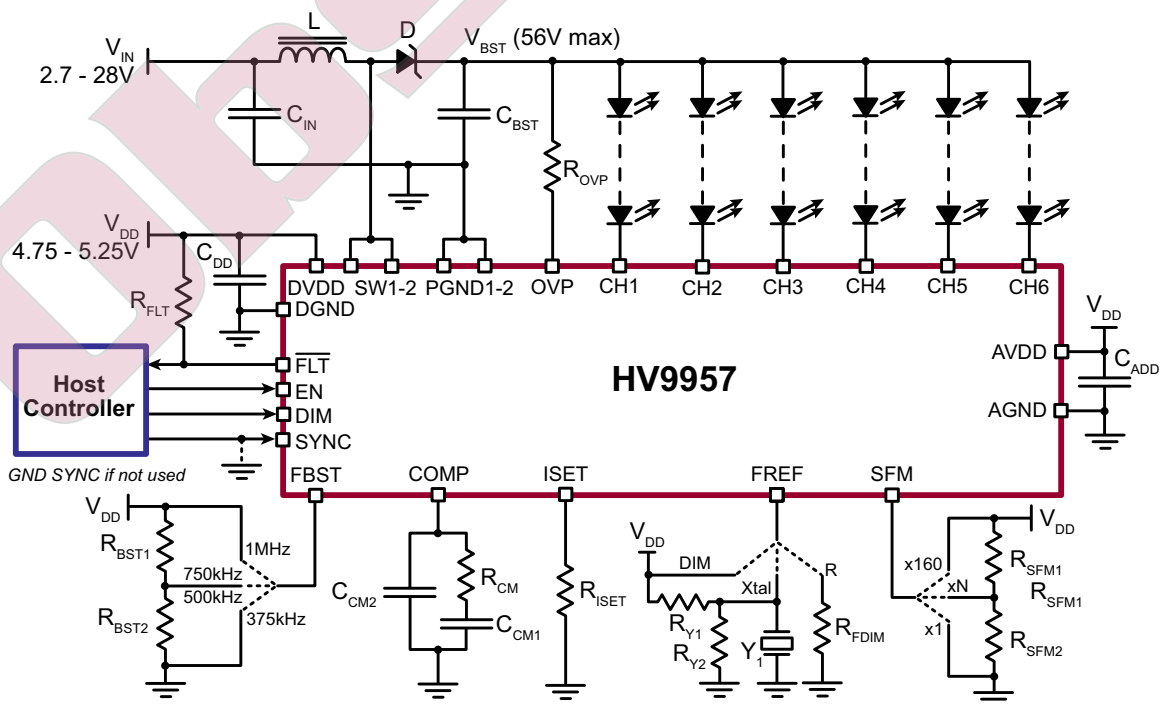
### General Description

The HV9957 LED driver combines a switch-mode boost converter and six low-dropout linear current regulators to provide the advantages of high efficiency with precise current control. It may be configured for many applications, and is especially suited for one to three cell lithium-ion powered devices. An internal boost controller with an integrated switch eliminates the need for an external MOSFET.

Phased PWM dimming eliminates audible noise, reduces transient load on the boost converter, and minimizes supply current ripple. PWM dimming may be synchronized to an external signal such as the display refresh rate or, internally generated by a resistor or crystal oscillator.

Fault protection is provided against open/shorted LEDs, over voltage, under voltage, over current, and over temperature conditions. When a string fails, either shorted or open, the affected channel is removed from feedback and the rest continue operating normally.

### Typical Application Circuit



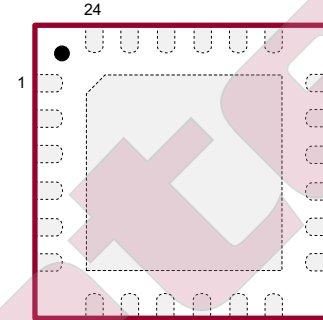
## Ordering Information

Device	<b>24-Lead QFN</b> 4.00x4.00mm body 0.80mm height (max) 0.50mm pitch
HV9957	HV9957K7-G

-G indicates package is RoHS compliant ("Green")



## Pin Configuration



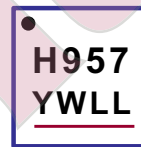
**24-Lead QFN (K7)**  
(top view)

## Absolute Maximum Ratings

Parameter	Value
$V_{DD}$ , $DV_{DD}$	-0.3 to 6.5V
CH1-6, SW1-2	60V
FREF, DIM, SFM SYNC, EN, FBSx, OVP, $\overline{FLT}$	-0.3V to ( $V_{DD} + 0.3V$ )
$I_{FLT}$	10mA
$V_{ISET}$	-0.3V to $V_{DD}$
Storage temperature	-65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Product Marking



Y = Last Digit of Year Sealed  
 W = Code for Week Sealed  
 L = Lot Number  
 — = "Green" Packaging

Package may or may not include the following marks: Si or

**24-Lead QFN (K7)**

## Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions	
$V_{DD}$	IC supply voltage	4.75	5.00	5.50	V	---	
$C_{DD}$	$V_{DD}$ capacitor	$DV_{DD}$	4.7	-	-	$\mu F$	One ceramic or an aluminum/tantalum +100nF ceramic
		$AV_{DD}$	4.7	-	-		
$V_{BST}$	Boost converter output voltage	-	-	56	V	$V_{IN} \geq 12V$	
$T_J$	Operating junction temperature*	-40	-	125	°C	---	
$I_{CH}$	LED current	-	-	30	mA	---	
$f_{DIM}$	PWM dimming frequency (all operating modes)	3.5	-	24	kHz	---	
$R_{OSC}$	Precision oscillator resistor	125	-	250	k $\Omega$	---	
$f_{XTAL}$	Crystal frequency	-	24.576	-	MHz	---	
$f_{SYNC}$	SYNC frequency	60	-	480	Hz	---	
$I_{SW}$	Boost converter switch current	-	-	2.2	A	---	
$C_{COMP}$	Loop compensation network	Type 2			-	---	
BCOM	Boost converter operating mode	CCM or DCM			-	---	

Note:

\* Junction temperature internally linked.

**Electrical Characteristics** (over recommended operating conditions at 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
<b>Supply</b>						
$I_{DD}$	$V_{DD}$ active current ( $AV_{DD} + DV_{DD}$ )	-	7.0	10	mA	$f_{BST} = 1.0\text{MHz}$
$I_{DDQ}$	$V_{DD}$ standby current ( $AV_{DD} + DV_{DD}$ )	-	1.0	10	$\mu\text{A}$	EN = 0
$I_{LKG}$	OFF state leakage current, sum of SW1 - 2, OVP, and CH1 - 6 pins	-	-	10	$\mu\text{A}$	EN pin = 0, 12V applied to SWx and CHx, 5.0V applied to VDD pins
<b>Boost Converter</b>						
$f_{BST}$	Switching frequency	338	375	412	kHz	FBST = 0 - $0.05 \times V_{DD}$
		450	500	550	kHz	FBST = $0.28 - 0.38 \times V_{DD}$
		675	750	825	kHz	FBST = $0.62 - 0.72 \times V_{DD}$
		0.90	1.00	1.10	MHz	FBST = $0.95 - 1.00 \times V_{DD}$
$R_{SW}$	Switch ON-resistance	-	120	150	m $\Omega$	$I_{SW} = 1.0\text{A}$
$I_{SAT}$	Switch saturation current	3.0	-	-	A	$V_{SW} > 350\text{mV}$
$t_{RISE}$	Switch current rise time	-	-	5.0	ns	$I_{SW} = 1.0\text{A}$ , 10% - 90%
$t_{FALL}$	Switch current fall time	-	-	5.0	ns	$I_{SW} = 1.0\text{A}$ , 90% - 10%
$t_{BLNK}$	Blanking interval	-	7.0	-	ns	---
$t_{SS}$	Soft start interval	-	6.4	-	ms	---
<b>LED Drivers (CH1-CH6)</b>						
$V_{ISET}$	Voltage at ISET pin	-	700	-	mV	---
$I_{CH}$	Full scale output current (average of all channels)	19.6 - 29.4	20.0 - 30.0	20.4 20.4 30.6	mA	$R_{ISET} = 20.0\text{k}\Omega$ , $V_{CH} = 900\text{mV}$ $R_{ISET} = 20.0\text{k}\Omega$ , $V_{CH} = 0 - 900\text{mV}$ $R_{SET} = 13.3\text{k}\Omega$ , $V_{CH} = 900\text{mV}$
$I_{CH(OFF)}$	Output current when disabled	-	-	10	$\mu\text{A}$	EN = 0
$\Delta I_{CH}$	Current matching (deviation from average of all 6 channels) See Output Characteristics graph	-1.5	-	+1.5	%	$I_{OUT} = 20\text{mA}$ , $D_{DIM} = 100\%$ $V_{CH} = 0.7 - 2.0\text{V}$
		-1.5	-	+1.5→2.0	%	$V_{CH} = 2.0 - 10\text{V}$
$V_{DO}$	Regulated dropout voltage headroom (lowest active channel)	700	900	1100	mV	$I_{OUT} = 30\text{mA}$
<b>PWM LED Drive (CH1 - CH6)</b>						
$D_{DIM}$	Duty cycle absolute accuracy Average of all 6 channels	-	-	0	%	$D_{IN} = 0\%$ , $f_{DIM} = 8\text{kHz}$
		1.90	2.00	2.10		$D_{IN} = 2\%$ , $f_{DIM} = 8\text{kHz}$
		48.5	50.0	51.5		$D_{IN} = 50\%$ , $f_{DIM} = 8\text{kHz}$
		100	-	-		$D_{IN} = 100\%$ , $f_{DIM} = 8\text{kHz}$
$\Delta t_{PW}$	Pulse width matching Deviation from avg of all 6 chs Refer to Output Pulse graph	-0.5	-	+0.5	%	$D_{IN} = 2 - 100\%$ , $f_{DIM} = 8\text{kHz}$ , measured at 50% full-scale
$t_{SYNC(MIN)}$	Minimum sync pulse width	300	-	-	ns	---
$f_{INT}$	Internally generated dimming frequency	9.552 -10ppm	9.600 9.600	9.648 +10ppm	kHz	$R_{FDIM} = 200\text{k}\Omega$ , $SFM = V_{DD}$ , no xtal, $SFM = V_{DD}$ , 24.576MHz xtal

## Electrical Characteristics (over recommended operating conditions at 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
$f_{\text{SYNC(MIN)}}$	Minimum SYNC frequency	-	48	55	Hz	---
$f_{\text{SYNC(MAX)}}$	Maximum SYNC frequency	540	600	-	Hz	---
$t_{\text{RISE}}$	Output current rise time	-	35	-	ns	$I_{\text{CH}} = 20\text{mA}$ , 10 - 90%
$t_{\text{FALL}}$	Output current fall time	-	160	-	ns	$I_{\text{CH}} = 20\text{mA}$ , 90 - 10%

### Protection Circuits

UVLO	$V_{\text{DD}}$ UVLO trip point, OFF	4.00	4.20	4.40	V	---
UVLO <sub>HYS</sub>	$V_{\text{DD}}$ UVLO hysteresis	-	300	-	mV	---
$V_{\text{OCP}}$	Switch over current protection	-	350	-	mV	SW ON
$t_{\text{OCP}}$	$I_{\text{OCP}}$ switch shut-OFF response time	-	-	50	ns	$I_{\text{SW}} < 200\text{mA}$
$I_{\text{OVP}}$	OVP bias current	1.12	1.14	1.16	$\times I_{\text{SET}}$	$V_{\text{OVP}} < 1.7\text{V}$
$I_{\text{OVPH}}$	OVP hysteresis current	-6%	-5%	-4%	$\times I_{\text{OVP}}$	$V_{\text{OVP}} > 2.3\text{V}$
$V_{\text{OVP}}$	OVP threshold voltage	1.7	2.0	2.3	V	---
$V_{\text{ACH}}$	ACH threshold voltage	1.15	1.25	1.35	V	---
$T_{\text{ACT1}}$	Over temperature protection activation temperature, stage 1	125	135	145	°C	Rising
$T_{\text{RST1}}$	Over temperature protection reset temperature, stage 1	-	-20	-	°C	Falling
$T_{\text{ACT2}}$	Over temperature protection activation temperature, stage 2	10	15	20	°C + $T_{\text{ACT2}}$	Rising
$T_{\text{RST2}}$	Over temperature protection reset temperature, stage 2	-	-30	-	°C + $T_{\text{ACT2}}$	Falling
$T_{\text{OTP}}$	Over temperature protection re-activation interval	-	800	-	ms	---
EN <sub>FLT</sub>	Enable low pulse width to reset fault	0.1	-	10	µs	---
EN <sub>OFF</sub>	Enable low pulse width to disable	50	-	-	µs	---

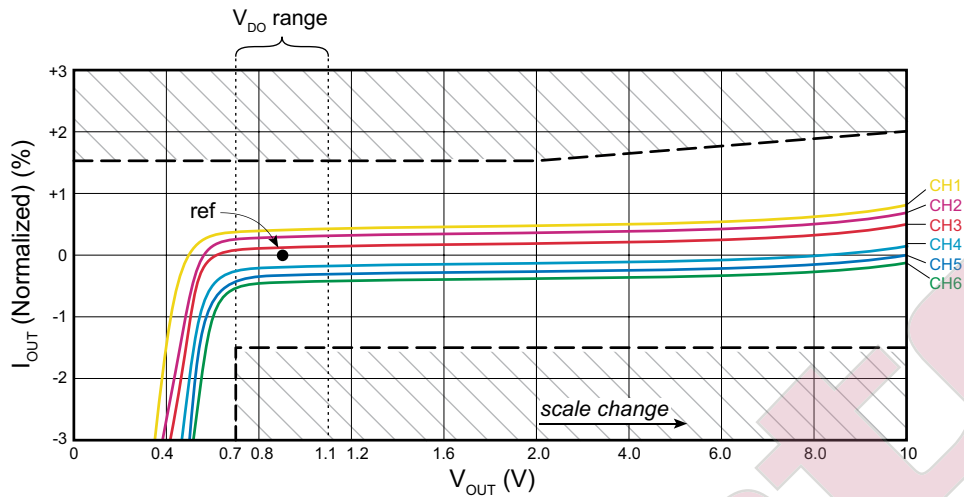
### Control Inputs/Outputs (SYNC, DIM, $\overline{\text{FLT}}$ , SFM, FREF, FBST, EN)

$I_{\text{SFM}}$	SFM input current	-5.0	-	+5.0	µA	$V_{\text{SFM}} = 0 - 5.0\text{V}$
$V_{\text{IL}}$	Logic low input voltage	-	-	0.8	V	---
$V_{\text{IH}}$	Logic high input voltage	2.1	-	-	V	---
$V_{\text{OL}}$	Logic low output voltage	-	-	0.4	V	$I_{\text{LOAD}} = 4.0\text{mA}$
$I_{\text{L}}$	Logic low input current	-	-	5.0	µA	$V_{\text{IN}} = \text{grounded, open, or } 4.75 - 5.25\text{V}$
$I_{\text{H}}$	Logic high input current	-	-	5.0	µA	

### Thermal (Guaranteed by design - not production tested.)

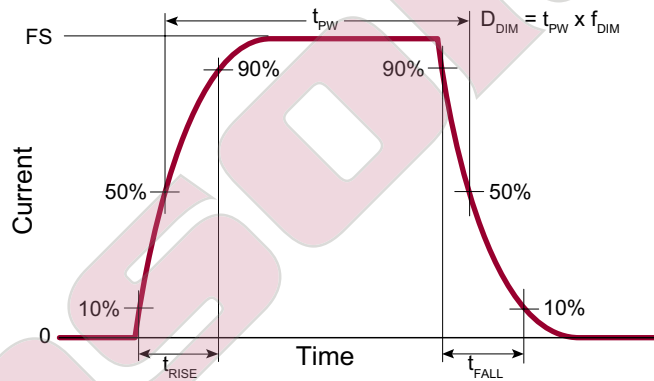
$\theta_{j-a}$	Thermal resistance, junction to ambient	-	34	-	°C/W	Soldered to PCB with 5.0cm <sup>2</sup> exposed copper area using 5 thermal vias
$\theta_{j-p}$	Thermal resistance, junction to underside plate	-	3.6	-	°C/W	---

**Output Characteristics** ( $I_{CH} = 20mA$  nominal)



Example curves shown for illustrative purposes only.  
 Normalization reference is the average current of all 6 channels at 900mV.  
 Limits apply to each channel individually.

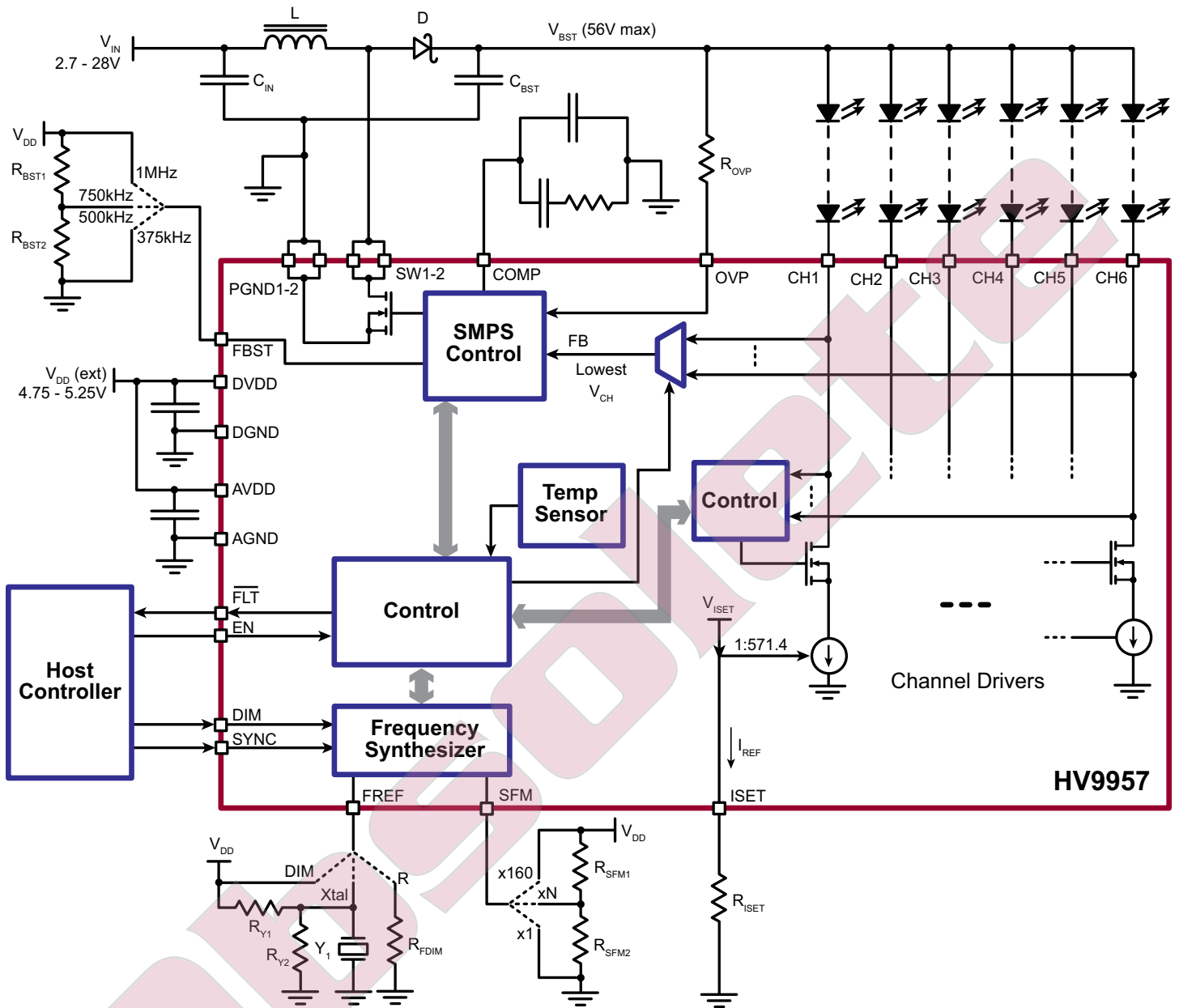
**Output Pulse** (PWM Dimming)



**Abbreviations:**

OVP	Over-Voltage Protection	PWM	Pulse Width Modulation	CCM	Continuous Conduction Mode
OCP	Over-Current Protection	FLT	Fault bit or pin	DCM	Discontinuous Conduction Mode
OLP	Open LED Protection	PHD	Phased Dimming		
SLP	Shorted LED Protection	SFM	Sync Frequency Multiplier	VBST	Boost converter output voltage
OTP	Over-Temperature Protection	RSA	Redistribute start angles (phased dimming)		

Simplified Internal Block Diagram



## Application Information

### Operation

The HV9957 combines a switch-mode boost converter and six low-dropout linear current regulators to provide the advantages of high efficiency and precise current control.

### Supplies

Two independent supplies may be used to power the back-light controller circuit: one to supply the HV9957 ( $V_{DD}$ ) and another to supply the boost converter ( $V_{IN}$ ). The supply for the boost converter may range from 2.7 to 28V depending on the load. The HV9957 supply ( $V_{DD}$ ) is 5.0V nominal.

The boost converter need not be supplied from the same source as for the HV9957. The low ON-resistance internal boost converter switch combined with CCM operation allows boost converter supply voltages as low as 2.7V for single-cell lithium-ion batteries. At lower boost supply voltages, output power decreases due to the increased switch current.

The HV9957 has two power states - shutdown and active. To keep standby currents low, internal circuits are powered down when shut down.

The active state is when the HV9957 is driving the LED strings. When transitioning from shutdown to active, a soft-start circuit ramps input current over a 6.4ms interval.

### HV9957 States

EN pin	State
0 for >50 $\mu$ s	Shutdown
0 $\rightarrow$ 1	Soft-start
1	Active
1-0-1 for <10 $\mu$ s	Reset fault

### Under-voltage Lock Out (UVLO)

The boost converter and output drivers will not be enabled until  $V_{DD}$  reaches its UVLO thresholds. When  $V_{DD}$  falls by the UVLO hysteresis voltage from the turn-ON threshold, the boost converter and output drivers are disabled.

### Boost Converter

The boost converter provides the high voltage needed to drive the LED strings. It gets its feedback from the active output channels, maintaining a minimum voltage of 900mV across the linear current regulators (CH1 - 6). Therefore, the boost converters' output voltage ( $V_{BST}$ ) will be 900mV ( $V_{DO}$ )

plus the maximum LED string voltage drop ( $V_{STR(MAX)}$ ).

$$V_{BST} = V_{DO} + V_{STR(MAX)}$$

It is recommended that the boost ratio ( $V_{BST} / V_{OUT}$ ) be limited to 9 or less.

Due to boost switch limitations, load capability decreases with lower supply voltages. As with any switching converter, input power is relatively constant for a given load. Since  $P_{IN} = V_{IN} \cdot I_{IN}$ , input current increases as input voltage decreases. The following graph depicts the load capability for various supply voltages and LEDs/string.

### Load Capability

Batt Cells	LED / str	$V_{OUT}$ (V)	$V_{IN}$ (V)	Max $P_{LOAD}$ (W)	Max $I_{LED}$ (mA)	Avg $I_{IN}$ (A)
1	7	22.4	2.7	3.4	25	1.4
			3.8	4.0	30	1.0
			4.2	4.0	30	1.1
2	12	38.4	5.4	6.9	30	1.4
			7.6	6.9	30	1.0
			8.4	6.9	30	0.9
3	17	54.4	8.1	9.8	30	1.3
			11.4	9.8	30	1.0
			12.6	9.8	30	0.9

Based on mathematical modeling and assumed characteristics of external components. The actual circuit may yield different results.

$I_{IN}$  is based on assumed 90% efficiency and CCM. Ripple should be factored in, depending on the inductor value and boost frequency

$V_{OUT}$  is based on 3.2V LEDs.

The boost converter frequency is pin-programmable in four steps by applying the appropriate voltage to the FBST pin.

FBST	Internal Osc	XTAL Osc
0V	375kHz	$\pm$ 64
1/3 $V_{DD}$	500kHz	$\pm$ 48
2/3 $V_{DD}$	500kHz	$\pm$ 32
$V_{DD}$	1.0MHz	$\pm$ 24



Slope compensation is employed internally, therefore continuous conduction mode (CCM) can be used.

An RC network on the COMP pin establishes boost converter loop stability.

## Over Current Protection (OCP)

The boost converter internal switch is protected against over current. Switch voltage is monitored when the switch is ON, and if it reaches the  $V_{OCP}$  threshold, the OCP circuit immediately turns OFF the switch. OCP occurs on a cycle-by-cycle basis, resetting every boost converter cycle.

When OCP is active, peak current is limited and the boost converter may not support the load. The LEDs will dim, often unequally since the strings have different voltage drops. Some strings may extinguish entirely.

OCP latches the  $\overline{FLT}$  pin. It is reset by toggling EN.

## Soft Start

Inrush current limiting during boost converter turn-ON is provided by a soft-start circuit which gradually ramps-up the boost converter duty cycle over a 6.4ms interval.

## Output Channels (CH1–6)

Each channel has a linear current regulator which maintains a constant current thru the connected LED string. Full-scale current is established by the value of the external  $R_{SET}$  resistor. In addition, the linear regulators may be turned ON and OFF under PWM control to provide a duty cycle average dimming control.

Efficiency is maximized by maintaining a low voltage across the outputs. The channel with the highest LED string voltage drop, and thus the lowest channel voltage, becomes the feedback point for regulating the boost converter output voltage. Once a channel has been identified as faulty due to OLP or SLP, it will not be used as a feedback point for boost converter regulation.

## Full-scale LED Current (ISET)

Output current ( $I_{CH}$ ) is set by the value of the resistor connected to the ISET pin ( $R_{ISET}$ ).

$$I_{CH} = \frac{400V}{R_{ISET}}$$

## Enable

The EN pin serves two functions: it enables and disables the HV9957, or resets fault circuitry. When held high for at

least 50ns the HV9957 is enabled. When toggled low for 10 $\mu$ s, the fault circuits are reset, except for OTP, which is self-resetting.

When held low for more than 50 $\mu$ s, the HV9957 is disabled. To achieve very low standby current consumption, enable controls the power provided to internal circuits. For this reason, there is a delay after EN = 1 until the driver reaches full operation.

## PWM Dimming

In PWM dimming, an external PWM signal applied to the DIM input controls the ON/OFF duty cycle of the outputs (CH1 - 6). A logic 1 enables the outputs, while a logic 0 disables the outputs. The LED drive frequency need not be the frequency of the signal applied to the DIM input. See the section on LED drive frequency on Page 14.

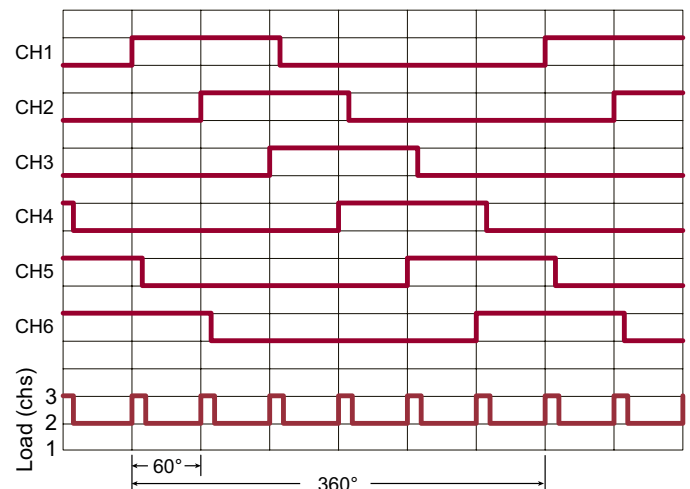
In PWM dimming, the average LED current is the duty cycle average of the full-scale current.

$$I_{CH} = I_{FS} \cdot D_{PWM}$$

where:  $I_{CH}$  = average output current  
 $I_{FS}$  = full scale current  
 $D_{PWM}$  = duty cycle

## Phased PWM Dimming

With conventional PWM dimming, all the channels turn ON and OFF at the same time. Phased PWM dimming offsets the beginning of the ON time for each channel, distributing the start angles equally across 360°.



Phased dimming reduces the transient load on the boost converter, minimizing supply current ripple. This in turn, reduces conducted EMI on the supply rail and minimizes possible interference to adjacent circuitry. It also effectively sex-



tuples the PWM dimming frequency, allowing a low PWM dimming frequency for dynamic range, while extending the audible effects beyond the range of human hearing.

With non-phased dimming, the dynamic load would have an amplitude of 6 channels and a frequency equal to the PWM dimming frequency. With phased PWM dimming, the transient load will be one channel amplitude at most, and at a frequency six times the dimming frequency.

When one or more channels is disabled by a fault condition, the phase angles of the remaining good strings are redistributed equally across 360°. For example, with all six channels active, the start phase angles are integer multiples of 360° ÷ 6 = 60°. If one string fails, the remaining five strings have start phase angles that are integer multiples of 360° ÷ 5 = 72°.

Phased dimming is active whether sync is used or not.

## Protection Circuits

Robust protection is provided for various fault conditions, including boost switch over current, supply under voltage, output over voltage, temperature, shorted LED strings, and open or partially open LED strings. When OTP1 is activated, the HV9957 first attempts to alleviate the fault condition by disabling the shorted or open string. The string identified as open and/or shorted is disconnected while keeping the other strings lit.

If the fault condition persists and results in excessive die temperature, all the channels and the boost converter are disabled until die temperature falls below the reset threshold, at which point the driver is re-enabled. If the fault condition persists, the cycle is repeated.

## Over Voltage Protection (OVP)

Over voltage protection prevents VBST from rising to destructive levels in the event that any LED strings become opened. VBST is sensed by converting the voltage to current via  $R_{OVP}$ . The OVP pin is biased at a constant voltage.

$$\begin{aligned} V_{OVP} &= R_{OVP} \cdot 8/7 \cdot I_{SET} + 2V && \text{rising} \\ &= 0.95 \cdot R_{OVP} \cdot 8/7 \cdot I_{SET} + 2V && \text{falling} \end{aligned}$$

where  $V_{OVP}$  is the OVP threshold voltage.

OVP is usually activated by an open or a partially open (Zener-protected) LED string as the boost converter seeks to regulate the voltage at output with the open LED.

The OVP pin goes into a high resistance state during shut-down to minimize supply current.

## Shorted LED Protection (SLP) Temperature Triggered

Protection against shorted LED strings is provided. Any string identified as shorted is removed from the boost converter feedback loop and disconnected. The remaining good strings continue to operate normally.

The  $\overline{\text{FLT}}$  pin is asserted low. The fault circuit is reset by toggling EN or cycling power.

## Open LED Protection (OLP)

With an open LED string,  $V_{BST}$  rises as it attempts to achieve 900mV at the channel with the open string. Eventually OVP or SLP activates, at which time those outputs having zero volts are marked as open and are removed from boost converter feedback. The current regulators on the open strings continue to operate and will regulate LED current should the string reconnect, but the channel will not be reconnected to the boost converter feedback. To restore feedback, the EN pin toggled or power cycled OFF and ON. Refer to the Fault Summary table.

The driver continues running with the remaining good strings.

The  $\overline{\text{FLT}}$  pin is asserted low. The fault condition is reset by toggling EN or cycling power.

## Over-temperature Protection (OTP)

OTP is in two stages. OTP1 seeks to reduce die temperature by disconnecting the faulty string. If temperature continues to rise, OTP2 is triggered as a fail safe mechanism, shutting down the driver.

OTP is self-resetting once temperature falls below the reset threshold.

## SLP and OLP Behavior

The process of identifying and disabling the channel having faulty string is two steps: 1) detecting a fault, and 2) determining if the fault is a shorted, partially open (Zener-protected), or fully open LED.

First consider the case with a partially open LED. The faulty channel will be at the 900mV feedback point, while the remaining channels will be relatively higher. Using a conventional approach for SLP, where those channels with an ab-

solute voltage (REF to GND) above a set threshold, the five good strings will be misidentified as shorted and disabled.

Another problem exists with a conventional SLP; it can block activation of OLP. Open strings cause boost voltage to rise in an attempt to achieve 900mV on the faulty channel. The channel with the open string remains at ground, eventually causing VBST to rise until OVP trips. This is the trigger for the OLP circuit, which then identifies and disables channels at 0V. The problem with this approach arises with the good strings: as VBST rises towards OVP, the good strings apply a high voltage to the channel outputs. This can cause SLP to trip before OVP trips, causing good strings to be misinterpreted as shorted and disabled while the open string remains. To reduce the chances of this occurring, the SLP threshold can be set higher, but this may render SLP useless.

The purpose of SLP is to prevent excessive dissipation in the channel output drivers and the resultant rise in die temperature. If die temperature remains reasonable, the shorted LED string can continue to operate, albeit at reduced brightness. Note that little power is wasted in the shorted LED.

For these two reasons the primary mechanism for disabling faulty strings is triggered when die temperature becomes excessive rather than at an arbitrary voltage level. The exceptions are the SLP and OVP limits, which should be high as a fail safe mechanism rather than as the normal trigger for the faulty string protection circuit. Once die temperature reaches the OTP1 threshold, a single string is identified as faulty and disabled. This should reduce internal power dissipation two ways. First, it eliminates the power dissipation in the channel driver with the faulty string. Second, the disconnected string reduces the load on the boost converter, which in turn allows the boost switch to run cooler.

When the die temperature falls below the hysteresis temperature, OTP re-arms after 800ms. If the die temperature has not fallen by the hysteresis temperature, OTP1 is re-triggered. In addition, to prevent the successive disabling of channels following an OLP event, the protection circuit is not re-armed until at least one channel's voltage has fallen below the ACH (All Channels High) threshold. When OTP1 resets and ACH goes low, the protection circuit is re-armed to trigger on another fault, but the previously identified faulty string remains disabled under the assumption that faulty strings do not spontaneously repair themselves. Toggling EN or cycling power resets the faulty strings.

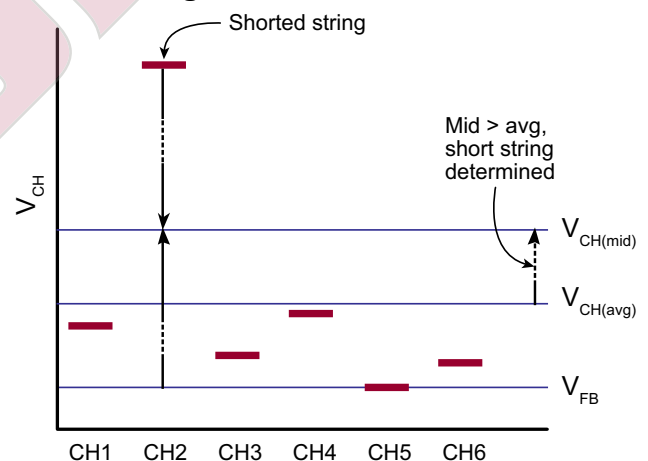
If the disabling of strings does not prevent die temperature

from rising, the second-stage OTP activates, shutting down the boost converter. OTP2 self-resets when die temperature falls by the hysteresis temperature, re-enabling the boost converter but not reconnecting faulty strings.

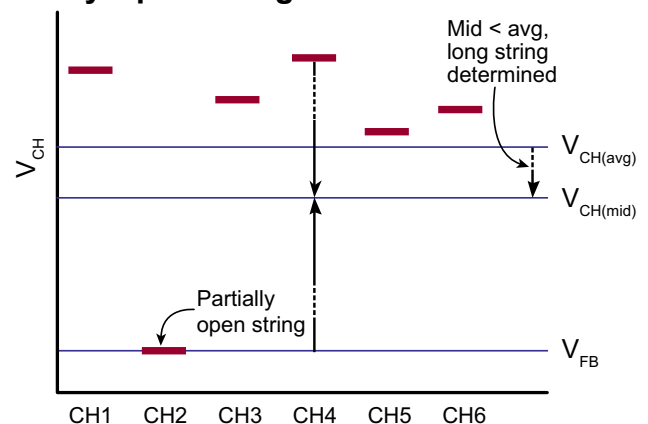
If a string is fully open, the protection circuit cannot wait for the temperature to rise to OTP1 level - in the meantime output voltage would rise to destructive levels. Once OVP is activated, the channel with the open string is identified and disconnected. If more than one string is open, OVP will retrigger and the second open string is disconnected. The cycle repeats as long as there is an open string on an active channel.

Once OTP1 is triggered, a fault condition has been established and the next step is to determine if a short or long string is the cause. An 'outlier' approach is used. Outliers being those channels with a voltage significantly different from the others. The midpoint between the highest and lowest active channels is compared to the average of the active channels to determine whether the faulty string is long or short. The following examples demonstrate the technique.

### Shorted String



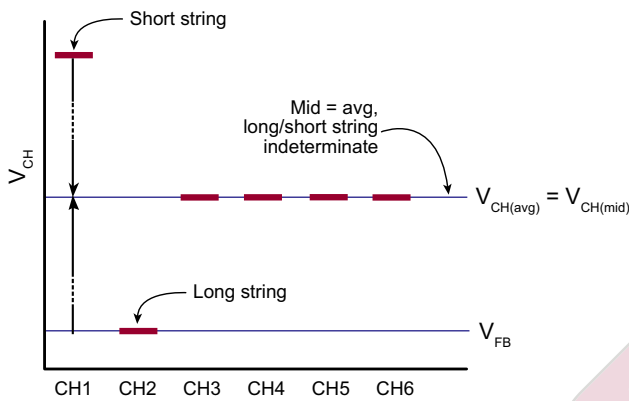
### Partially Open String



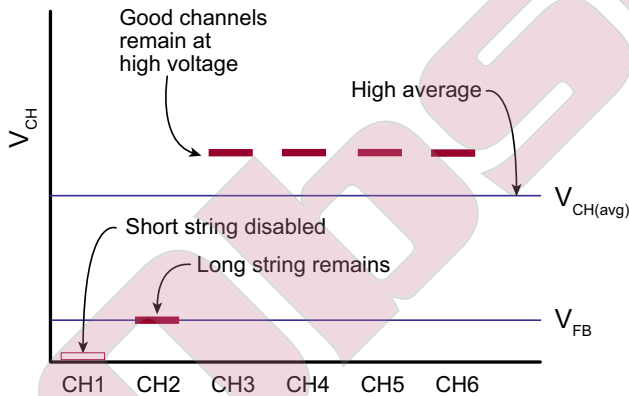
In the previous two examples, only a single faulty string has been considered. A problem arises if one string is long and another short such that the midpoint is at the average. Either the short or long string can be disabled. It is preferable to disable the long string, so a bias is applied to the midpoint favoring the long string. Long strings result in higher driver dissipation, as the following diagrams graphically explain.

In addition to lower driver dissipation, if the long string is caused by an open LED with a protection Zener conducting, power is wasted in the Zener. On the other hand, a shorted LED wastes no (or little) power.

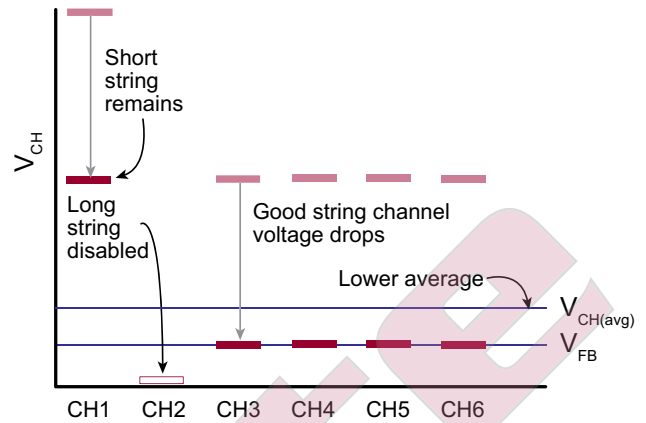
### Long & Short String



### Short String Favored



### Long String Favored



### Under-voltage Lock Out (UVLO)

The boost converter and output drivers will not be enabled until  $V_{DD}$  reaches 4.2V nominal. When  $V_{DD}$  falls by 300mV from the 4.2V turn-ON threshold, the boost converter and output drivers are disabled.

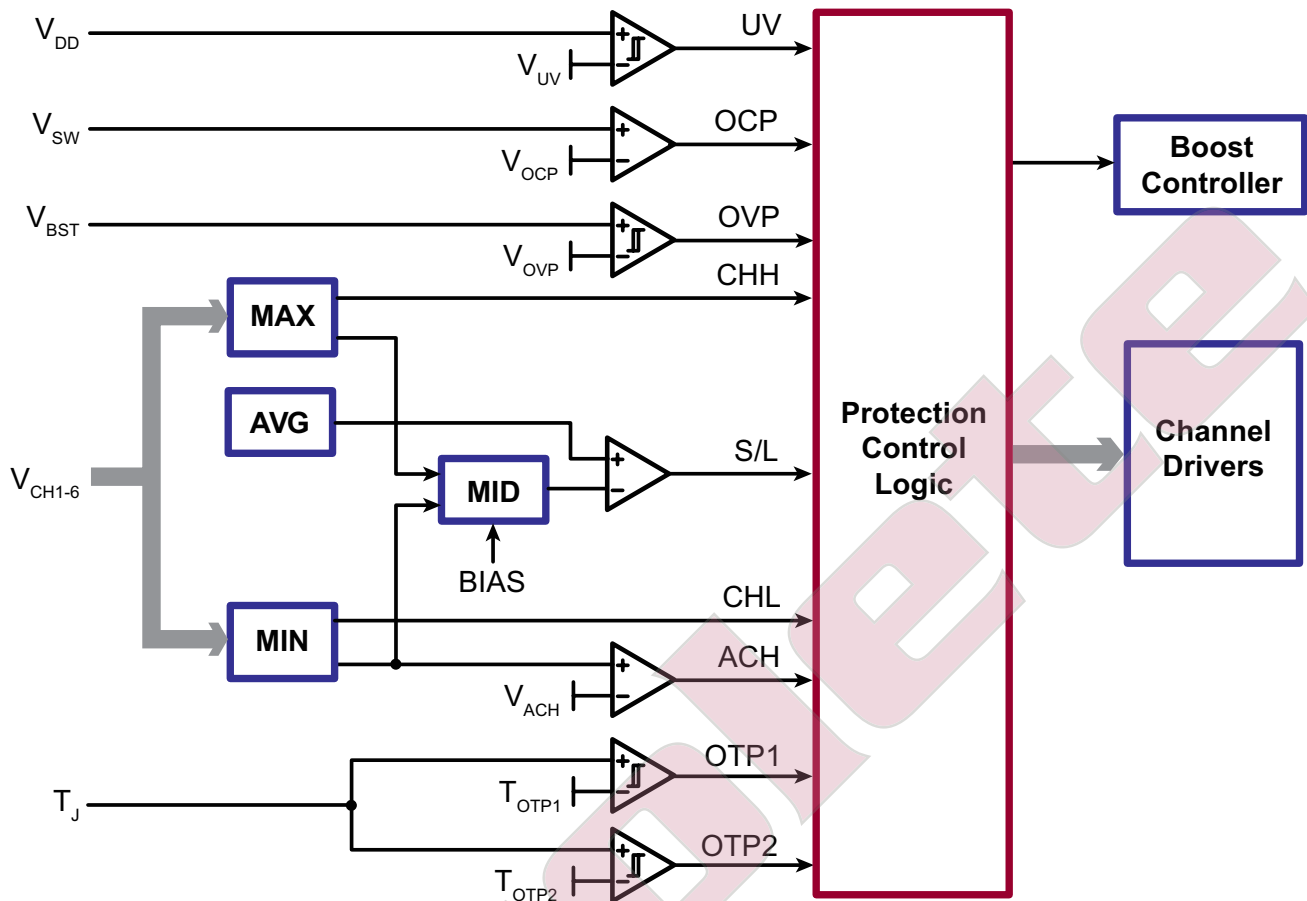
### Fault pin ( $\overline{FLT}$ pin)

The  $\overline{FLT}$  output pin signals a fault condition; SLP, OLP, OCP, or OTP. It is active low and open drain, requiring an external pull-up. It may be wire-or'd with other devices.

The  $\overline{FLT}$  output may be used to generate an interrupt to the host controller.

toggling EN resets both the SLP/OLP circuits and the  $\overline{FLT}$  pin.

## Fault Protection Block Diagram



### Inputs

$V_{DD}$  is supply voltage.  
 $V_{SW}$  is the ON-state boost switch voltage..  
 $V_{BST}$  is the boost converter output voltage.  
 $V_{CH1-6}$  are the voltages at the channel outputs.  
 $T_J$  is the die temperature.

### References

$V_{UV}$  is the  $V_{DD}$  under voltage threshold.  
 $V_{OCP}$  is the boost switch over current protection threshold.  
 $V_{OVP}$  is the boost converter over voltage threshold.  
**BIAS** is the offset applied to the midpoint.  
 $V_{ACH}$  is the All Channels High threshold ( $V_{ACH} > V_{FB}$ ).  
 $T_{OTP1}$  is the over temperature stage 1 protection threshold. ( $T_{OTP1} < T_{OTP2}$ )  
 $T_{OTP2}$  is the over temperature stage 2 protection threshold.

### Functions

**MAX** selects the maximum voltage of all active channels. Outputs the voltage and channel.  
**MIN** selects the minimum voltage of all active channels. Outputs the voltage and channel.  
**MID** finds the midpoint between the highest and lowest active channel voltages.  
**AVG** determines the average voltage of all active channels.

### Inputs to Logic Block

**UV** indicates when the supply voltage is too low.  
**OCP** indicates when the boost switch current is excessive.  
**OVP** indicates when the boost output voltage exceeds the threshold established by  $R_{OVP}$ .  
**CHH** identifies the channel with the highest voltage.  
**CHL** identifies the channel with the lowest voltage.  
**SLP** indicates when a shorted string applies excessive voltage to the channel output.  
**S/L** indicates whether the farthest outlying channel is a short string or a long string (0=short, 1=long).  
**ACH** is all channels high - when all channels are above the regulated feedback voltage.  
**OTP1** indicates when die temperature has become excessive.  
**OTP2** indicates when die temperature has become critical.

Fault Protection Logic Table

UV	OCP	OVP	S/L	ACH	OTP1	OTP2	CHL & CHH	Description
1	X	X	X	X	X	X	X	Shuts down the IC when supply voltage is too low.
0	1	0	X	X	X	0	X	Turns OFF boost converter switch when instantaneous current becomes excessive. Operates cycle-by-cycle. The active channels remain ON, but with a lower $V_{BST}$ some strings may not be lit.
0	0	1	X	X	X	0	X	Shuts down boost converter when output voltage exceeds threshold set by $R_{OVP}$ . The channel outputs are checked for an open string and are disconnected from feedback all at once. The channels remain on to discharge $C_{OUT}$ .  The boost converter is re-enabled when $V_{BST}$ falls below the lower OVP threshold and the voltage at least one channel falls below the $V_{ACH}$ threshold
X	X	X	1	0	1	0	X	Short/Long string. The S/L signal is used to determine if the channel to be disabled has a long string or a short string, with a bias towards a long string.
X	X	X	X	X	X	X	CH	Identifies the channel with the lowest (CHL) and highest (CHH) voltages. In conjunction with S/L, identifies the channel to be disabled.
0	0	0	0	1	0	0	X	All channels High. Indicates when all active channels have a voltage above the regulated feedback voltage, which occurs when a channel with an open or long string is disabled. ACH disables the faulty string protection circuit and turns OFF the boost converter until one channel falls below $V_{ACH}$ . The active channels remain ON when the boost converter is disabled to assure $C_{OUT}$ is discharged.
0	0	0	0	0	1	0	X	Excessive die temperature triggers the faulty string protection circuit, disconnecting a string. If die temperature falls below the hysteresis threshold, OTP1 is re-armed for any subsequent faulty strings. If die temperature rises, OTP2 triggers.
X	X	X	X	X	X	1	X	Critical die temperature immediately shuts down the boost converter. Self-resets when die temperature falls by the hysteresis threshold. The boost converter is re-enabled but faulty strings remain disconnected.

### LED Drive Frequency

The LED drive frequency may be derived from four sources: the SYNC input, the DIM input, an internal resistor-programmable precision oscillator, or a crystal-controlled internal oscillator. If a SYNC signal is present, it is used. If the SYNC signal is not present or <48Hz, the LED drive frequency is established by either the internal oscillator or the DIM signal. If the pin controlling the internal oscillator is pulled to VDD, the DIM input is used. If a resistor to ground is on this pin, the internal oscillator is used. If a crystal is connected to FREF and it is biased between  $0.6V_{DD}$  and  $0.8V_{DD}$ , a crystal oscillator is used.

An internal frequency synthesizer can be used to multiply the selected reference frequency. The Sync Frequency Multiplier (SFM) is set to one of ten possible values by applying a voltage to the SFM pin. The voltage is referenced to VDD, so a resistive voltage divider can be used to set the sync frequency multiplier. If the SFM pin is grounded, the reference frequency (SYNC, DIM, or internal) determines LED drive frequency on a 1:1 basis.

To handle higher DIM frequencies, an additional scaling factor (SCL) of 1/9 is applied for SFM values greater than 1.

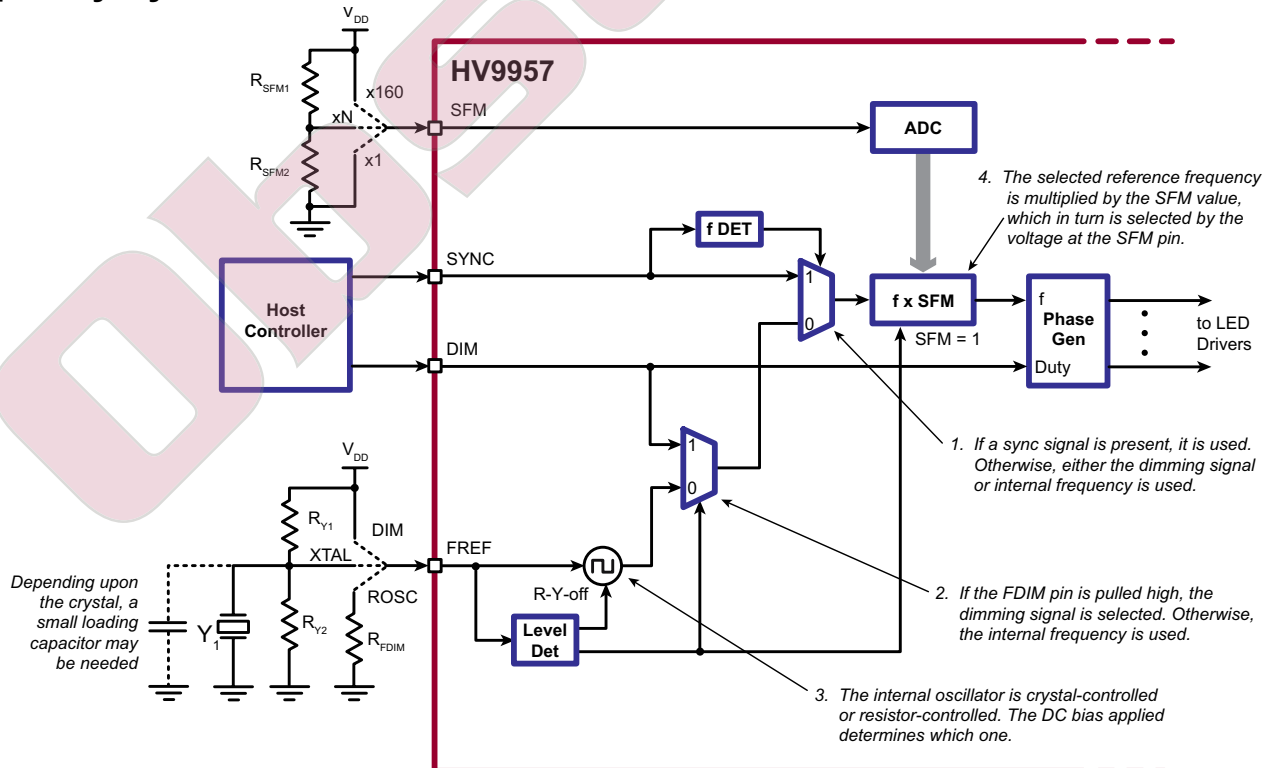
### LED Drive Frequency

$f_{SYNC}$	FREF pin		SFM pin	$f_{CH}$
	Attach	Bias		
Y	$R_{FDIM}$	0V	-	$SFM \times f_{SYNC}$
Y	Xtal	$0.7 \cdot V_{DD}$	-	$SFM \times f_{SYNC}$
Y	Xtal	$V_{DD}$	-	$SFM \times f_{SYNC}$
Y	none	$V_{DD}$	-	Illegal
N	$R_{FDIM}$	0V	-	$SFM \times f_{OSC}$
N	Xtal	$0.7 \cdot V_{DD}$	-	$SFM \times f_{XTAL} / 409,600$
N	none	$V_{DD}$	0V	$SFM \times f_{DIM}$
N	none	$V_{DD}$	>0V	$SFM \times f_{DIM} \times 1/9$

### Boost Frequency

FREF pin		$f_{BOOST}$ (for given $V_{FBST}$ )			
Attach	Bias	0V	$1/3 V_{DD}$	$2/3 V_{DD}$	$V_{DD}$
$R_{FDIM}$	0V	375kHz	500kHz	750kHz	1.0MHz
Xtal	$0.7 \cdot V_{DD}$	$f_{Xtal} / 64$	$f_{Xtal} / 48$	$f_{Xtal} / 32$	$f_{Xtal} / 24$
Xtal	$V_{DD}$	375kHz	500kHz	750kHz	1.0MHz
none	$V_{DD}$	375kHz	500kHz	750kHz	1.0MHz

### Frequency Synthesizer



This schematic is a conceptual presentation and may not reflect actual implementation.



## LED Drive Frequencies for Given Source Frequencies

#	$\frac{V_{SFM}}{V_{DD}}$	SFM	SYNC Input				R-Programmed			XTAL		DIM
			60Hz	120Hz	180Hz	240Hz	250k $\Omega$	200k $\Omega$	125k $\Omega$	24.576 MHz	Har of 60Hz	540Hz
0	0.0	1	60	120	180	240	48.00	60.000	72.00	60	1.000	540
1	0.091	17	1,020	2,040	3,060	4,080	816	1,020	1,224	1,020	17.000	9,180
2	0.182	23	1,380	2,760	4,140	5,520	1,104	1,380	1,656	1,380	23.000	12,420
3	0.273	32	1,920	3,840	5,760	7,680	1,536	1,920	2,304	1,920	32.000	17,280
4	0.364	45	2,700	5,400	8,100	10,800	2,160	2,700	3,240	2,700	45.000	24,300
5	0.455	62	3,720	7,440	11,160	14,880	2,976	3,720	4,464	3,720	62.000	33,480
6	0.545	85	5,100	10,200	15,300	20,400	4,080	5,100	6,120	5,100	85.000	45,900
7	0.636	117	7,020	14,040	21,060	28,080	5,616	7,020	8,424	7,020	117.000	63,180
8	1.000	160	9,600	19,200	28,800	38,400	7,680	<b>9,600</b>	11,520	<b>9,600</b>	160.000	86,400
9	0.727	221	13,260	26,520	39,780	53,040	10,608	13,260	15,912	13,260	221.000	119,340
10	0.818	307	18,420	36,840	55,260	73,680	14,736	18,420	22,104	18,420	307.000	165,780
11	0.909	410	24,600	49,200	73,800	98,400	19,680	24,600	29,520	24,600	410.000	221,400

## Notes:

1. SFM values chosen for 9600Hz,  $R_{osc}$  frequency range and overlap, and xtal harmonics of 60Hz.
2. Row #8 is out of sequence so that 9600Hz may be obtained without resistors (SFM pin =  $V_{DD}$ ).
3. Hatched cells indicate illegal conditions. The PWM duty cycle may be erroneous but no damage to either the HV9957 nor LEDs will be incurred.

### Suggested PCB Layout (top layer)

Switching node with high AC voltage and frequency. Keep trace length short and keep away from sensitive nodes. Wide traces for the switching node, while providing low resistance, increases parasitic capacitance to the ground plane, increasing switching losses.

If sensitive circuitry adjacent to high voltage switching node, include a guard trace.

To provide unbroken ground plane for good heatsinking, do not use thermal relief on ground vias. Other vias requiring a clearance ring should be kept distant from the HV9957.

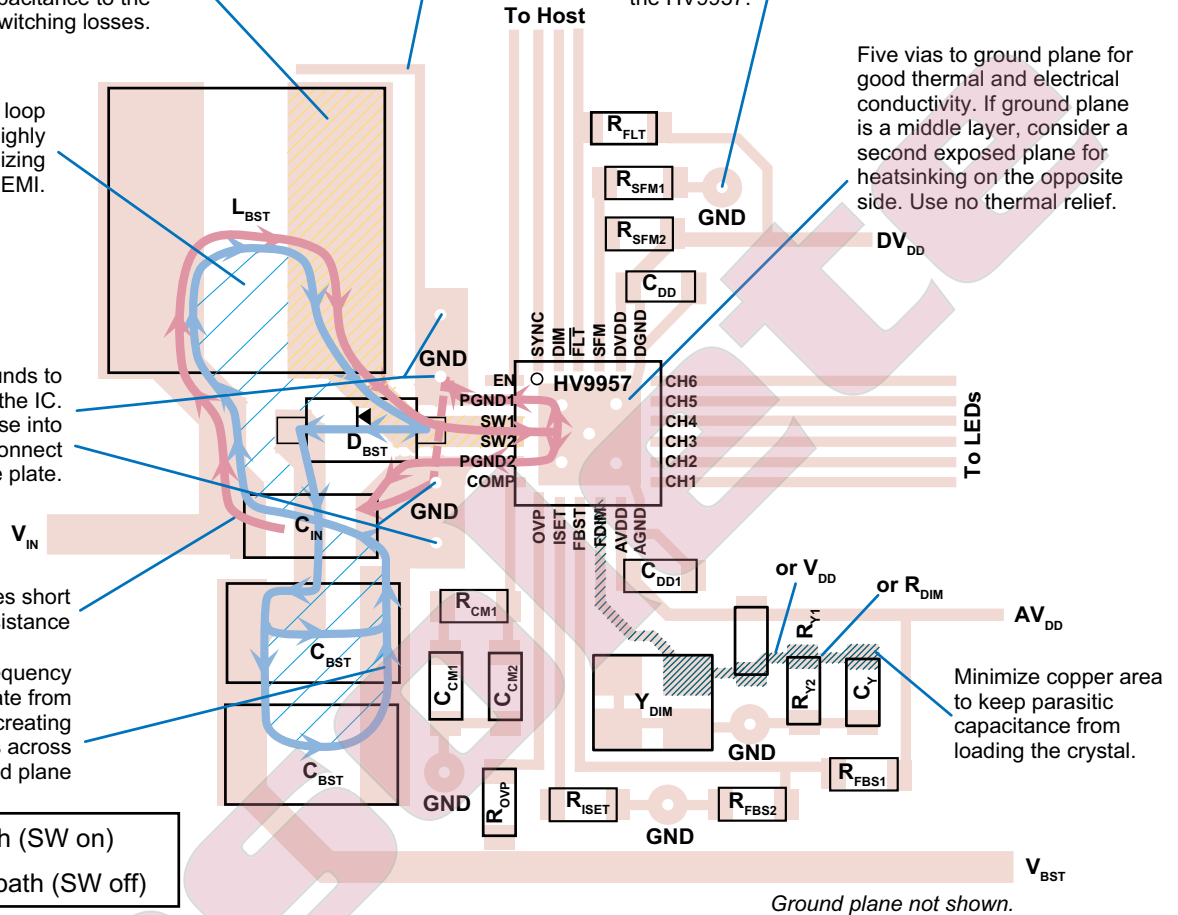
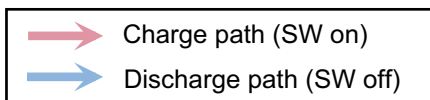
Charge and discharge loop areas small and highly coincident, minimizing radiated EMI.

Five vias to ground plane for good thermal and electrical conductivity. If ground plane is a middle layer, consider a second exposed plane for heatsinking on the opposite side. Use no thermal relief.

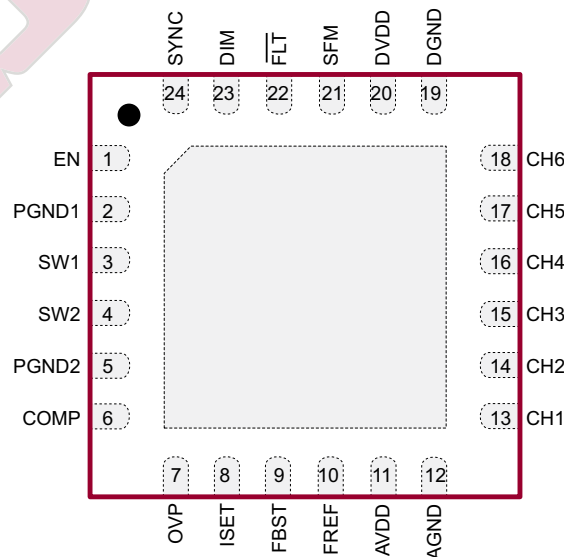
Connect boost grounds to ground plane close to the IC. To avoid injecting noise into the IC, do not directly connect PGND pin to underside plate.

Keep high current traces short to minimize trace resistance

High current, high frequency ground paths separate from ground plane to avoid creating voltage differentials across ground plane



### Pinout (top view)

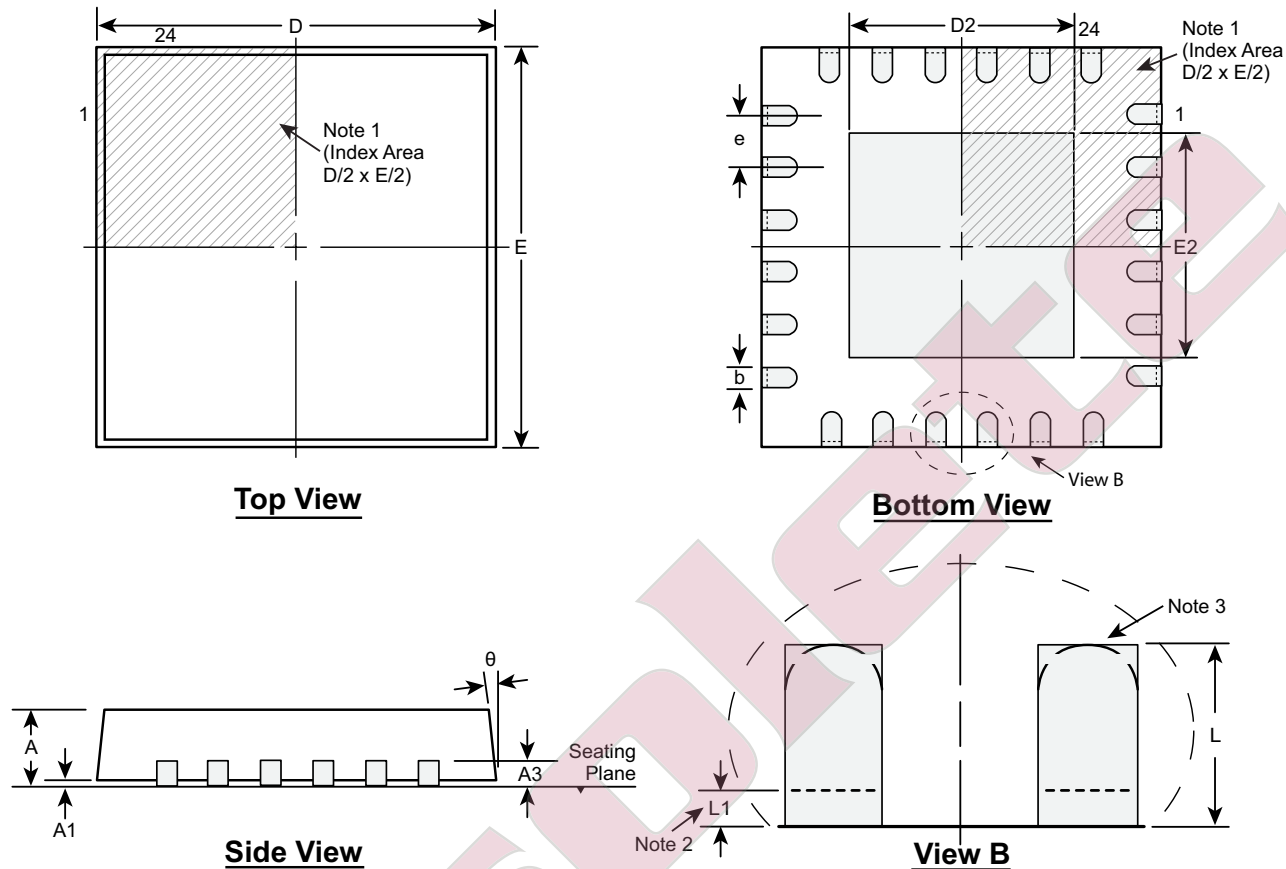


## Pin Description

Pin #	Pin Name	Description
1	EN	Enable input. When held low, shuts down the driver. When briefly toggled low, resets fault protection.
2	PGND1	Boost converter ground. The internal boost converter switch is connected to these pins.
3	SW1	Boost converter internal switch.
4	SW2	
5	PGND2	Boost converter ground. The internal boost converter switch is connected to these pins.
6	COMP	Boost converter loop compensation. An RC network connected between this pin and ground establishes loop stability.
7	OVP	Over voltage protection monitor. Biased at a constant current. A resistor from this pin to $V_{BST}$ sets the OVP threshold.
8	ISET	Output current set. A resistor from this pin to ground establishes full-scale output current.
9	FBST	Sets boost converter frequency.
10	FREF	Determines PWM dimming frequency when a SYNC signal is not present. When VDD applied, the frequency of the DIM signal is used. When a resistor to ground is connected, an internal R-C oscillator is used. When biased at $0.5 - 0.9 \times V_{DD}$ and a crystal connected, an internal crystal oscillator is used.
11	AVDD	Supply for internal analog circuits. Bypass with a $1.0\mu\text{F}$ capacitor to ground.
12	AGND	Analog ground.
13	CH1	Current sink outputs for driving the LED strings.
14	CH2	
15	CH3	
16	CH4	
17	CH5	
18	CH6	
19	DGND	Digital ground.
20	DVDD	Supply input for internal digital circuits. Bypass locally with a $4.7\mu\text{F}$ capacitor to ground.
21	SFM	Determines the sync frequency multiplier for SYNC input, DIM input or internal dimming frequency.
22	$\overline{\text{FLT}}$	Fault output, active low and open drain. An external pull-up is required. May be wire-or'd with other devices.
23	DIM	Input for an externally applied PWM dimming signal.
24	SYNC	Input for synchronizing the PWM drive signal to an external signal. When synchronization is not used, connect SYNC to ground.
Underside Plate		The exposed metal plate on the underside is at ground potential and may be connected to ground or left floating. It provides heat sinking and should be soldered to a copper area on the PCB.

# 24-Lead QFN Package Outline (K7)

4.00x4.00mm body, 0.80mm height (max), 0.50mm pitch



**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	3.85	2.55	3.85	2.55	0.50 BSC	0.25	0.03	0°
	NOM	0.75	0.02		0.25	4.00	2.70	4.00	2.70		0.35	-	-
	MAX	0.80	0.05		0.30	4.15	2.80	4.15	2.80		0.45	0.15	14°

Drawings not to scale.  
 Supertex Doc.#: DSPD-24QFNK74X4P050, Version A031609.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

**Supertex inc.** does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)