

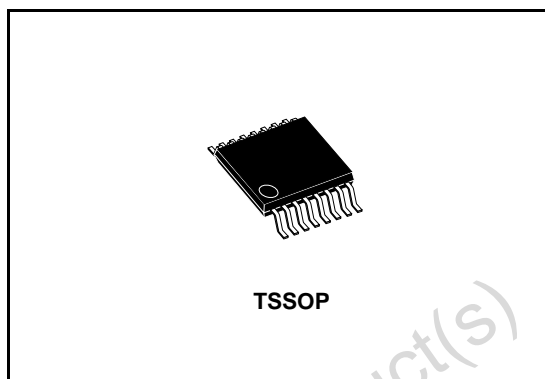
3V LVDS quad cmos differential line driver

Feature summary

- >400 MBPS (200MHz) switching rates
- Flow-through pinout simplifies pcb layout
- 300ps (max.) differential skew
- 1.8 ns (typ.) propagation delay
- 3.3V Power supply design
- ± 350 mV Differential signaling
- Low power dissipation (3.5mW at 3.3V static in tristate)
- Interoperable with existing 5V LVDS receivers
- High impedance on LVDS Output on power down
- Conforms to TIA/EIA-644 LVDS standard
- Industrial operating temperature range (-40 °C to +85 °C)
- Available in surface mount (SOIC) and low profile TSSOP package

Description

The STLVDS47 is a quad CMOS flow-through differential line driver designed for applications requiring ultra low power dissipation and high data rate. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.



The STLVDS47 accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition, the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low die power state of 1.3mW typical. The STLVDS47 has a flow-through pinout for easy PCB layout.

The EN and EN* inputs are ANDed together and control the TRI-STATE output.

The STLVDS47 and companion line receiver (STLVDS48) provide a new alternative to high power pseudo-ECL devices for high-speed point-to-point interface applications.

Order code

Part number	Temperature Range	Package	Comments
STLVDS47BTR	-40 to 85 °C	TSSOP16 (Tape & Reel)	2500 parts per reel

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1 Pin configuration

Figure 1. Pin connections and functional diagram

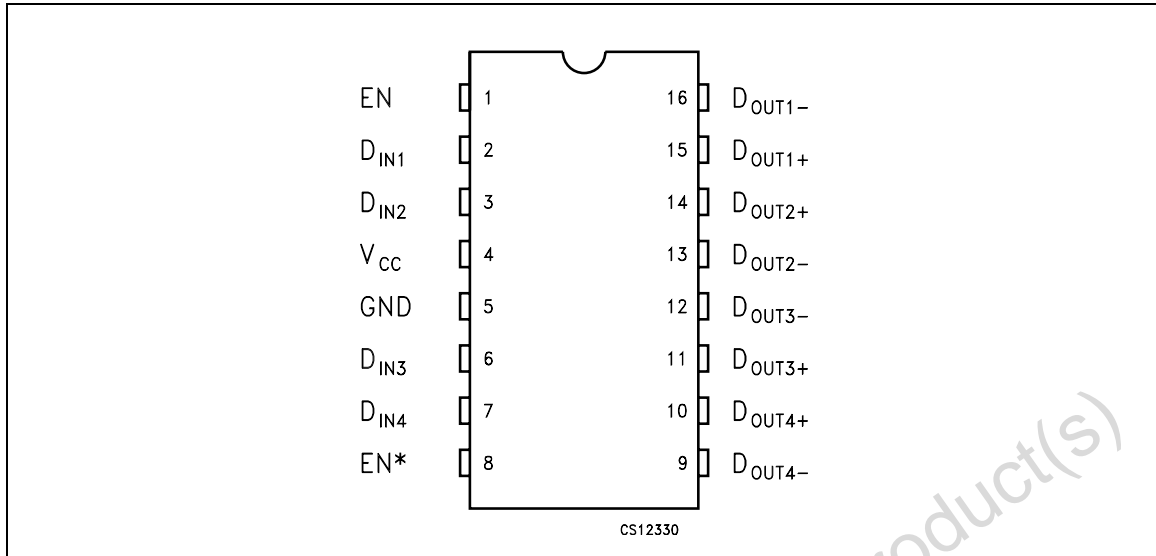
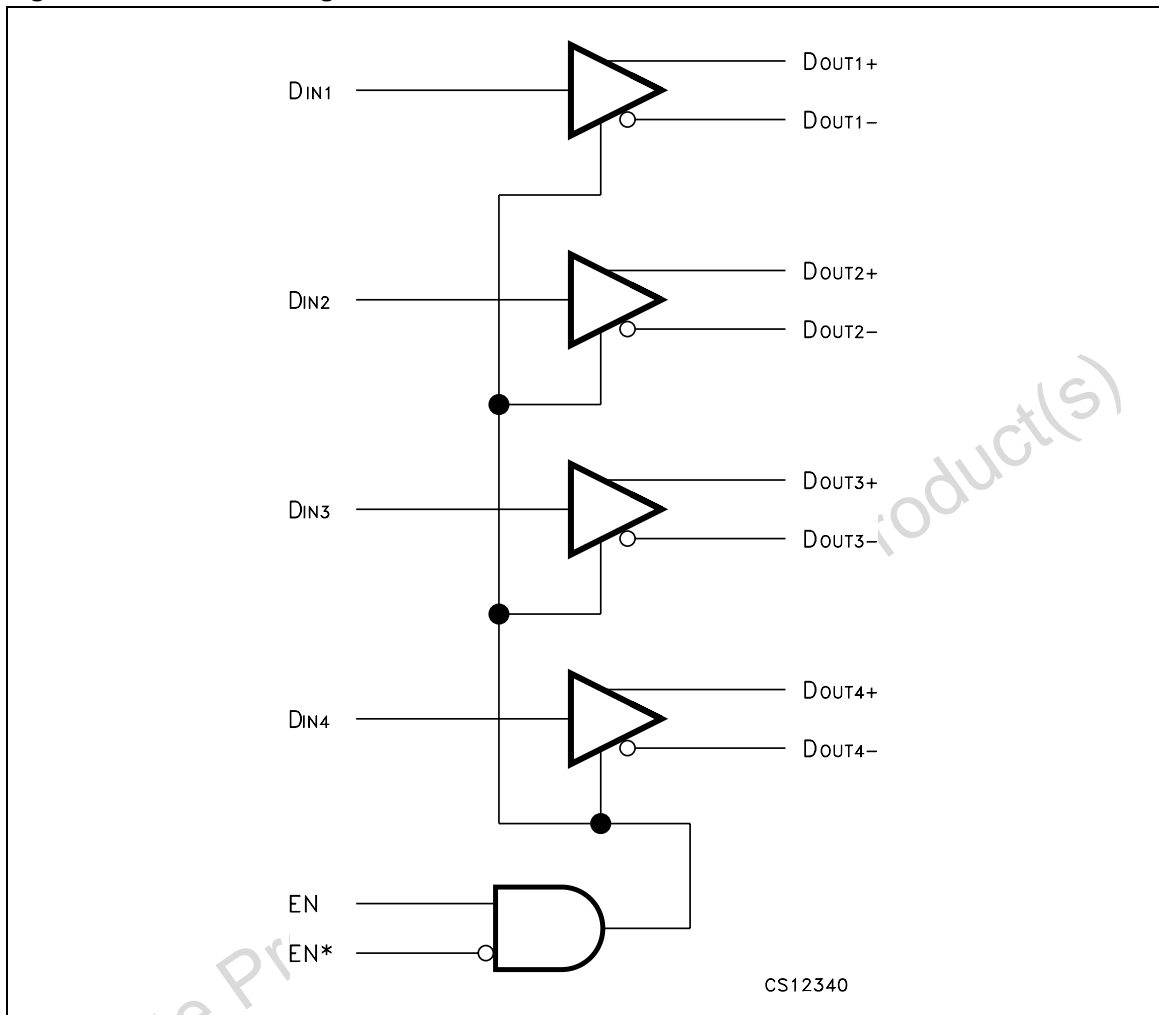


Table 1. Pin description

Pin n°	Symbol	Name and function
1	EN	Enable
2	D _{IN1}	First driver input
3	D _{IN2}	Second driver input
4	V _{CC}	Supply voltage
5	GND	Ground
6	D _{IN3}	Third driver input
7	D _{IN4}	Fourth driver input
8	EN*	Enable (inverting)
9	D _{OUT4-}	Fourth driver inverting output
10	D _{OUT4+}	Fourth driver non-inverting output
11	D _{OUT3+}	Third driver non-inverting output
12	D _{OUT3-}	Third driver inverting output
13	D _{OUT2-}	Second driver inverting output
14	D _{OUT2+}	Second driver non-inverting output
15	D _{OUT1+}	First driver non-inverting output
16	D _{OUT1-}	First driver inverting output

2 Diagram

Figure 2. Functional diagram



3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.3 to 4	V
D_{IN}	Input voltage	-0.3 to 6	V
EN, EN*	Enable input voltage	-0.3 to 6	V
D_{OUT+}, D_{OUT-}	Output voltage	-0.3 to 3.9	V
I_{SCTOUT}	Short circuit duration	Continuous	
T_{stg}	Storage temperature range	-65 to +150	°C

Note: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 3. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
T_A	Operating free-air temperature	-40		85	°C

4 Electrical characteristics

Table 4. Electrical characteristics

(Typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$, $T_A = -40$ to 85°C , unless otherwise specified). (Note 1, 2).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OD1}	Differential output voltage	$R_L = 100\ \Omega$	247	350	454	mV
ΔV_{OD1}	Change in magnitude of V_{OD1} for complementary output states		-35		35	mV
V_{OC}	Offset voltage		1.125	1.2	1.375	V
ΔV_{OC}	Change in magnitude of V_{OS} for complementary output states		-25		25	mV
I_{IH}	Input high current	$V_{IN} = 2\text{V}$			20	μA
I_{IL}	Input low current	$V_{IN} = 0.8\text{V}$			10	μA
I_{OS}	Output short circuit current (Note 3)	ENABLED, $D_{IN} = V_{CC}$, $D_{OUT+} = 0\text{V}$ or $D_{IN} = \text{GND}$, $D_{OUT-} = 0\text{V}$		6	10	mA
I_{OSD}	Differential output short circuit (Note 3)	ENABLED, $V_{OD} = 0\text{V}$		3	10	mA
I_{OFF}	Power-off leakage	$V_{OUT} = 0\text{V}$ or 3.6V , $V_{CC} = 0\text{V}$ or Open			± 1	μA
I_{OZ}	Output TRI-STATE current	$EN = 0.8\text{V}$ and $EN^* = 2\text{V}$ $V_{OUT} = 0\text{V}$ or V_{CC}			± 1	μA
I_{CCL}	Loaded supply current drivers enabled	$R_L = 100\ \Omega$ All Channels, $D_{IN} = V_{CC}$ or GND (all inputs)		18	26	mA
I_{CCZ}	No load supply current drivers disabled	$D_{IN} = V_{CC}$ or GND, $EN = \text{GND}$, $EN^* = V_{CC}$		0.4	1	mA

- Note:
- 1 Current into device pins is defined as positive. Current out of device pins as negative. All voltage are reference to ground except: V_{OD1} and ΔV_{OD1} .
 - 2 The STLVDS47 is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90 Ω to 110 Ω).
 - 3 Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Table 5. Switching characteristics

(Typical values are at $T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 10\%$, $T_A = -40$ to 85°C , unless otherwise specified). (Note 1, 2).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation delay time low-to-high-level output	$R_L = 100\ \Omega$, $C_L = 5\ \text{pF}$	1.6	1.8	2.7	ns
t_{PHL}	Propagation delay time high-to-low-level output		1.6	1.8	2.7	ns
t_r	Differential output signal rise time			0.5	1	ns
t_f	Differential output signal fall time			0.5	1	ns
$t_{SK(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $)			100	300	ps
$t_{SK(o)}$	Channel-to-channel output skew (Note 1)			100	300	ps
$t_{SK(pp)}$	Part-to-part skew (Note 2)				1	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			5.4	10	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			7.4	12	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			3.5	6	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			3.9	6	ns
f_{MAX}	Maximum operating frequency			250		MHz

- Note:
- C_L includes probe and jig capacitance.
 - $t_{SK(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
 - $t_{SK(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with same supply voltage, at the same temperature, and have identical packages and test circuits.

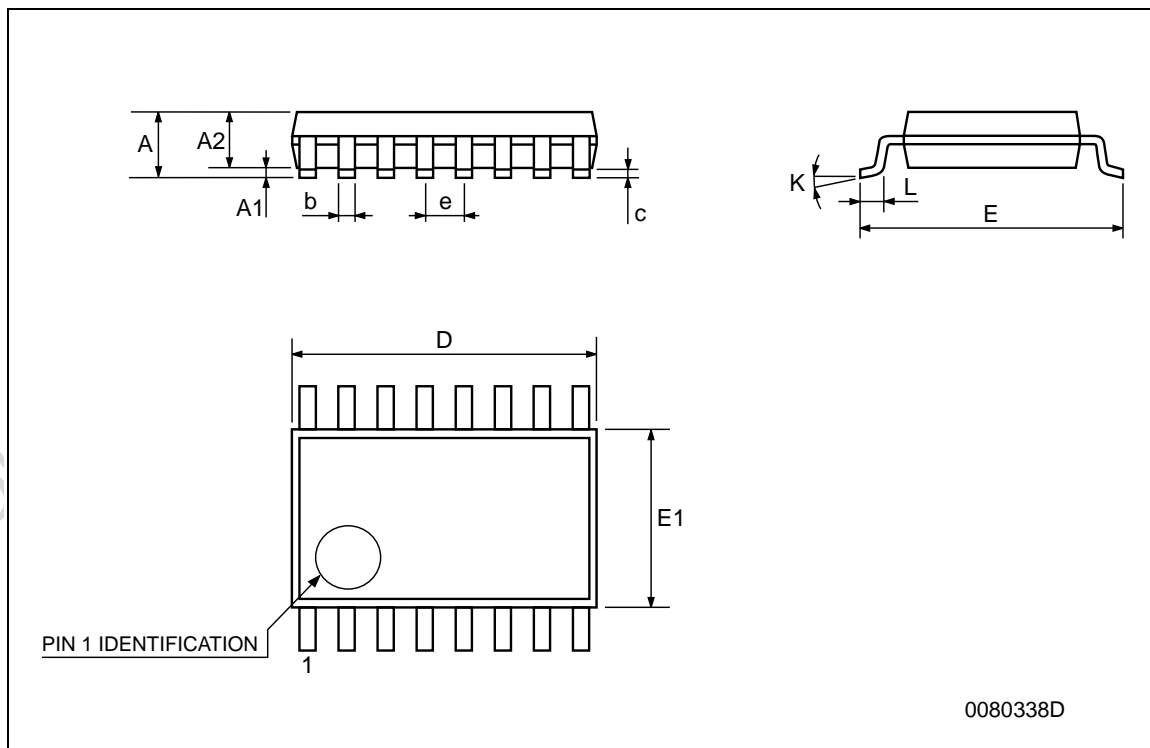
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

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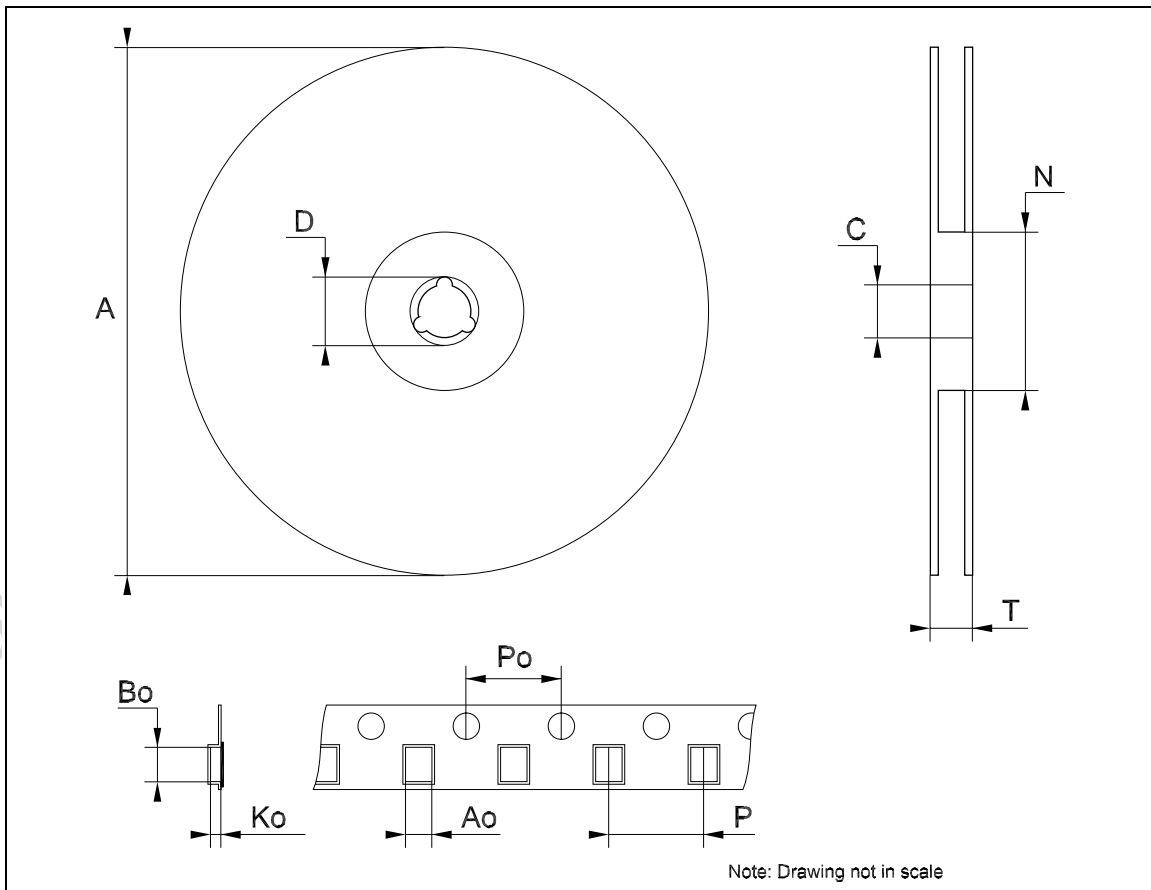
TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Tape & Reel TSSOP16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



6 Revision history

Table 6. Revision history

Date	Revision	Changes
06-Apr-2006	2	Order codes has been updated and new template.

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