Three-Channel CCM/DCM Boost LED Driver with Sub-Microsecond PWM Dimming

Features

- Three out-of-phase constant-current boost converters
- Current loop closed with sub-microsecond PWM dimming pulses supports PWM dimming >20kHz
- Internal 40V linear regulator
- External clock input
- External individual reference inputs
- Individual PWM dimming inputs
- Programmable slope compensation
- +0.2A/-0.4A gate drivers
- Independent short circuit protection with hiccup for each channel
- Latching output open-circuit protection

Applications

- LCD panel backlighting

General Description

The HV9989 is a three-channel peak current mode PWM controller for driving single switch converters in a constant output current mode. It can be used for driving either RGB LEDs or multiple channels of white LEDs.

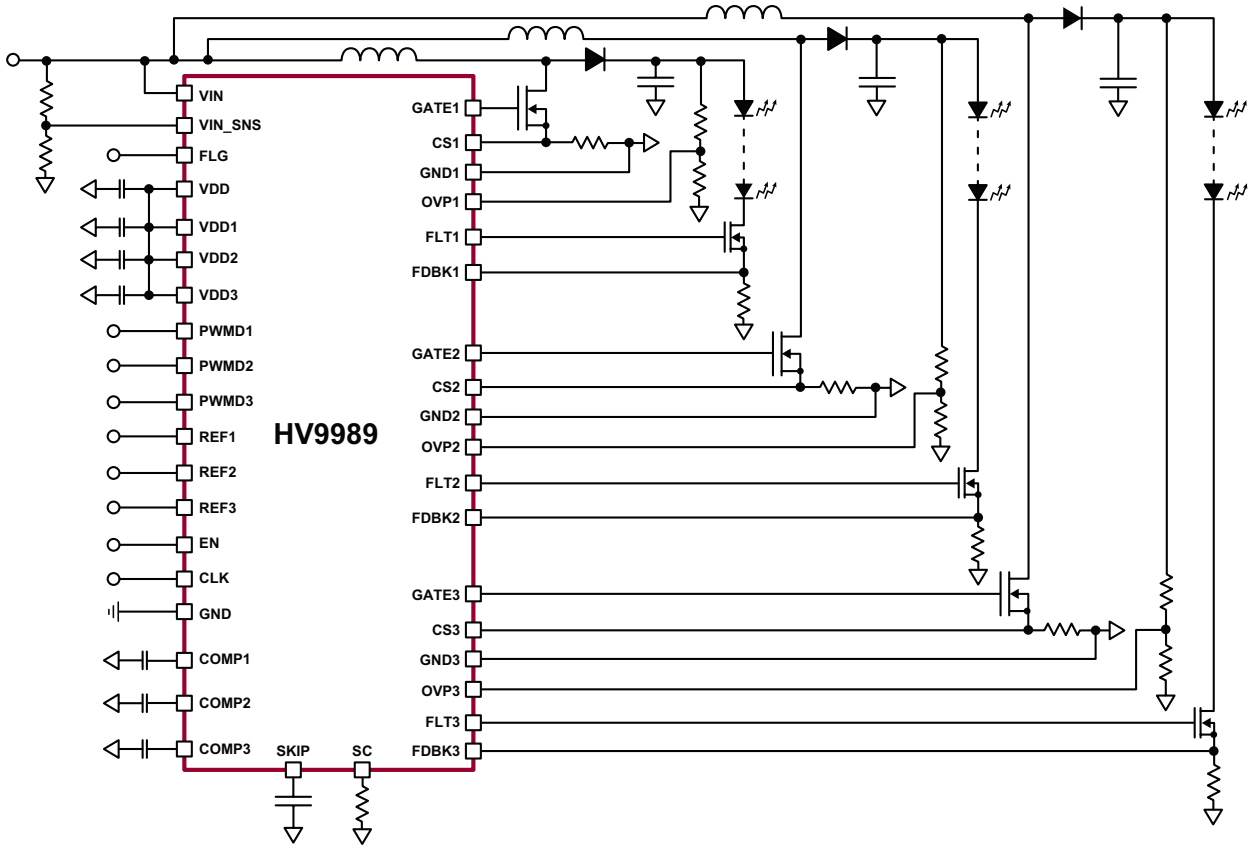
The HV9989 features Supertex's proprietary PWM dimming control algorithm achieving a dimming pulse of a few hundred nanoseconds from a continuous-conduction mode (CCM) or discontinuous-conduction mode (DCM) boost converter, while maintaining the instantaneous LED constant current determined by the external reference voltage input. This feature permits dimming frequency outside of the audible range. The feature can also yield a wide dimming ratio in excess of 10,000:1 at low dimming frequency. Each of the three channels features individual PWM dimming and reference voltage inputs.

The switching frequencies of the three converters are controlled by an external clock signal, such that the channels operate at a switching frequency of 1/12th the external clock frequency and are positioned 120^{O} out-of-phase to reduce the input current ripple.

The HV9989 provides a full protection feature set, including output-short and open-circuit protection, for each individual channel that is independent from the other channels.

The HV9989 is powered by a built-in 40V linear regulator.

Typical Boost Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV9989K6-G	40-Lead (6x6) QFN	490/Tray
HV9989K6-G M935	40-Lead (6x6) QFN	2000/Reel

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

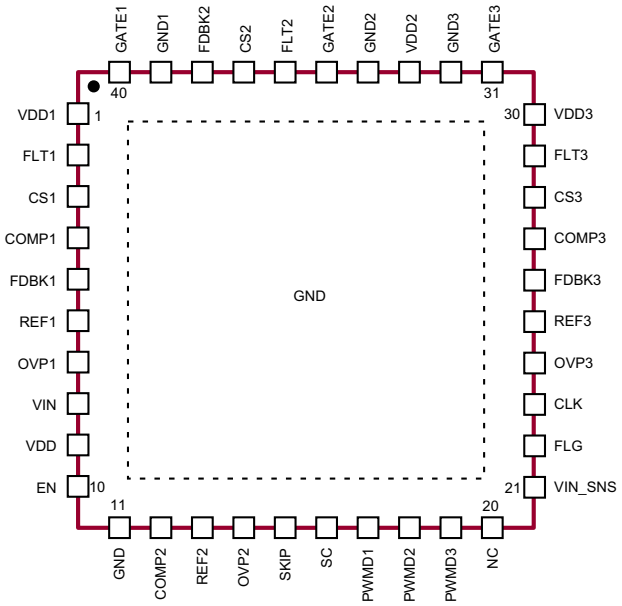
Parameter	Value
VIN to GND	-0.5V to +45V
VDD to GND, VDD 1-3 to GND	-0.3V to +10V
All other pins to GND	-0.3V to (V_{DD} + 0.3V)
Junction temperature	+125°C
Storage ambient temperature range	-65°C to +150°C
Continuous Power dissipation (T_A = +25°C)	4000mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

Package	θ_{ja}
40-Lead QFN	24°C/W

Pin Configuration



40-Lead QFN
(top view)

Product Marking

L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
___ = "Green" Packaging

Package may or may not include the following marks: Si or

40-Lead QFN

Electrical Characteristics

*(The * denotes the specifications which apply over the full operating ambient temperature range 0°C < T_A < +85°C, otherwise the specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD1} = V_{DD2} = V_{DD3} = V_{DD} unless otherwise noted)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage	*	10	-	40	V	DC input voltage
I_{INSD}	Shut-down mode supply current	*	-	-	500	µA	EN = 0.8V
I_{IN}	Supply current	-	-	-	4.5	mA	EN ≥ 2.0V; PWMD1 = PWMD2 = PWMD3 = GND
Internal Regulator							
V_{DD}	Internally regulated voltage	*	7.0	-	8.1	V	V_{IN}= 11V; EN = GND; External I_{DD} = 30mA
ΔV_{DD}	Load regulation	-	-	-	80	mV	V_{IN}= 11V; EN = GND; External $I_{DD(A)}$ = 10mA, $I_{DD(B)}$ = 30mA $\Delta V_{DD} = V_{DD(A)} - V_{DD(B)}$
UVLO	V_{DD} under voltage lockout threshold	-	5.9	-	6.4	V	V_{DD} falling
$UVLO_{HYST}$	V_{DD} under voltage hysteresis	-	-	500	-	mV	V_{DD} rising

\# *Denotes specifications guaranteed by design*
* *The specifications which apply over the full operating temperature range at 0°C < T_A < +85°C are guaranteed by design and characterization.*

Electrical Characteristics *(cont.)*

Sym	Parameter		Min	Typ	Max	Units	Conditions
PWM Dimming (PWMD1, PWMD2 and PWMD3)							
$V_{PWMD(lo)}$	PWMD input low voltage	*	-	-	0.8	V	---
$V_{PWMD(hi)}$	PWMD input high voltage	*	2.0	-	-	V	---
R_{PWMD}	PWMD pull down resistor	-	80	-	160	kΩ	V_{PWMD} = 5.0V
T_d	Delay time to PWMD latch	#	50	-	150	ns	---
T_{DP}	D_{MAX} inhibit delay	#	-	400	-	ns	---
Gate (GATE1, GATE2 and GATE3)							
I_{SOURCE}	Gate short circuit current, sourcing	#	0.2	-	-	A	V_{GATE} = 0V
I_{SINK}	Gate sinking current	#	0.4	-	-	A	V_{GATE} = V_{DD}
T_{RISE}	Gate output rise time	-	-	50	85	ns	C_{GATE} = 1.0nF
T_{FALL}	Gate output fall time	-	-	25	45	ns	C_{GATE} = 1.0nF
D_{MAX}	Maximum duty cycle	#	-	91	-	%	---
Over-voltage Protection (OVP1, OVP2 and OVP3)							
$V_{OVP,rising}$	Over-voltage rising trip point	*	4.7	-	5.4	V	OVP rising
Current Sense (CS1, CS2 and CS3)							
T_{BLANK}	Leading edge blanking	*	210	-	460	ns	---
T_{DELAY}	Delay to GATE	-	-	-	250	ns	50mV overdrive to the current sense comparator
Slope Compensation (SC)							
$C_{SC(EFF)}$	Effective capacitance	#	0.9	1.0	1.1	nF	---
ΔV_{SC}	V_{DD} - to-SC voltage drop	*	1.25	-	3.25	V	R_{SC} = 120kΩ
Internal Transconductance Opamp (Gm1, Gm2 and Gm3)							
GB	Gain bandwidth product	#	-	1.0	-	MHz	75pF capacitance at COMP pin
A_V	Open loop DC gain	-	65	-	-	dB	Output open
K_{COMP}	COMP-to-CS divider ratio	#	-	1/12	-	-	---
V_{CM}	Input common-mode range	#	-0.3	-	3.0	V	---
V_O	Output voltage range	#	0.7	-	6.75	V	---
G_m	Transconductance	-	500	-	700	µA/V	---
V_{OFFSET}	Input offset voltage	-	-5.0	-	5.0	mV	---
I_{BIAS}	Input bias current	#	-	0.5	1.0	nA	---
T_R	Recovery delay	#	-	120	-	ns	FDBK = 0V, REF = 0.5V, PWMD rising
Oscillator (CLOCK)							
f_{OSC1}	Oscillator frequency	-	-	500	-	kHz	F_{CLOCK} = 6.0MHz
K_{SW}	Oscillator divider ratio	#	-	12	-	-	---
Phi1	GATE1 - GATE2 phase delay	#	-	120	-	°	---
Phi1	GATE1 - GATE3 phase delay	#	-	240	-	°	---

 # Denotes specifications guaranteed by design.

** The specifications which apply over the full operating temperature range at $0^oC < T_A < +85^oC$ are guaranteed by design and characterization.*

Electrical Characteristics *(cont.)*

Sym	Parameter		Min	Typ	Max	Unit	Conditions
Oscillator (CLOCK)							
T_{OFF}	CLOCK low time	#	50	-	-	ns	---
T_{ON}	CLOCK high time	#	50	-	-	ns	---
$V_{CLOCK,HI}$	CLOCK input high	*	2.0	-	-	V	---
$V_{CLOCK,LO}$	CLOCK input low	*	-	-	0.8	V	---
Disconnect Driver (FLT1, FLT2 and FLT3)							
$T_{RISE,FAULT}$	Fault output rise time	-	-	-	300	ns	330pF capacitor at FLTx pin
$T_{FALL,FAULT}$	Fault output fall time	-	-	-	200	ns	330pF capacitor at FLTx pin
Short Circuit Protection (all three channels)							
$T_{BLANK,SC}$	Blanking time	*	400	-	800	ns	---
G_{SC}	Gain for short circuit comparator	-	1.9	2.0	2.1	-	---
V_{omin}	Minimum current limit threshold	#	0.15	-	-	V	REF = GND
T_{OFF}	Propagation time for short circuit detection	-	-	-	250	ns	FDBK = 2 • REF + 0.1V
HICCUP timer							
$I_{HC,SOURCE}$	Current source at SKIP pin used for hiccup mode protection	-	-	10	-	µA	---
ΔV_{CAP}	SKIP voltage swing	#	-	4.0	-	V	---
Low output detection (OVP1, OVP2, OVP3, VIN_SNS, FLG)							
$V_{OVP\_OS\_F}$	OVP offset voltage	*	-25	-	25	mV	OVP falling
$V_{OVP\_OS\_R}$	OVP offset voltage	-	40	-	70	mV	OVP rising
$V_{FLG(LOW)}$	FLG low voltage	-	0	-	0.4	V	I(FLG) = 1.0mA
V_{IN_CM}	Input common-mode range	#	-0.3	-	5.0	V	---

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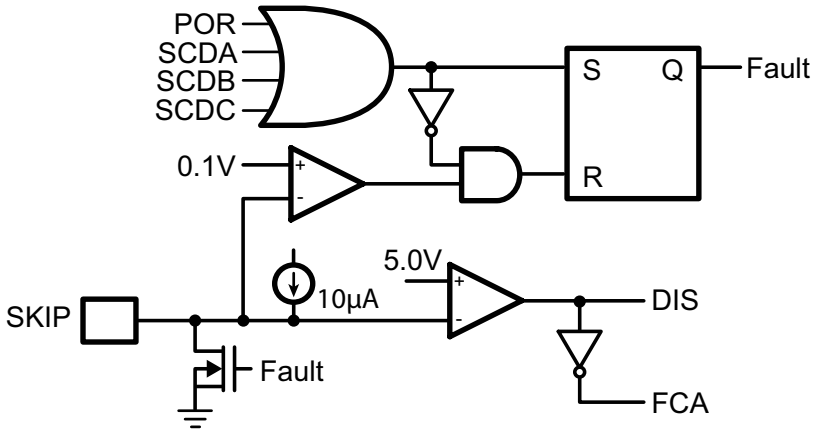
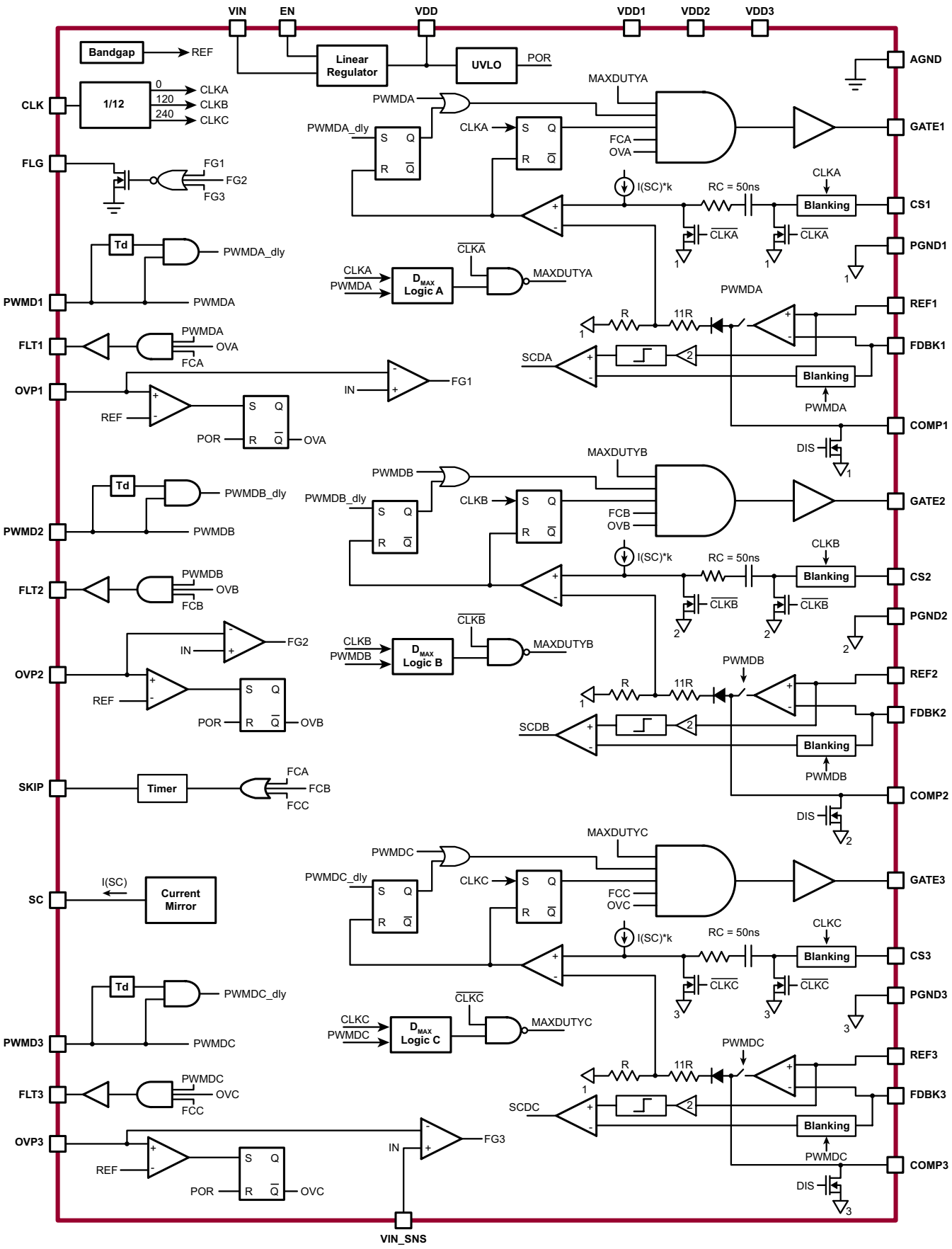
Timer Circuit



Internal Block Diagram



Functional Description

Power Topology

The HV9989 is a three-channel, switch mode converter LED driver designed to control a continuous conduction mode boost or SEPIC converter in a constant frequency mode. The IC includes an internal linear regulator, which operates from 10 to 40V input voltages. The IC can also be powered directly using the VDD pins and bypassing the internal linear regulator. The IC includes features typically required in LED drivers like open LED protection, output short circuit protection, linear and PWM dimming, programmable input current limiting and accurate control of the LED current. A high current gate drive output enables the controller to be used in high power converters. The IC is ideally suited for backlight applications using either RGB or multi-channel white LED configurations.

Power Supply to the IC (VIN, VDD, VDD1-3)

The HV9989 can be powered directly from its VIN pin that takes a voltage up to 40V. When a voltage is applied at the VIN pin, the HV9989 tries to maintain a constant 7.75V (typ) at the VDD pin. The regulator also has a built in under-voltage lockout which shuts off the IC if the voltage at the VDD pin falls below the UVLO threshold. By connecting this VDD pin to the individual VDD pins of the three channels, the internal regulator can be used to power all three channels in the IC.

In case the internal regulator is not utilized, an external power supply (7 - 9V) can be used to power the IC. In this case, the power supply is directly connected to the VDD pins and the VIN pin is left unconnected.

All four VDD pins must be bypassed by a low ESR capacitor (≥0.1µF) to provide a low impedance path for the high frequency current of the output gate driver. These capacitors must be referenced to the individual grounds for proper noise rejection (see Layout Guidelines section for more information). Also, in all cases, the four VDD pins *must* be connected together externally.

The input current drawn from the external power supply (or VIN pin) is a sum of the 4mA current drawn by the all the internal circuitry (for all three channels) and the current drawn by the gate drivers (which in turn depends on the switching frequency and the gate charge of the external FET).

$$I_{IN} = 4mA + (Q_{G1} + Q_{G2} + Q_{G3}) \bullet f_S$$

In the above equation, f_S is the switching frequency of the converters and Q_{G1-3} are the gate charges of the external FETs (which can be obtained from the FET datasheets).

The EN pin is a TTL compatible input used to disable the IC. Pulling the EN pin to GND will shut down the IC and reduce the quiescent current drawn by the IC to be less than 500µA. If the enable function is not required, the EN pin can be connected to VDD.

Clock Input (CLK)

The switching frequency of the converters are set by using a TTL compatible square wave input at the CLK pin. The switching frequencies of the three converters will be 1/12th the frequency of the external clock.

Current Sense (CS1-3)

The current sense input is used to sense the source current of the switching FET. The CS input of the HV9989 includes a built in 100ns (minimum) blanking time to prevent spurious turn off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 12 (including the internal diode drop). This stepped-down voltage is given to one of the comparators as the current reference.

It is recommended that the sense resistor R_{CS} be chosen so as to provide about 250mV current sense signal.

Slope Compensation

For continuous conduction mode converters operating in the constant frequency mode, slope compensation becomes necessary to ensure stability of the peak current mode controller, if the operating duty cycle is greater than 0.5. Choosing a slope compensation which is one half of the down slope of the inductor current ensures that the converter will be stable for all duty cycles.

Slope compensation in the HV9989 can be programmed by a single resistor at SC input common for all three channels. Assuming a down slope of DS (A/ms) for the inductor current, the SC resistor can be computed as:

$$R_{SC} = \frac{2 \bullet (V_{DD} - \Delta V_{SC})}{DS \bullet 10^6 \bullet R_{CS} C_{SC(EFF)}} \approx \frac{11\mu V}{DS \bullet R_{CS} C_{SC(EFF)}}$$

where R_{CS} is the current sense resistor at the CS_X inputs.

Control of the LED Current

The LED currents in the HV9989 are controlled in a closed-

loop manner. The current references which set the three LED currents are provided at the REF pins (REF1-3). This reference voltage is compared to the FDBK voltages (FDBK1-3) which sense the LED currents in the three channels using current sense resistors. The HV9989 includes three 1MHz transconductance amplifiers with tri-state outputs, which are used to close the feedback loops and provide accurate current control. The compensation networks are connected at the COMP pins (COMP1-3).

The outputs of the op-amps are buffered and connected to the current sense comparators using 12:1 dividers. The buffer helps to prevent the integrator capacitor from discharging during the PWM dimming state.

The outputs of the op-amps are controlled by the signal applied to the PWMD pins (PWMD1-3). When PWMD is high, the output of the op-amp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor will force the converter into steady state almost instantaneously.

Linear Dimming

Linear dimming can be accomplished in the HV9989 by varying the voltages at the REF pins. Note that since the HV9989 is a peak current mode controller, it has a minimum on-time for the GATE outputs. This minimum on-time will prevent the converters from completely turning off even when the REF pins are pulled to GND. Thus, linear dimming cannot accomplish true zero LED current. To get zero LED current PWM dimming has to be used. Note that different signals can be connected to the three REF pins if desired, and they need not be connected together.

Due to the offset voltage of the short circuit comparator as well as the non-linearity of the X2 gain stage, pulling the REF pin very close to GND would cause the internal short circuit comparator to trigger and shut down the IC. To overcome this, the output of the gain stage is limited to 125mV (minimum), allowing the REF pin to be pulled all the way to 0V without triggering the short circuit comparator.

Note: *Since this control IC is a peak current mode controller, pulling the REF pin to zero will not cause the LED current to go to zero. The converter will still be operating at it minimum on-time causing a very small current to flow through the LEDs. To get zero LED current, the PWMD input has to be pulled to GND.*

PWM Dimming

PWM dimming in the HV9989 can be accomplished using a TTL compatible square wave source at the PWMD1-3 pins.

The HV9989 has an enhanced PWM dimming capability, which allows PWM dimming to widths less than one switching cycle with no drop in the LED current.

The enhanced PWM dimming performance of the HV9989 can be best explained by considering typical boost converter circuits without this functionality. When the PWM dimming pulse becomes very small (less than one switching cycle for a DCM design or less than a few switching cycles for a CCM design), the boost converter is turned off before the input current can reach its steady state value. This causes the input power to drop, which is manifested in the output as a drop in the LED current (Figure. 5; for a CCM design).

Figure 5a: PWM Dimming with dimming on-time far greater than one switching time period

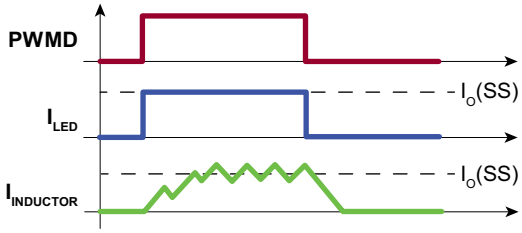
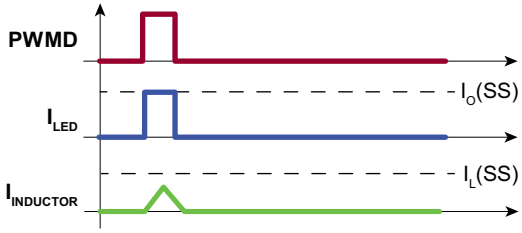


Figure 5b: PWM Dimming with dimming on-time equal to one switching time period

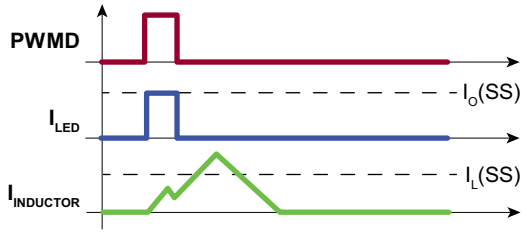


In the above figures, I_O(SS) and I_L(SS) refer to the steady state values (PWMD = 100%) for the output current and inductor current respectively. As can be seen, the inductor current does not rise enough to trip the CS comparator. This causes the closed loop amplifier to lose control of the LED current and COMP rails to VDD.

In the HV9989, however, this problem is overcome by keeping the boost converter ON, even though PWMD has gone to zero to ensure enough power is delivered to the output.

Thus, the amplifier still has control over the LED current and the LED current will be in regulation as shown in Figure. 6.

Figure 6: PWM Dimming with dimming on-time equal to one switching time period with the HV9989



Note that the GATE output is not limited by its maximum duty cycle D_{MAX} past the PWMD signal trailing edge. The gate is kept on until the corresponding CS reference is met by $I_{INDUCTOR}$.

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The FLT pin goes low, turning off the disconnect switch. However, the boost FET is kept running.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The chosen filter capacitor should be large enough so that it can absorb the inductor energy without significant change of the voltage across it. If the capacitor voltage change is significant, it would cause a turn-on spike in the inductor current when PWMD goes high.

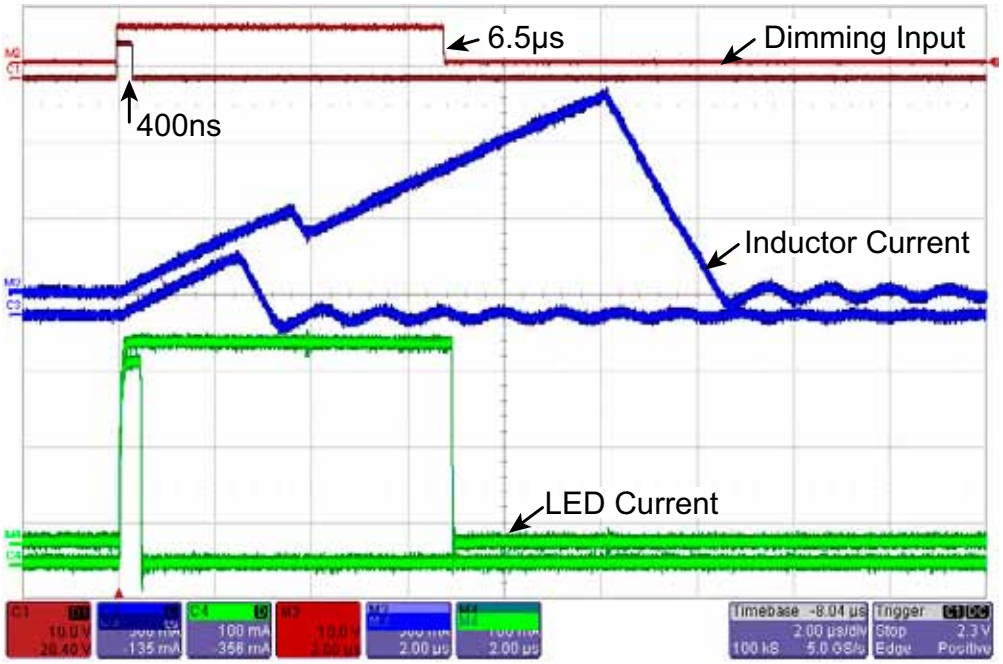
SKIP Timer Logic

During the power-on reset (POR) state upon startup, both GATE and FLT outputs are disabled. The COMP pins and the SKIP pin are pulled to GND.

When an output over-current condition is detected in any individual channel, the corresponding GATE and FLT outputs are disabled, and the corresponding COMP output is pulled to GND. The remaining channel GATE, FLT and COMP outputs are not affected. The SKIP pin is pulled to GND. If pulling FLT low clears the over-current condition in the faulty channel, and once the voltage at the SKIP pin falls below 1.0V, the capacitor at the SKIP pin is released and is charged slowly by a 10µA current source. Once the capacitor is charged to 5.0V, the COMP pins are released and GATE and FLT pins are allowed to turn on. If the hiccup time is long enough, it will ensure that the compensation networks are all completely discharged and that the converters start at minimum duty cycle.

If, during the charging phase of the SKIP output, an over-current condition is detected in another channel, the SKIP pin is pulled to GND again, and the ramp starts over. All faulty channels make an attempt to recover at the same time, when the FLT capacitor is charged to 5.0V. Operation of other “good” channel(s) is not affected by the SKIP pin status.

Figure 7: Deep PWM dimming performance: LED current maintained in regulation



The hiccup timing capacitor can be programmed as:

$$C_{RAMP} = \frac{10\mu A \bullet t_{HICCUP}}{4V}$$

Short Circuit Protection

When a short circuit condition is detected (output current becomes higher than twice the steady state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the short circuit condition disappears. At this time, the hiccup timer is started (Figure. 3). Once the timing is complete, the converter attempts to restart. If the fault condition still persists, the converter shuts down and goes through the cycle again. If the fault condition is cleared (due to a momentary output short) the converter will start regulating the output current normally. This allows the LED driver to recover from accidental shorts without having to reset the IC.

During short circuit conditions, there are two conditions that determine the hiccup time.

The first is the time required to discharge the compensation capacitors. Assuming a pole-zero R-C network at the COMP pin (series combination of R_Z and C_Z in parallel with C_C),

$$t_{COMP,n} = 3 \bullet R_{Zn} \bullet C_{Zn}$$

where n refers to the channel number.

In case the compensation networks are only type 1 (single capacitor), then:

$$t_{COMP,n} = 3 \bullet 300\Omega \bullet C_{Cn}$$

Thus, the maximum compensation time required can be computed as:

$$t_{COMP,MAX} = max\ (t_{COMP1}, t_{COMP2}, t_{COMP3})$$

The second is the time required for the inductors to completely discharge following a short circuit. This time can be computed as:

$$t_{ind,n} = \frac{\pi}{4}\sqrt{L_n \bullet C_{On}}$$

where L and C_O are the input inductor and output capacitor of each power stage.

Thus, the maximum time required to discharge the inductors can be computed as:

$$t_{IND,MAX} = max\ (t_{IND1}, t_{IND2}, t_{IND3})$$

The hiccup time is then chosen as:

$$t_{HICCUP} = max\ (t_{COMP,MAX}, t_{IND,MAX})$$

False Triggering of the Short Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string causes a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short circuit comparator, it will cause the IC to falsely detect an over current condition and shut down.

In the HV9989, to prevent these false triggerings, there is a built-in 500ns blanking network for the short circuit comparator. This blanking network is activated when the PWMD input goes high. Thus, the short circuit comparator will not see the spike in the LED current during the PWM dimming turn-on transition. Once the blanking timer is complete, the short circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWM dimming signal goes high, the total detection time will be:

$$t_{DETECT1} = t_{BLANK} + t_{DELAY} \approx 950ns\ (max)$$

If the short circuit occurs when the PWM dimming signal is already high, the time to detect will be:

$$t_{DETECT1} = t_{DELAY} \approx 250ns\ (max)$$

Over-voltage Protection

The HV9989 provides latching over-voltage protection. When the load is disconnected in a boost converter, the output voltage rises as the output capacitor starts charging. When the output voltage reaches the OVP rising threshold, the HV9989 detects an over-voltage condition and turns off the converter. The converter is turned back on only when the EN pin is toggled.

In most designs, the lower threshold voltage of the over-voltage protection when the converter will be turned on will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED

string voltage will cause a spike in the output current when the FLT signal goes high. This causes a short circuit to be detected and the HV9989 will go into short circuit protection. This behavior continues till the output voltage becomes lower than the LED string voltage at which point, no fault will be detected and normal operation of the circuit will commence.

Input-Output Voltage Comparator

The HV9989 includes a circuit for detecting any of the three boost converter output voltages falling below the input voltage. The input voltage is monitored at the VIN_SNS input using a resistor divider having the same ratio as the OVP1-3 resistor dividers. An open-drain FLG output reports a high impedance state when the voltage at either of the OVP1-3 inputs falls below VIN_SNS. The FLG output recovers into the low-impedance state when the faulty OVP input voltage becomes greater than VIN_SNS by a 55mV hysteresis.

A pull-up resistor should be added at FLG. The FLG output can sink up to 1.0mA.

Pin Description

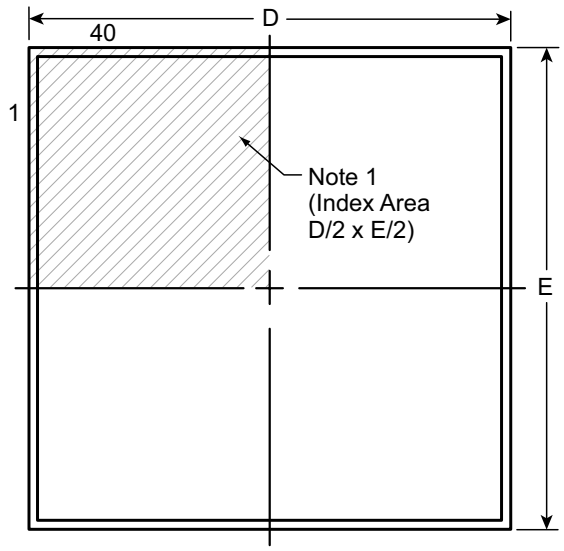
Pin #	Name	Description
1	VDD1	This pin is the power supply pin for channel 1. It can either be connected to the VDD pin or supplied with an external power supply. It must be bypassed with a low ESR capacitor to their respective GND1 (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally.
2	FLT1	This pin is used to drive external disconnect switches. The disconnect switches are used to protect the LEDs in case of fault conditions, and also help to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
3	CS1	This pin is used to sense the souce current of the external power FET used with channel 1. It includes a built-in 210ns (min) blanking timer.
4	COMP1	Stable closed loop control can be accomplished by connecting a compensation network between the COMP pin and its GND.
5	FDBK1	This pin provides output current feedback for channel 1 by using a current sense resistor.
6	REF1	The voltages at this pin sets the output current level for channel 1. Recommended voltage range for this pin is 0V – 1.25V.
7	OVP1	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 5V, channel 1 of the HV9989 is turned off. The fault is reset by re-enabling the IC using the EN pin.
8	VIN	This is the input of the internal 40V linear regulator.
9	VDD	This pin is the output of the linear regulator. It maintains a regulated 7.75V as long as the voltage of the VIN pin is between 10 and 40V. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF). This pin can be used as a power supply for the three channels.
10	EN	When the pin is pulled below 0.8V, the IC goes into a standby mode and draws minimal current.
11	GND	This is the ground connection for the common circuitry in the HV9989.
12	COMP2	Stable closed loop control can be accomplished by connecting a compensation network between the COMP pin and its GND.
13	REF2	The voltages at this pin sets the output current level for channel 2. Recommended voltage range for this pin is 0 – 1.25V.
14	OVP2	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 5V, channel 2 of the HV9989 is turned off. The fault is reset by re-enabling the IC using the EN pin.
15	SKIP	This pin programs the hiccup timer for short circuit fault on any of the three channels. A capacitor to GND programs the hiccup time.
16	SC	This pin sets the current to program slope compensation voltage ramp at the three CS inputs. Connect a resistor to GND.
17	PWMD1	This pin is used to PWM dim channel 1.
18	PWMD2	This pin is used to PWM dim channel 2.
19	PWMD3	This pin is used to PWM dim channel 3.

Pin Description *(cont.)*

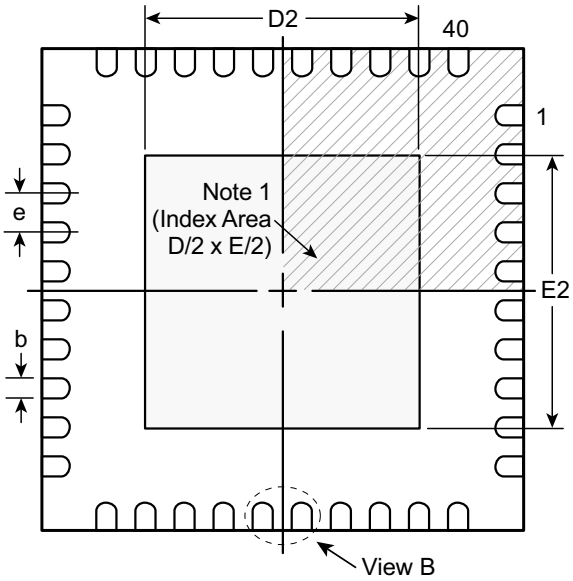
Pin #	Name	Description
20	NC	No connection.
21	VIN_SNS	When voltage at this pin exceeds any of the voltages at OVP 1-3, the high-impedance state is issued at the FLG output.
22	FLG	This is an open-drain logic output reporting a high-impedance state in the case of any of the OVP 1-3 voltages falling below the VIN_SNS voltage. A hysteresis is added at VIN_SNS to avoid oscillation.
23	CLK	This pin is the clock input for the HV9989. The input to the CLK pin should be a TTL compatible square wave signal. The three channels will switch at 1/12th the switching frequency of the signal applied at the CLK pin.
24	OVP3	This pin provides the over voltage protection for the converter. When the voltage at this pin exceeds 5V, channel 3 of the HV9989 is turned off. The fault is reset by re-enabling the IC using the EN pin.
25	REF3	The voltages at this pin sets the output current level for channel 3. Recommended voltage range for this pin is 0V – 1.25V.
26	FDBK3	This pin provides output current feedback for channel 3 by using a current sense resistor.
27	COMP3	Stable closed loop control can be accomplished by connecting a compensation network between the COMP pin and its GND.
28	CS3	This pin is used to sense the souce current of the external power FET used with channel 3. It includes a built-in 210ns (min) blanking timer.
29	FLT3	This pin is used to drive external disconnect switches. The disconnect switches are used to protect the LEDs in case of fault conditions and also help to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
30	VDD3	This pin is the power supply pin for channel 3. It can either be connected to the VDD pin or supplied with an external power supply. It must be bypassed with a low ESR capacitor to their respective GND3 (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally.
31	GATE3	This pin is the output gate driver for the external N-channel power MOSFET.
32	GND3	Ground return for channel 3. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
33	VDD2	This pin is the power supply pin for channel 2. It can either be connected to the VDD pin or supplied with an external power supply. It must be bypassed with a low ESR capacitor to their respective GND2 (at least 0.1µF). All VDD pins (VDD, VDD1-3) must be connected together externally.
34	GND2	Ground return for channel 2. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
35	GATE2	This pin is the output gate driver for the external N-channel power MOSFET.
36	FLT2	This pin is used to drive external disconnect switches. The disconnect switches are used to protect the LEDs in case of fault conditions and also help to provide excellent PWM dimming response by disconnecting and reconnecting the LEDs from the output capacitor during PWM dimming.
37	CS2	This pin is used to sense the souce current of the external power FET used with channel 2. It includes a built-in 210ns (min) blanking timer.
38	FDBK2	This pin provides output current feedback for channel 2 by using a current sense resistor.
39	GND1	Ground return for channel 1. It is recommended that all the GNDs of the IC be connected together in a STAR connection at the input GND terminal to ensure best performance.
40	GATE1	This pin is the output gate driver for the external N-channel power MOSFET.

40-Lead QFN Package Outline (K6)

6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch

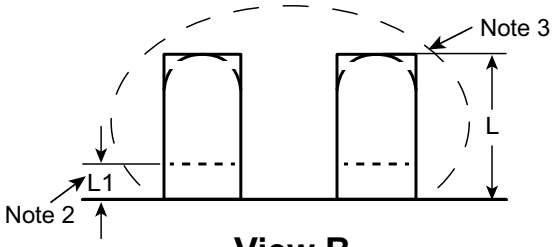


Top View



Bottom View

Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ°
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	5.85*	1.05	5.85*	1.05	0.50 BSC	0.30†	0.00	0
	NOM	0.90	0.02		0.25	6.00	-	6.00	-		0.40†	-	-
	MAX	1.00	0.05		0.30	6.15*	4.45	6.15*	4.45		0.50†	0.15	14

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc. #:** DSPD-40QFNK66X6P050, Version C041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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