19-3977; Rev 0; 1/06

EVALUATION KIT AVAILABLE

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

General Description

The MAX1366/MAX1368 low-power, 4.5- and 3.5-digit, panel meters feature an integrated sigma-delta analog-to-digital converter (ADC), LED display drivers, voltage digital-to-analog converter (DAC), and a 4–20mA (or 0 to 16mA) current driver.

The MAX1366/MAX1368's analog input voltage range is programmable to either ±2V or ±200mV. The MAX1368 drives a 3.5-digit (±1999 count) display and the MAX1366 drives a 4.5-digit (±19,999 count) display. The ADC output directly drives the LED display as well as the voltage DAC, which, in turn, drives the 4–20mA (or 0 to 16mA) current-loop output.

In normal operation, the 0 to 16mA/4–20mA current-loop output follows the ±2V or ±200mV analog input to drive remote panel-meter displays, data loggers, and other industrial controllers. For added flexibility, the MAX1366/MAX1368 allow direct access to the ADC result, DAC output, and the V/I converter input.

The sigma-delta ADC does not require external precision integrating capacitors, autozero capacitors, crystal oscillators, charge pumps, or other circuitry commonly required in dual-slope ADC panel-meter circuits. On-chip analog input and reference buffers allow direct interface with high-impedance signal sources. Excellent common-mode rejection and digital filtering provides greater than 100dB rejection of simultaneous 50Hz and 60Hz line noise. Other features include data hold and peak detection and overrange/underrange detection.

The MAX1366/MAX1368 require a 2.7V to 5.25V supply, a 4.75V to 5.25V V/I supply, and a 7V to 30V loop supply. They are available in a space-saving (7mm x 7mm), 48-pin TQFP package and operate over the extended (-40°C to +85°C) temperature range.

Applications

Industrial Process Control
Automated Test Equipment
Data-Acquisition Systems
Digital Panel Meters
Digital Voltmeters
Digital Multimeters

Pin Configuration appears at end of data sheet.

Typical Operating Circuits appear at end of data sheet.

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Features

- **Microcontroller (µC)-Interface, Digital Panel Meter**
  - **20-Bit Sigma-Delta ADC**
    - **4.5-Digit Resolution (±19,999 Count, MAX1366)**
    - **3.5-Digit Resolution (±1999 Count, MAX1368)**
  - **No Integrating/Autozeroing Capacitors**
  - **100MΩ Input Impedance**
  - **±200mV or ±2.000V Input Range**
- **LED Display**
  - **Common-Cathode 7-Segment LED Driver**
  - **Programmable LED Current (0 to 20mA)**
  - **2.5Hz Update Rate**
- **Output DAC and Current Driver**
  - **±15-Bit DAC with 14-Bit Linear V/I Converter**
  - **Selectable 0 to 16mA or 4–20mA Current Output**
  - **Unipolar/Bipolar Modes**
  - **±50µA Zero Scale, ±40ppmFS/°C (typ)**
  - **±0.5% Gain Error, ±25ppmFS/°C (typ)**
  - **Separate 7V to 30V Supply for Current-Loop Output**
- **2.7V to 5.25V ADC/DAC Supply**
- **4.75V to 5.25V V/I Converter Supply**
- **Internal 2.048V Reference or External Reference**
- **SPI™-/QSPI™-/MICROWIRE™-Compatible Serial Interface**
- **48-Pin, 7mm x 7mm TQFP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1366ECM	-40°C to +85°C	48 TQFP
MAX1368ECM	-40°C to +85°C	48 TQFP

Selector Guide

PART	PACKAGE CODE	RESOLUTION (DIGITS)
MAX1366ECM	C48-6	4.5
MAX1368ECM	C48-6	3.5

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ABSOLUTE MAXIMUM RATINGS

(With reference to GND, unless otherwise specified.)
AV_{DD}, DV_{DD} .....-0.3V to +6.0V
AIN+, AIN-, REF+, REF-.....V_{NEGV} to (AV_{DD} + 0.3V)
REG_FORCE, CMP, DAC_VDD, DACVOUT, CONV_IN, 4-20OUT.....-0.3V to (AV_{DD} + 0.3V)
EN_BPM, EN_I, REFSELE, DACDATA_SEL, CLK, $\overline{EOC}$, $\overline{CS\_DAC}$, SCLK, DIN DOUT.....-0.3V to (DV_{DD} + 0.3V)
NEGV .....-2.6V to (AV_{DD} + 0.3V)
LED_EN.....-0.3V to (DV_{DD} + 0.3V)
SET.....-0.3V to (AV_{DD} + 0.3V)
REG_AMP, REG_VDD .....-0.3V to +6.0V
LEDG .....-0.3V to +0.3V
GND_DAC .....-0.3V to +0.3V
GND_V/I.....-0.3V to +0.3V
SEG_ to LEDG.....-0.3V to (V_{LEDV} + 0.3V)
DIG_ to LEDG.....-0.3V to (V_{LEDV} + 0.3V)
LOWBATT .....-0.3V to (AV_{DD} + 0.3V)
REF_DAC .....-0.3V to (AV_{DD} + 0.3V)
DACVOUT .....-0.3V to (AV_{DD} + 0.3V)
DIG_ Sink Current 300mA
DIG_ Source Current.....50mA
SEG_ Sink Current 50mA
SEG_ Source Current.....50mA
Maximum Current Input into Any Other Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 22.7mW/°C above +70°C).....1818.2mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC ACCURACY						
Noise-Free Resolution		MAX1366	-19,999		+19,999	Counts
		MAX1368	-1999		+1999	
Integral Nonlinearity (Note 1)	INL	2.000V range		±1		Counts
		200mV range		±1		
Range-Change Ratio		(V_{AIN+} - V_{AIN-} = 0.100V) on 200mV range; (V_{AIN+} - V_{AIN-} = 0.100V) on 2.0V range		10:1		Ratio
Rollover Error		V_{AIN+} - V_{AIN-} = full scale		±1		Counts
Output Noise				10		μV_{P-P}
Offset Error (Zero Input Reading)		V_{AIN+} - V_{AIN-} = 0 (Note 2)	-0		+0	Counts
Gain Error		(Note 3)	-0.5		+0.5	%FSR
Offset Drift (Zero Reading Drift)		V_{AIN+} - V_{AIN-} = 0 (Note 4)		0.1		µV/°C
Gain Drift				±1		ppm/°C
INPUT CONVERSION RATE						
External Clock Frequency				4.9152		MHz
External Clock Duty Cycle			40		60	%
Update Rate		Internal clock		5		Hz
		External clock, f_{CLK} = 4.9152MHz		5		
ANALOG INPUTS (AIN+, AIN-) (bypass to GND with 0.1µF or greater capacitors)						
AIN Input Voltage Range (Note 5)		RANGE bit = 0	-2.0		+2.0	V
		RANGE bit = 1	-0.2		+0.2	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN Absolute Input Voltage Range to GND			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		Internal clock mode, 50Hz and 60Hz ±2%		100		dB
		External clock mode, 50Hz and 60Hz ±2%, f_{CLK} = 4.9152MHz		100		
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA
LOW-BATTERY VOLTAGE MONITOR (LOWBATT)						
LOWBATT Trip Threshold				2.048		V
LOWBATT Leakage Current				10		pA
Hysteresis				20		mV
INTERNAL REFERENCE (REF- = GND, INTREF = DV_{DD})						
REF Input Voltage	V_{REF}	AV_{DD} = 5V	2.007	2.048	2.089	V
REF Output Short-Circuit Current				1		mA
REF Output Temperature Coefficient	TC_{VREF}			40		ppm/°C
Load Regulation		I_{SOURCE} = 0 to 300µA, I_{SINK} = 0 to 30µA		6		µV/µA
Line Regulation				50		µV/V
Noise Voltage		0.1Hz to 10Hz		25		$µV_{P-P}$
		10Hz to 10kHz		400		
EXTERNAL REFERENCE (INTREF BIT = 0)						
REF Input Voltage		Differential, (V_{REF+} - V_{REF-})		2.048		V
Absolute REF+, REF- Input Voltage to GND (V_{REF+} must be greater than V_{REF-})			-2.2		+2.2	V
Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)		Internal clock mode, 50Hz and 60Hz ±2%		100		dB
		External clock mode, 50Hz and 60Hz ±2%, f_{CLK} = 4.9152MHz		120		
Common-Mode 50Hz and 60Hz Rejection (Simultaneously)	CMR	For 50Hz and 60Hz ±2%, R_{SOURCE} < 10kΩ		150		dB
Common-Mode Rejection	CMR	At DC		100		dB
Input Leakage Current				10		nA

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance				10		pF
Average Dynamic Input Current		(Note 6)	-20		+20	nA
CHARGE PUMP						
Output Voltage	NEGV	C_{NEGV} = 0.1µF to GND	-2.60	-2.42	-2.30	V
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, CLK)						
Input Current	I_{IN}	V_{IN} = 0 or DV_{DD}	-10		+10	µA
Input Low Voltage	V_{INL}				0.3 x DV_{DD}	V
Input High Voltage	V_{INH}		0.7 x DV_{DD}			V
Input Hysteresis	V_{HYS}	DV_{DD} = 3V		200		mV
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	0.8 x D_{VDD}			V
Tri-State Leakage Current	I_L		-10		+10	µA
Tri-State Output Capacitance	C_{OUT}			15		pF
ADC POWER SUPPLY (Note 10)						
AV_{DD} Voltage	AV_{DD}		2.70		5.25	V
DV_{DD} Voltage	DV_{DD}		2.70		5.25	V
Power-Supply Rejection AV_{DD}	PSR_A	(Note 7)		80		dB
Power-Supply Rejection DV_{DD}	PSR_D	(Note 7)		100		dB
AV_{DD} Current (Notes 8, 9)	I_{AVDD}				640	µA
		Standby mode			305	
DV_{DD} Current (Notes 8, 9)	I_{DVDD}	DV_{DD} = +5.25V			320	µA
		DV_{DD} = +3.3V			180	
		Standby mode			20	
DAC POWER SUPPLY						
DAC Supply Voltage	V_{DAC_VDD}		2.70		5.25	V
DAC Supply Current				0.10	0.21	mA
LINEAR REGULATOR AND V/I CONVERTER POWER REQUIREMENTS						
REG_AMP Supply Voltage	V_{REG_AMP}		4.75		5.25	V
REG_AMP Supply Current				0.19	0.30	mA
REG_VDD Voltage	V_{REG_VDD}			5.20		V

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REG_VDD Supply Current		Includes 20mA programmed current		25.2	27.4	mA
LED DRIVERS (Table 7)						
LED Supply Voltage	V_{LEDV}		2.70		5.25	V
LED Shutdown Supply Current	I_{SHDN}				10	µA
LED Supply Current	I_{LEDV}	Seven segments and decimal point on, R_{SET} = 25kΩ		176	180	mA
Display Scan Rate	f_{OSC}	MAX1366		512		Hz
		MAX1368		640		
Segment Current Slew Rate	$I_{SEG}/\Delta t$			25		mA/µs
DIG_ Voltage Low	V_{DIG}	$I_{DIG\_}$ = 176mA		0.178	0.300	V
Segment-Drive Source-Current Matching	ΔI_{SEG}			3	±10	%
Segment-Drive Source Current	I_{SEG}	V_{LEDV} - V_{SEG} = 0.6V, R_{SET} = 25kΩ	15.0	21.5	25.5	mA
LED Drivers Bias Current		From AV_{DD}		120		µA
Interdigit Blanking Time				4		µs
4-20OUT OUTPUT ACCURACY						
Zero-Scale Error		4mA or 0mA, at +25°C		±10	±50	µA
Zero-Scale Error Tempco				±40		ppmFS/°C
Gain Error		4mA or 0mA, at +25°C		±0.2	±0.5	%FS
Gain-Error Tempco				±25		ppmFS/°C
Span Linearity				±2	±4	µA
Power-Supply Rejection	PSR	V_{EXT} = 7V to 36V		4		µA/V
Signal Path Noise		10pF to AGND on 4-20OUT		2.0		$µA_{RMS}$
4–20mA Current Limit		Limited to 12.5 x V_{REF} / 1.28kΩ		20		mA
TIMING CHARACTERISTICS (Notes 11, 12, Figure 8)						
SCLK Operating Frequency	f_{SCLK}	DV_{DD} = 2.7V	0		4.2	MHz
SCLK Pulse-Width High	t_{CH}		100			ns
SCLK Pulse-Width Low	t_{CL}		100			ns
DIN-to-SCLK Setup	t_{DS}		50			ns
DIN-to-SCLK Hold	t_{DH}		0			ns
$\overline{CS}$ Fall to SCLK Rise Setup	t_{CSS}		50			ns
SCLK Rise to $\overline{CS}$ Rise Hold	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 50pF, Figures 11, 12			120	ns

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = DAC_VDD = +2.7V to +5.25V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, V_{REG_AMP} = +5.0V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF. Internal clock mode, unless otherwise noted. All specifications are at T_A = T_{MIN} to T_{MAX}. Typical values are at T_A = +25°C, unless otherwise noted.)

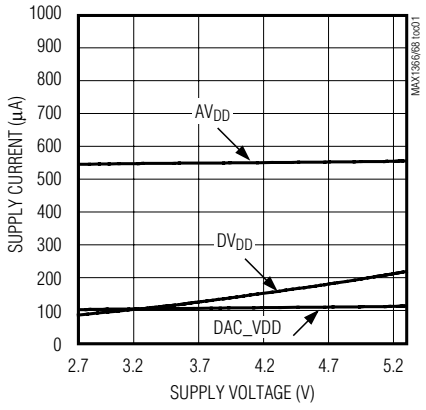
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_{LOAD} = 50pF, Figures 11, 12			120	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_{LOAD} = 50pF, Figures 11, 12			120	ns

Note 1: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after nulling the gain error and offset error.
Note 2: Offset calibrated. See OFFSET_CAL1 AND OFFSET_CAL2 in the *On-Chips Registers* section.
Note 3: Offset nulled.
Note 4: Offset-drift error is eliminated by recalibration at the new temperature.
Note 5: The input voltage range for the analog inputs is given with respect to the voltage on the negative input of the differential pair.
Note 6: V_{AIN+} or V_{AIN-} = -2.2V to +2.2V. V_{REF+} or V_{REF-} = -2.2V to +2.2V. All input structures are identical. Production tested on AIN+ and REF+ only. V_{REF+} must always be greater than V_{REF-}.
Note 7: Measured at DC by changing the power-supply voltage from 2.7V to 5.25V and measuring the effect on the conversion error with external reference. PSRR at 50Hz and 60Hz exceeds 120dB with filter notches at 50Hz and 60Hz (Figure 1).
Note 8: CLK and SCLK are disabled.
Note 9: LED drivers are disabled.
Note 10: Power-supply currents are measured with all digital inputs at either GND or DV_{DD} and with the device in internal clock mode.
Note 11: All input signals are specified with t_{RISE} = t_{FALL} = 5ns (10% to 90% of DV_{DD}) and are timed from a voltage level of 50% of DV_{DD}, unless otherwise noted.
Note 12: See the serial-interface timing diagrams (Figures 7–11).

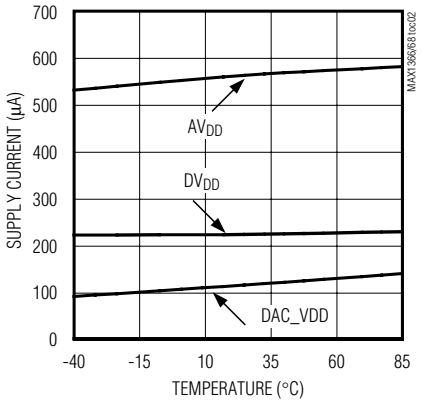
Typical Operating Characteristics

(A_{VDD} = D_{VDD} = +5V, V_{DAC_VDD} = +5.0V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF, RANGE bit = 1, internal clock mode. T_A = +25°C, unless otherwise noted.)

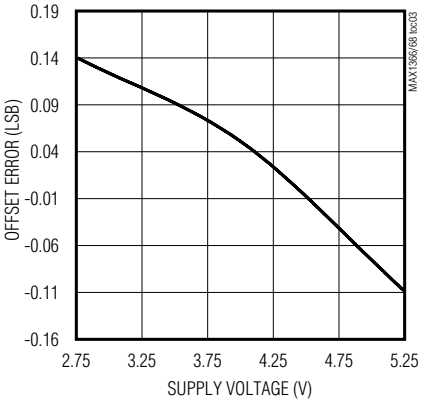
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



MAX1366 OFFSET ERROR vs. SUPPLY VOLTAGE

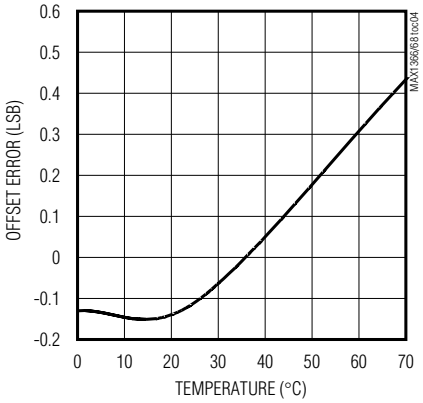


Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

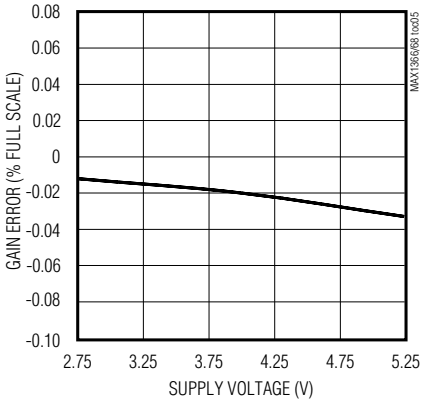
Typical Operating Characteristics

(A_{VDD} = D_{VDD} = +5V, V_{DAC_VDD} = +5.0V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF, RANGE bit = 1, internal clock mode. T_A = +25°C, unless otherwise noted.)

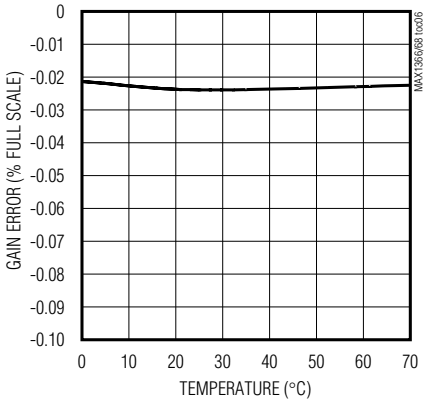
MAX1366
OFFSET ERROR vs. TEMPERATURE



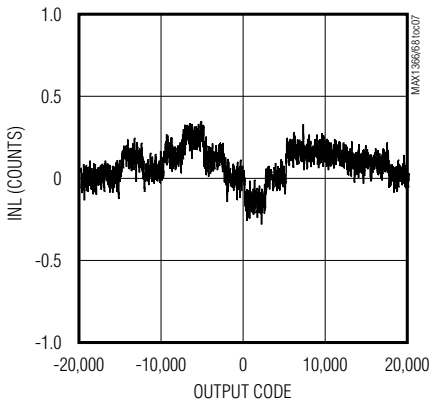
MAX1366
GAIN ERROR vs. SUPPLY VOLTAGE



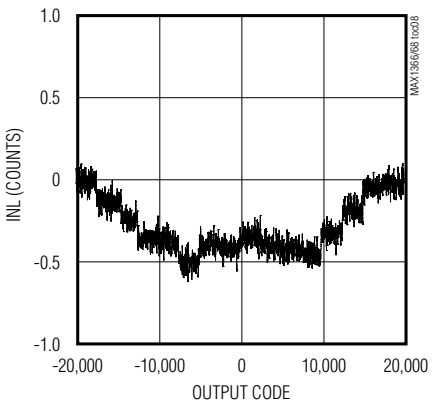
MAX1366
GAIN ERROR vs. TEMPERATURE



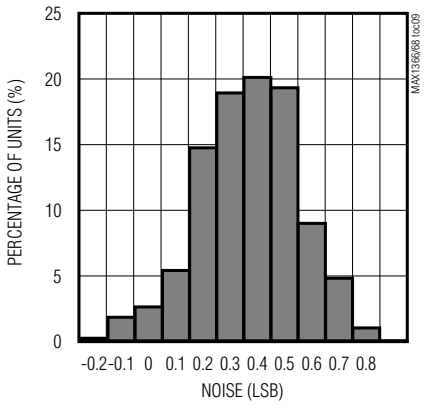
MAX1366
(±200mV INPUT RANGE) INL vs. OUTPUT CODE



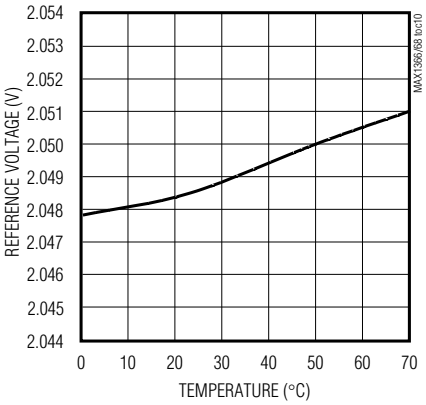
MAX1366
(±2V INPUT RANGE) INL vs. OUTPUT CODE



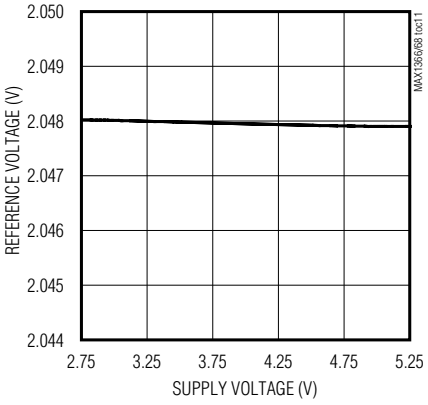
NOISE DISTRIBUTION



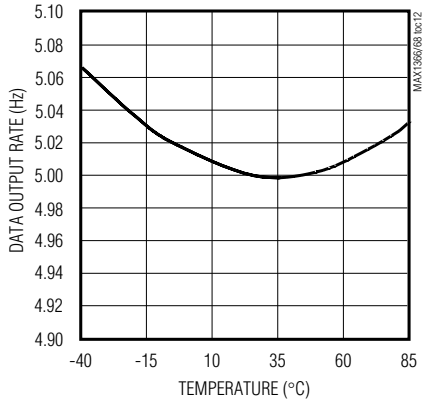
INTERNAL REFERENCE VOLTAGE
vs. TEMPERATURE



INTERNAL REFERENCE VOLTAGE
vs. ANALOG SUPPLY VOLTAGE



DATA OUTPUT RATE
vs. TEMPERATURE

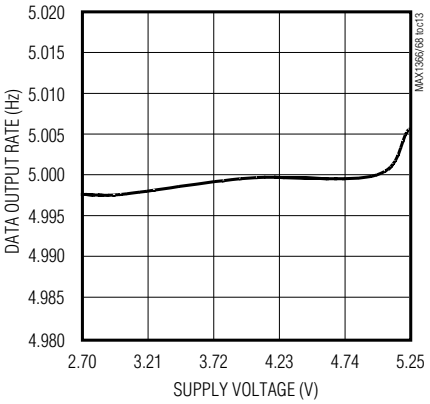


Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

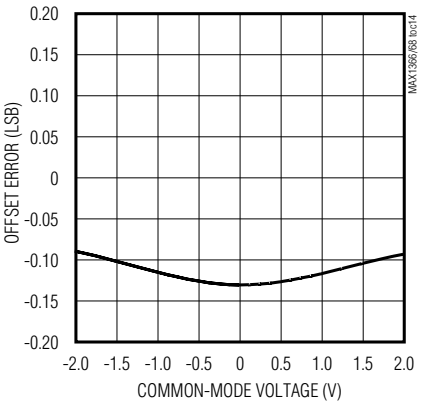
Typical Operating Characteristics

(A_{VDD} = D_{VDD} = +5V, V_{DAC_VDD} = +5.0V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF, RANGE bit = 1, internal clock mode. T_A = +25°C, unless otherwise noted.)

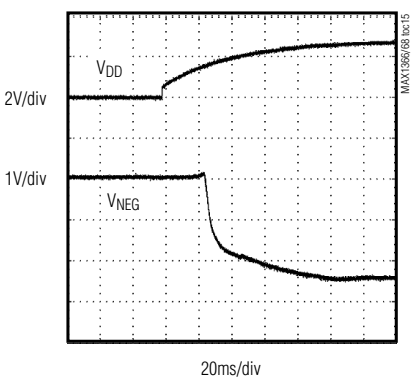
DATA OUTPUT RATE vs. SUPPLY VOLTAGE



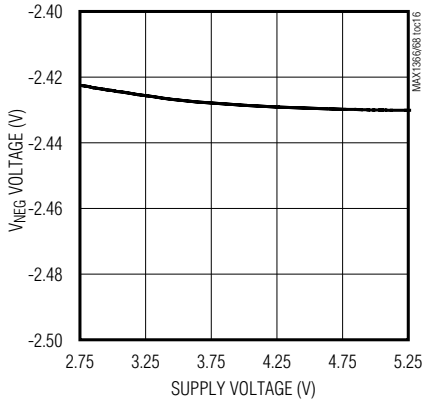
OFFSET ERROR vs. COMMON-MODE VOLTAGE



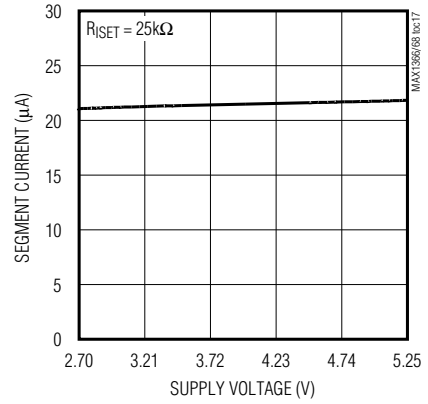
V_{NEG} STARTUP SCOPE SHOT



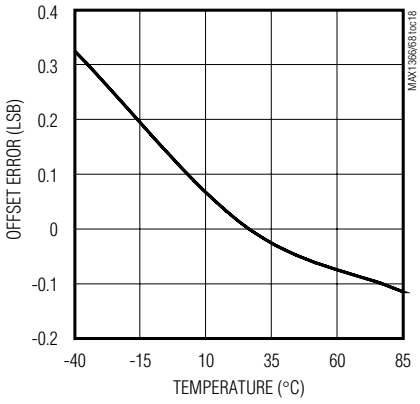
CHARGE-PUMP OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



SEGMENT CURRENT vs. SUPPLY VOLTAGE



DAC ZERO-CODE OFFSET ERROR vs. TEMPERATURE

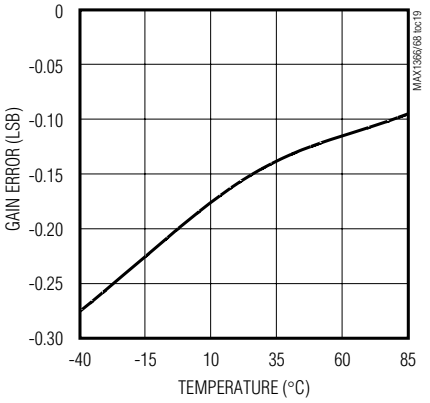


Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

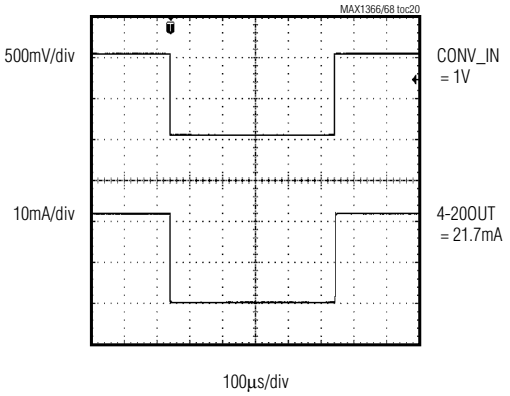
Typical Operating Characteristics (continued)

(A_{VDD} = D_{VDD} = +5V, V_{DAC_VDD} = +5.0V, GND = 0, LEDG = 0, V_{LEDV} = +2.7V to +5.25V, V_{REF+} - V_{REF-} = 2.048V (external reference), V_{EXT} = 7V, C_{REF+} = 0.1µF, REF- = GND, C_{NEGV} = 0.1µF, RANGE bit = 1, internal clock mode. T_A = +25°C, unless otherwise noted.)

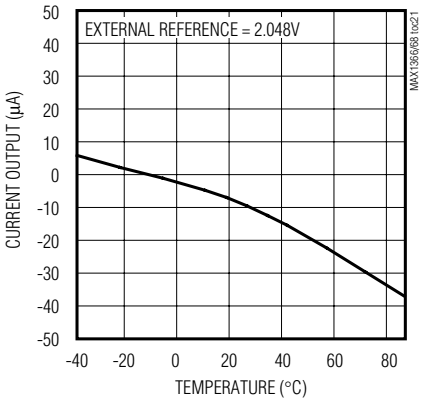
DAC GAIN ERROR vs. TEMPERATURE



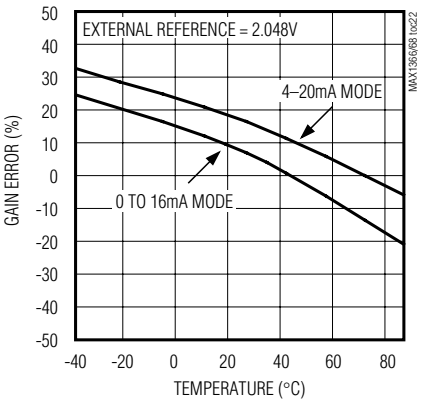
STEP RESPONSE



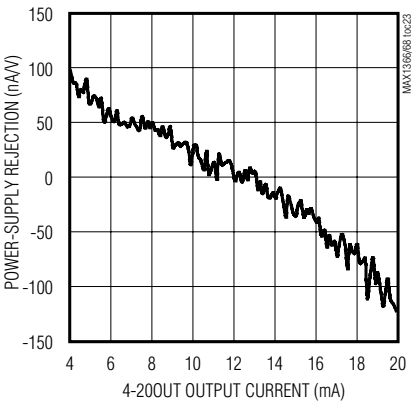
4-20OUT ZERO-SCALE ERROR vs. TEMPERATURE



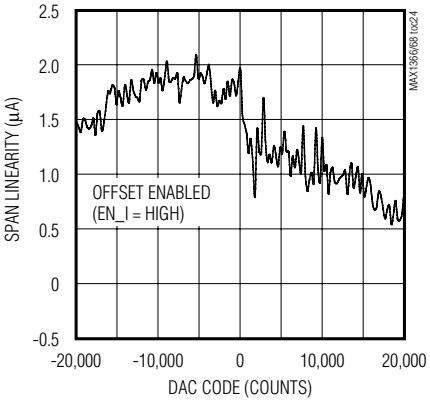
4-20OUT GAIN ERROR vs. TEMPERATURE



POWER-SUPPLY REJECTION vs. CURRENT OUTPUT (4-20OUT)



4-20OUT vs. DAC CODE (4-20OUT SPAN LINEARITY)



Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Pin Description

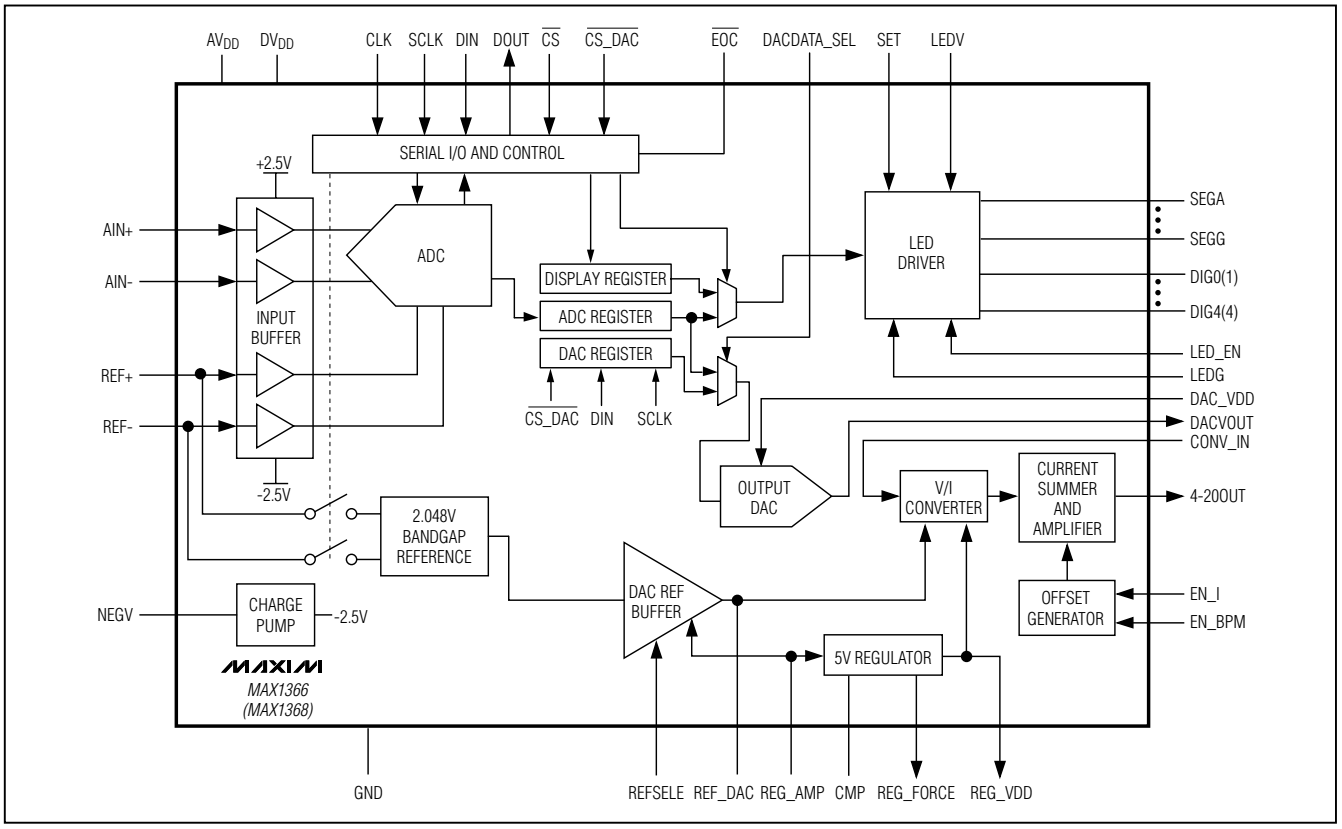
PIN	NAME	FUNCTION
1	AIN+	Positive Analog Input. Positive side of fully differential analog input. Bypass AIN+ to GND with a 0.1µF or greater capacitor.
2	AIN-	Negative Analog Input. Negative side of fully differential analog input. Bypass AIN- to GND with a 0.1µF or greater capacitor.
3	GND	Ground. Connect to star ground.
4	AV_{DD}	Analog Positive Supply Voltage. Connect AV_{DD} to a +2.7V to +5.25V power supply. Bypass AV_{DD} to GND with a 0.1µF capacitor.
5	DV_{DD}	Digital Positive Supply Voltage. Connect DV_{DD} to a +2.7V to +5.25V power supply. Bypass DV_{DD} to GND with a 0.1µF capacitor.
6	SET	Segment Current Set. Connect to ground through a resistor to set the segment current. See Table 7 for segment-current selection.
7	REG_VDD	V/I Converter Regulated Supply Output. REG_ VDD is typically 2.5V.
8	REG_FORCE	REG_VDD Control. Drives the gate of external depletion mode FET.
9	REG_AMP	Regulator/Reference Buffer Supply. Connect to a 4.75V to 5.25V power supply.
10	CMP	Regulator Compensation Node. Connect a 0.1µF capacitor from CMP to REG_FORCE.
11	DAC_VDD	DAC Analog Supply. Connect DAC_VDD to a +2.7V to +5.25V power supply.
12	DACVOUT	DAC Voltage Output. DAC output impedance is typically 6.2kΩ.
13	CONV_IN	V/I Converter Input
14	4–20OUT	4–20mA (0 to 16mA) Current-Loop Output. Referenced to GND.
15	GND_DAC	DAC Analog Ground. Connect to star ground.
16	GND_V/I	V/I Converter Analog Ground. Connect to star ground.
17	REF_DAC	V-to-I Converter/DAC Reference Input. Connect a voltage source for external reference operation or leave floating for internal reference. Bypass REF_DAC with a 0.1µF capacitor to GND for either internal or external reference operation.
18	EN_BPM	Active-High V/I-Converter Bipolar-Mode Enable. Set high for bipolar mode. Set low for unipolar mode.
19	EN_I	Active-High V/I-Converter 4mA Offset Enable. Set low for 0 to 16mA output. Set high for 4–20mA
20	REFSELE	DAC External Reference Selection. Set low for internal reference. Set high for external reference. Leave REF_DAC unconnected when REFSELE is low.
21	DACDATA_SEL	DAC Data-Source Select. Set high to select DAC register. Set low to have the DAC follow the ADC output.
22	$\overline{CS\_DAC}$	DAC SPI Chip Select. See Table 8.
23	CLK	External Clock Input. When the EXTCLK register bit is set to one, CLK is the master clock input for the modulator, filter, and DAC. When the EXTCLK register bit is reset to zero, the internal clock is used. The default power-on state is EXTCLK = 0 (internal clock mode). Connect CLK to GND or DV_{DD} when using internal clock.
24	$\overline{EOC}$	Active-Low End-of-Conversion Logic Output. A logic-low at $\overline{EOC}$ indicates that a new ADC result is available in the ADC result register.

Pin Description (continued)

PIN	NAME	FUNCTION
25	SCLK	Serial Clock Input. Apply an external clock to SCLK to facilitate communication through the serial bus. SCLK may idle high or low.
26	DOUT	Serial Data Output. DOUT presents serial data in response to register queries. Data shifts out on the falling edge of SCLK. DOUT goes high impedance when $\overline{CS}$ is high.
27	DIN	Serial Data Input. Data present at DIN is shifted into the internal registers in response to a rising edge at SCLK when CS is low.
28	$\overline{CS}$	Active-Low Chip-Select Input. Forcing $\overline{CS}$ low activates the serial interface. (See Table 8.)
29	LEDG	LED Segment-Drivers Ground
30	DIG0	Digit 0 Driver Out (Connected to GLED for the MAX1368)
31	DIG1	Digit 1 Driver Out
32	DIG2	Digit 2 Driver Out
33	DIG3	Digit 3 Driver Out
34	DIG4	Digit 4 Driver Out
35	SEGA	Segment A Driver
36	SEGB	Segment B Driver
37	LEDV	LED-Display Segment-Driver Supply. Connect to a +2.7V to +5.25V supply. Bypass with a 0.1µF capacitor to LEDG.
38	SEGC	Segment C Driver
39	SEGD	Segment D Driver
40	SEGE	Segment E Driver
41	SEGF	Segment F Driver
42	SEGG	Segment G Driver
43	SEGDP	Segment Decimal-Point Driver
44	LED_EN	Active-High LED Enable. The MAX1366/MAX1368 display driver turns off when LED_EN is low. The MAX1366/MAX1368 LED-display driver turns on when LED_EN is high.
45	NEGV	-2.5V Charge-Pump Voltage Output. Connect a 0.1µF capacitor to GND.
46	LOWBATT	Low-Battery-Voltage Monitor. When the LOWBATT input voltage is lower than 2.048V, the LOWBATT bit in the status register is set to one.
47	REF-	Negative Reference Voltage Input. For internal reference operation, connect REF- to GND. For external reference operation, bypass REF- to GND with a 0.1µF capacitor and set V_{REF-} from -2.2V to +2.2V ($V_{REF+} > V_{REF-}$).
48	REF+	Positive Reference Voltage Input. For internal reference operation, connect a 4.7µF capacitor from REF+ to GND. For external reference operation, bypass REF+ to GND with a 0.1µF capacitor and set V_{REF+} from -2.2V to +2.2V, provided that $V_{REF+} > V_{REF-}$.

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Functional Diagram



Detailed Description

The MAX1366/MAX1368 low-power, highly integrated ADCs with LED drivers convert a ±2V differential input voltage (one count is equal to 100µV for the MAX1366 and 1mV for the MAX1368) with a sigma-delta ADC and output the result to an LED display. An additional ±200mV input range (one count is equal to 10µV for the MAX1366 and 100µV for the MAX1368) is available to measure small signals with finer resolution.

In addition to displaying the results on an LED display, these devices feature a DAC and V-to-I converter for 4–20mA (or 0 to 16mA) current output that proportionally follows the ADC input. The MAX1366/MAX1368 use an external depletion-mode nMOS transistor to regulate 7V to 30V for the V/I converter. Use the 4–20mA (or 0 to 16mA) output to drive a remote display, data logger, PLC input, or other 4–20mA devices in a current loop.

The MAX1366/MAX1368 interface with a µC using an SPI-/QSPI-/MICROWIRE-compatible serial interface.

For added flexibility, the MAX1366/MAX1368 allow direct access to the ADC register, LED display register, and DAC output register using the SPI interface.

The MAX1366/MAX1368 include a 2.048V reference, internal charge pump, and a high-accuracy on-chip oscillator. The devices feature on-chip buffers for the differential input signal and external-reference inputs, allowing direct interface with high-impedance signal sources. In addition, they use continuous internal offset calibration and offer > 100dB of 50Hz and 60Hz line-noise rejection. Other features include data hold and peak detection and overrange/underrange detection.

Analog Input Protection

The MAX1366/MAX1368 provide internal protection diodes that limit the analog input range on AIN+, AIN-, REF+, and REF- from NEGV to (AV_{DD} + 0.3V). If the analog input exceeds this range, limit the input current to 10mA.

Internal Analog Input/Reference Buffers

The MAX1366/MAX1368 analog input/reference buffers allow the use of high-impedance signal sources. The input buffers' common-mode input range allows the analog inputs and the reference to range from -2.2V to +2.2V.

Modulator

The MAX1366/MAX1368 perform analog-to-digital conversions using a single-bit, 3rd-order, sigma-delta modulator. The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The modulator quantizes the input signal at a much higher sample rate than the bandwidth of the input. The MAX1366/MAX1368 modulator provides 3rd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise. A single-bit data stream is then presented to the digital filter to remove the frequency-shaped quantization noise.

Digital Filtering

The MAX1366/MAX1368 contain an on-chip digital low-pass filter that processes the data stream from the modulator using a $SINC^4$ response:

$$\left(\frac{\sin(x)}{x}\right)^4$$

The $SINC^4$ filter has a settling time of four output data periods (4 x 200ms). The MAX1366/MAX1368 have 25% overrange capability built into the modulator and digital filter. The digital filter is optimized for the f_{CLK} equal to 4.9152MHz. The frequency response of the $SINC^4$ filter is calculated as follows:

$$H(z)=\left[\frac{1(1-Z^{-N})}{N_{(1-Z^{-1})}}\right]^4$$

$$H(f)=\frac{1}{N}\left[\frac{\sin\left(N\pi\frac{f}{f_m}\right)}{\sin\left(\frac{\pi f}{f_m}\right)}\right]^4$$

where N is the oversampling ratio, and f_m = N x output data rate = 5Hz.

Filter Characteristics

Figure 1 shows the filter frequency response. The $SINC^4$ characteristic -3dB cutoff frequency is 0.228 times the first notch frequency (5Hz). The oversampling ratio (OSR) for the MAX1368 is 128 and the OSR for the MAX1366 is 1024. The output data rate for the digital filter corresponds to the positioning of the first notch of the filter's frequency response. The notches of the $SINC^4$ filter are repeated at multiples of the first notch frequency. The $SINC^4$ filter provides an attenuation of better than 100dB at these notches. For example, 50Hz is equal to 10 times the first notch frequency and 60Hz is equal to 12 times the first notch frequency. For large step changes at the input, allow a settling time of 800ms before valid data is read.

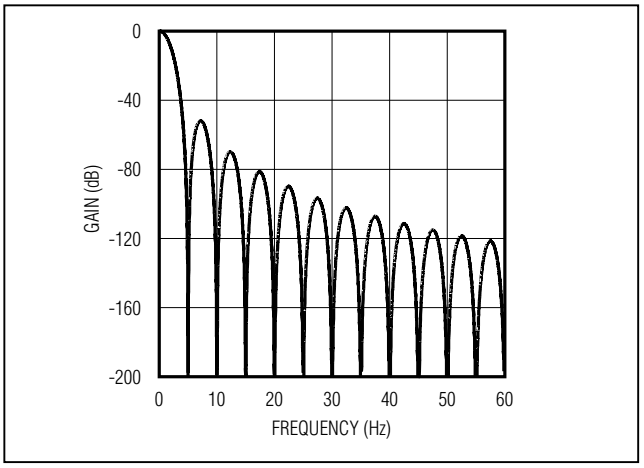


Figure 1. Frequency Response of the $SINC^4$ Filter (Notch at 60Hz)

Clock Modes

Configure the MAX1366/MAX1368 to use either the internal oscillator or an externally applied clock to drive the modulator, filter, and DAC. Set the EXTCLK bit in the control register to zero to put the device in internal clock mode. Set the EXTCLK bit to one to put the device in external clock mode. When using the internal oscillator, connect CLK to GND or DV_{DD}. The MAX1366/MAX1368 operate with a 4.9152MHz clock to achieve maximum rejection of 50Hz/60Hz common-mode, power-supply, and normal-mode noise.

Internal Clock Mode

The MAX1366/MAX1368 contain an internal oscillator. The power-up condition for the MAX1366/MAX1368 is internal clock operation with the EXTCLK bit in the control register equal to zero. Using the internal oscillator saves board space by removing the need for an external clock source.

External-Clock Mode

For external clock operation, set the EXTCLK bit in the control register to one and drive CLK with a 4.9152MHz

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

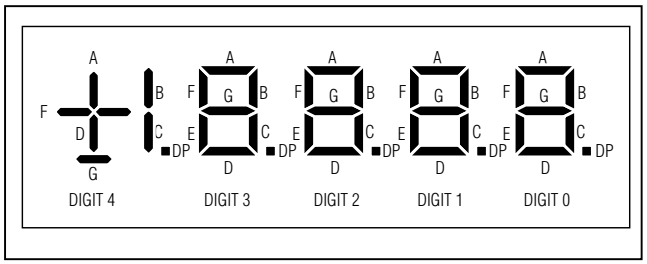


Figure 2. Segment Connection for the MAX1366 (4.5 Digits)

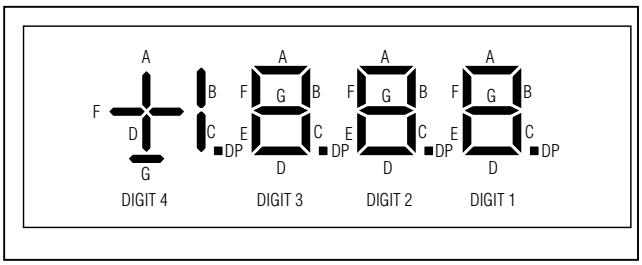


Figure 3. Segment Connection for the MAX1368 (3.5 Digits)

clock source for best 50Hz/60Hz rejection performance. Other external clock frequencies allow for custom conversion rates. A 2.4576MHz clock signal reduces the conversion rate and the LED update rate by a factor of two while keeping good 50Hz/60Hz noise rejection. The MAX1366/MAX1368 operate with an external clock source of up to 5.05MHz.

Charge Pump

The MAX1366/MAX1368 contain an internal charge pump to provide the negative supply voltage for the internal analog input/reference buffers. The bipolar input range of the analog input/reference buffers allows this device to accept negative inputs with high source impedances. Connect a 0.1µF capacitor from NEGV to GND.

LED Driver (Table 1)

The MAX1366 has a 4.5-digit common-cathode display driver, and the MAX1368 has a 3.5-digit common-cathode display driver.

Figures 2 and 3 show the connection schemes for a standard seven-segment LED display. The LED update rate is 2.5Hz.

The MAX1366/MAX1368 automatically display the results of the ADC, if desired. The MAX1366/MAX1368 also allow independent control of the LED driver through the serial interface, allowing for data processing of the ADC result before showing the result on the LED. Additionally, each LED segment can be individually controlled (see the *LED Segment-Display Register* sections).

Table 1. LED Priority Table

SEG_SEL	SPI/$\overline{ADC}$	HOLD	PEAK	DISPLAY VALUES FORM
1	X	X	X	LED segment registers
0	1	X	X	LED display register (user written)
0	0	1	X	LED display register
0	0	0	1	Peak register
0	0	0	0	ADC result register

X = Don't care.

Figure 4 shows a typical common-cathode configuration for two digits. In common-cathode configuration, the cathodes of all LEDs in a digit are connected together. Each segment driver of the MAX1366/MAX1368 connects to its corresponding LED's anodes. For example, segment driver SEGA connects to all LED segments designated as A. Similar configurations are used for other segment drivers.

The MAX1366/MAX1368 use a multiplexing scheme to drive one digit at a time. The scan rate is fast enough to make the digits appear to be lit. Figure 5 shows the data-timing diagram for the MAX1366/MAX1368 where t is the display scan period (typically around 1/512Hz or 1.9531ms). t_{ON} in Figure 5 denotes the amount of time each digit is on and is calculated as follows:

$$t_{ON} = \frac{t}{5} = \frac{1.95312ms}{5} = 390.60\mu s$$

Decimal-Point Control

The MAX1366/MAX1368 allow for full decimal-point control and feature leading-zero suppression.

Use the DPON, DPSET1, and DPSET2 bits in the control register to set the value of the decimal point (Tables 2 and 3). The MAX1366/MAX1368 overrange and underrange display is shown in Table 4.

Current Output

The MAX1366/MAX1368 feature a 4–20mA (0 to 16mA) current output for driving remote panel meters, data loggers, and process controllers in industrial applications. The DAC output is proportional to the input of the ADC and LED display. In the simplest configuration, connect DAC_VOUT directly to CONV_IN to have the current output (4–20mA or 0 to 16mA) follow the analog inputs.

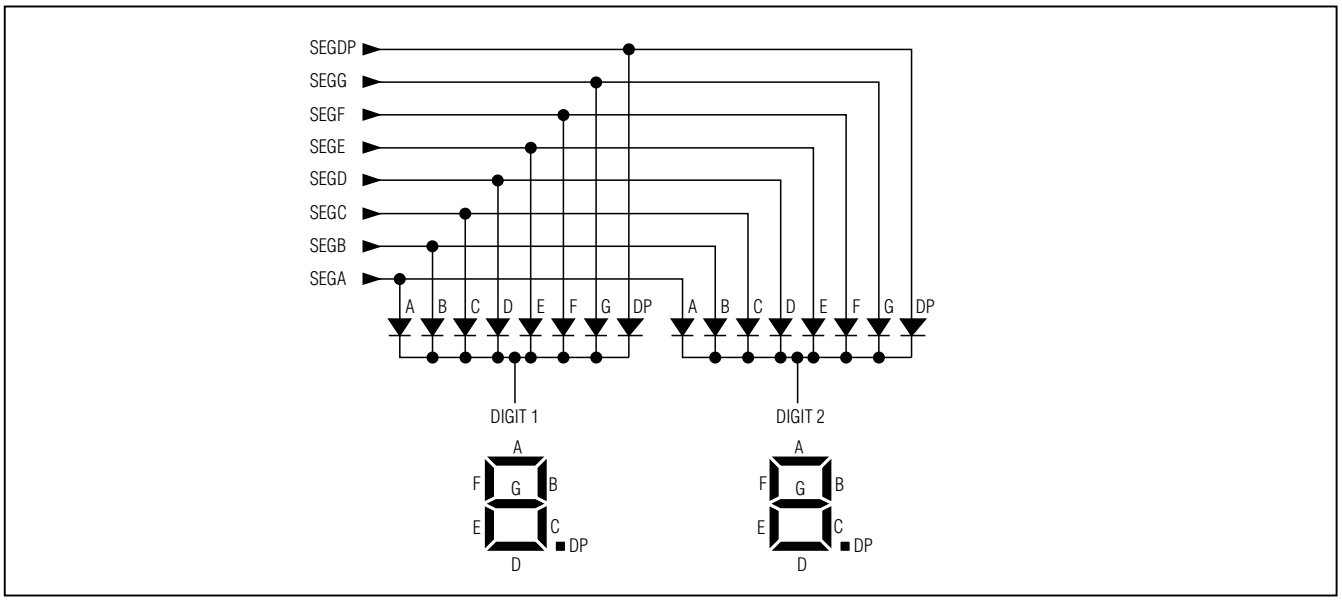


Figure 4. 2-Digit Common-Cathode Configuration

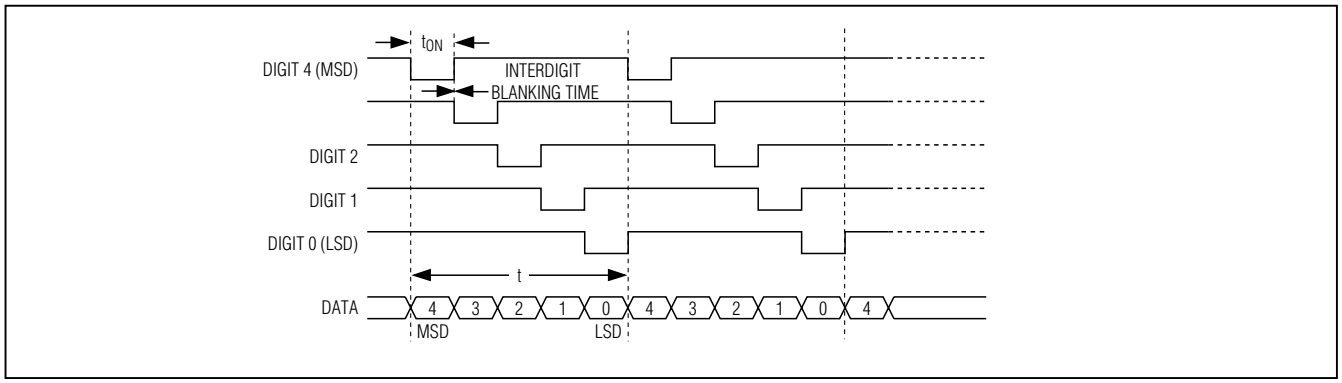


Figure 5. LED Voltage Waveform

Table 2. Decimal-Point Control Table—MAX1366

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
0	0	0	18888	0
0	0	1	18888	0
0	1	0	18888	0
0	1	1	18888	0
1	0	0	1888.8	0.0
1	0	1	188.88	0.00
1	1	0	18.888	0.000
1	1	1	1.8888	0.0000

Table 3. Decimal-Point Control Table—MAX1368

DPON	DPSET1	DPSET2	DISPLAY OUTPUT	ZERO INPUT READING
1	0	0	1888	0.
1	0	1	188.8	0.0
1	1	0	18.88	0.00
1	1	1	1.888	0.000

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

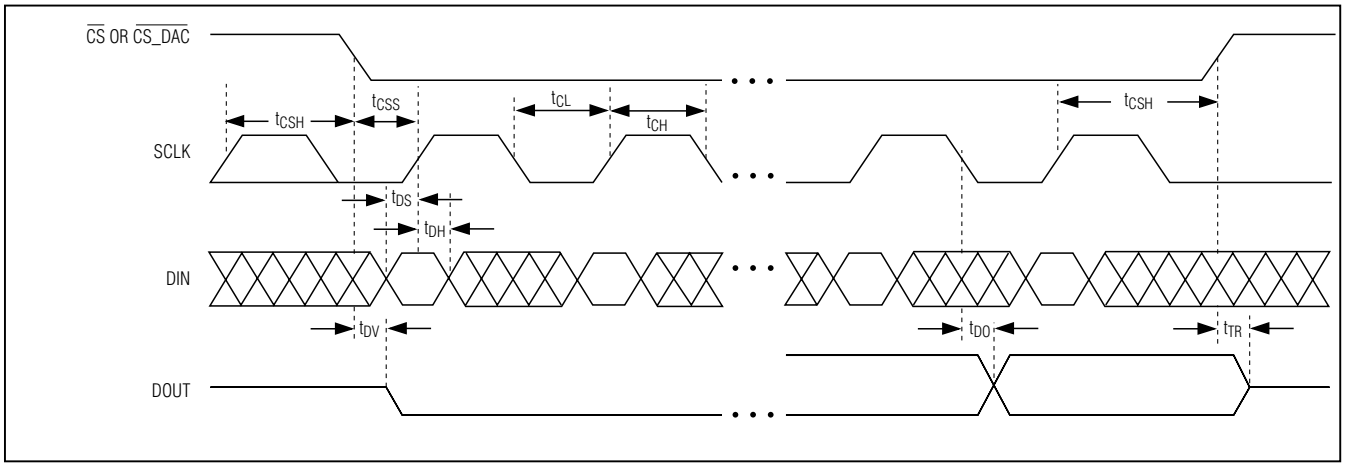


Figure 6. ADC and DAC Timing Diagram

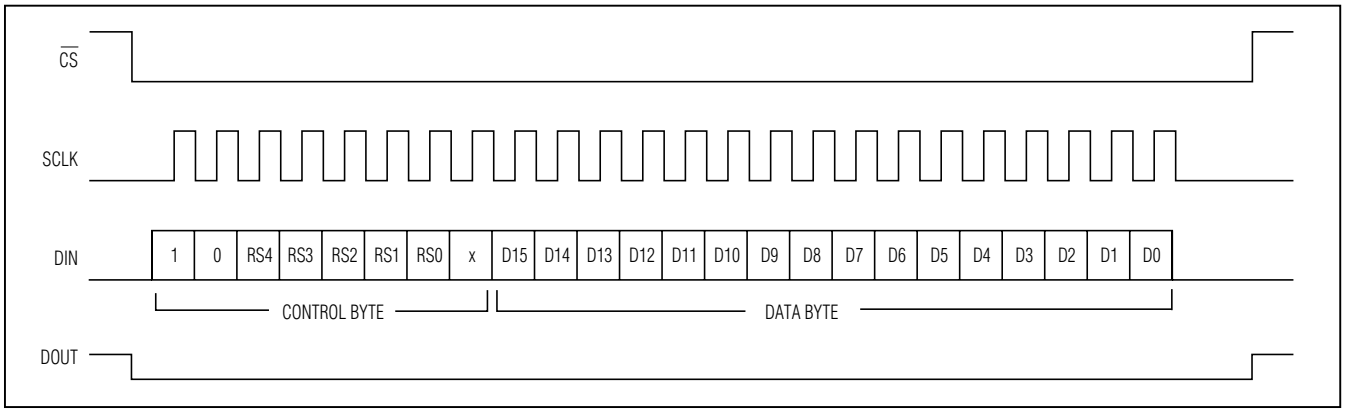


Figure 7. Serial-Interface, 16-Bit, Write Timing Diagram

Custom signal conditioning can be inserted between DAC_VOUT and CONV_IN, or CONV_IN can be driven independently by a voltage source if desired. See Figures 20–23 for the transfer functions of the DAC and V/I converter.

Note: The MAX1366/MAX1368 expect a 6kΩ (typ) source impedance from the voltage source driving CONV_IN.

Current Offset

Set EN_I high for a current span of 4–20mA. Set EN_I low for a current span of 0 to 16mA. See Table 5 for current output.

Unipolar Mode

Set EN_BPM low to engage unipolar operation. In unipolar mode, the current output at 4-20OUT (4–20mA or 0 to 16mA) maps the analog input voltage (0 to 2V or 0 to 200mV). Negative voltages at the analog input result in a 4mA or 0mA output, depending on the EN_I setting. See Table 5 for current output. See Figures 21 and 22.

Table 4. LED During Overrange and Underrange Conditions

CONDITION	MAX1368	MAX1366
Overrange	1---	1----
Underrange	-1---	-1----

Bipolar Mode

Set EN_BPM high to engage bipolar operation. In bipolar mode, the current output at 4-20OUT (4–20mA or 0 to 16mA) maps the analog input voltage (±2V or ±200mV). In bipolar mode, a 0V analog input maps to midscale (12mA). See Table 5 for current output. Also see Figures 21 and 22.

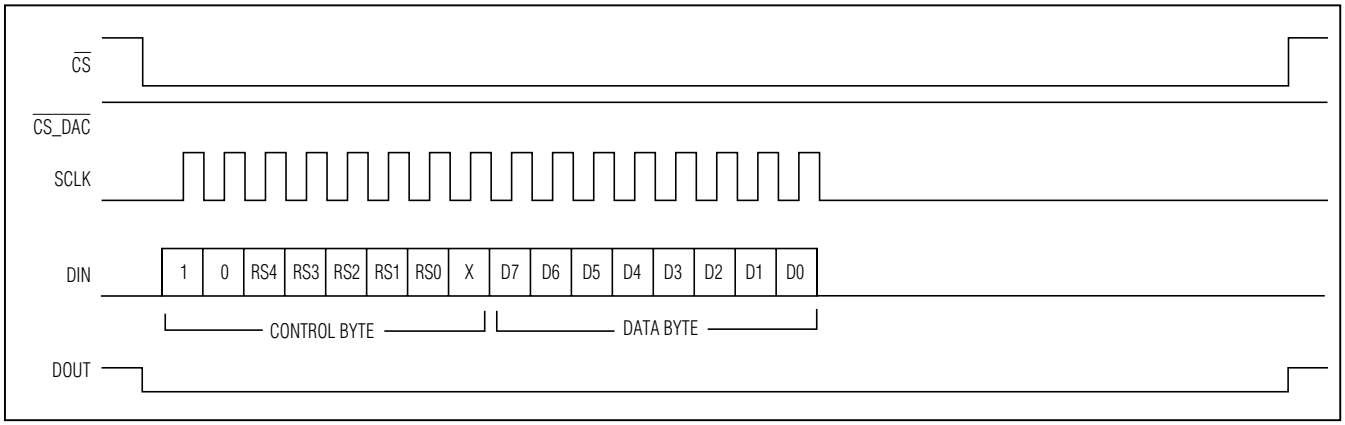


Figure 8. Serial-Interface, 8-Bit, Write Timing Diagram

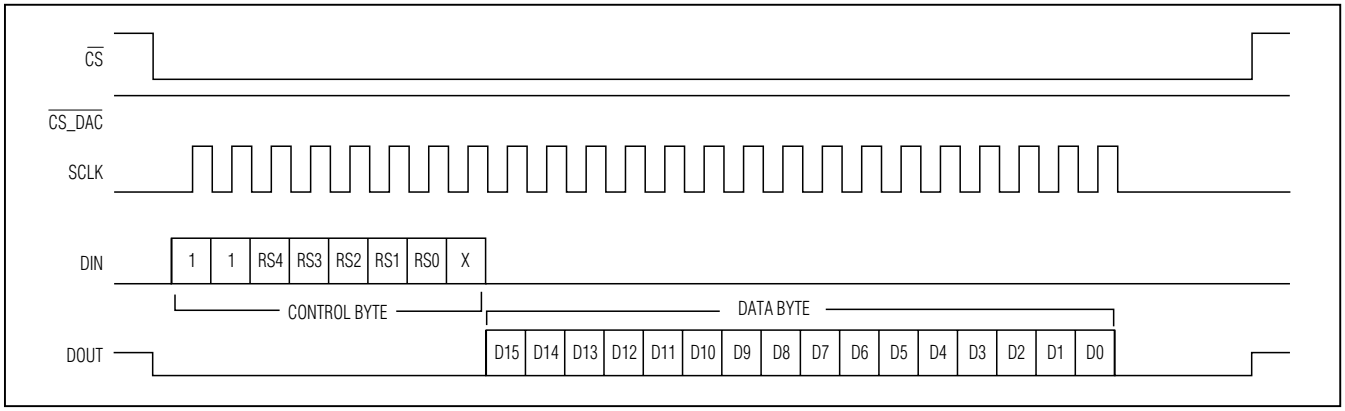


Figure 9. Serial-Interface, 16-Bit, Read Timing Diagram

Table 5. Current-Output Table

ANALOG INPUT	CURRENT OUTPUT (mA)			
	UNIPOLAR MODE (EN_I = LOW)	UNIPOLAR MODE (EN_I = HIGH)	BIPOLAR MODE (EN_I = LOW)	BIPOLAR MODE (EN_I = HIGH)
Negative Full Scale	0	4	0	4
0V	0	4	8	12
Positive Full Scale	16	20	16	20

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

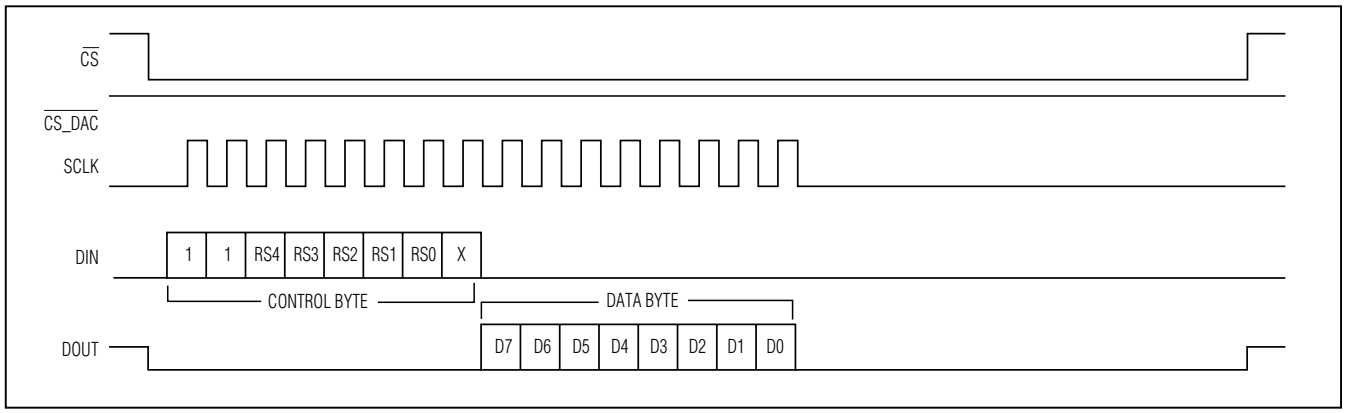


Figure 10. Serial-Interface, 8-Bit, Read Timing Diagram

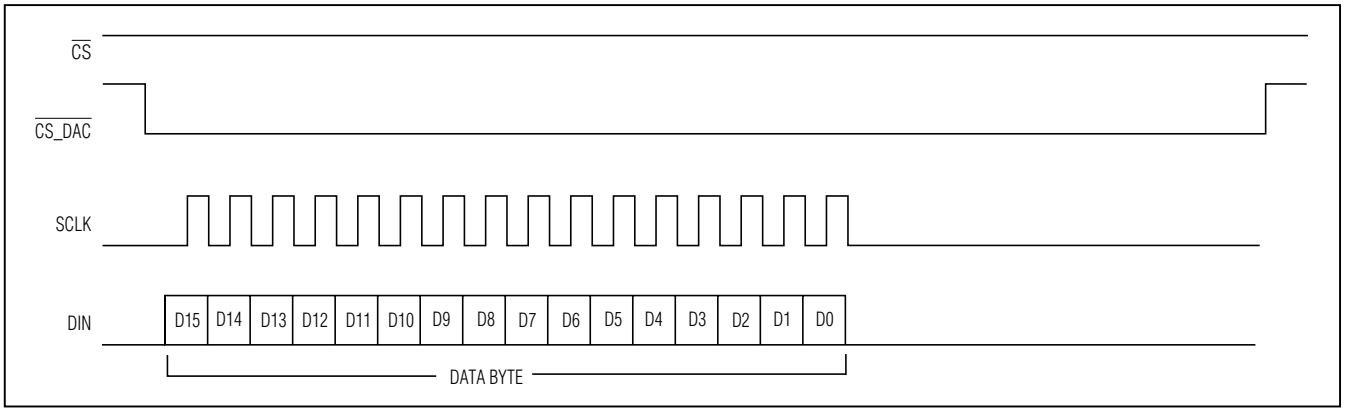


Figure 11. DAC Serial Interface

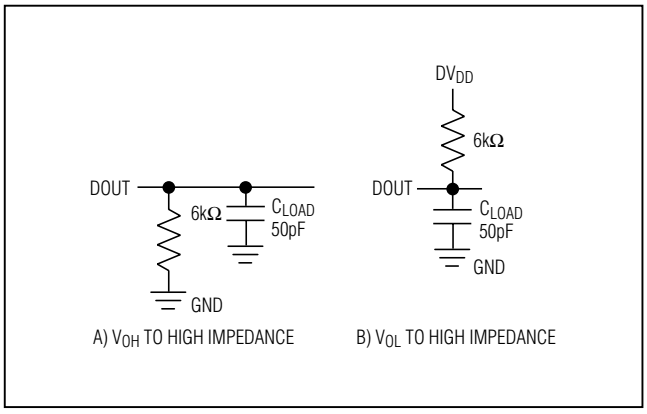


Figure 12. Load Circuits for Disable Time

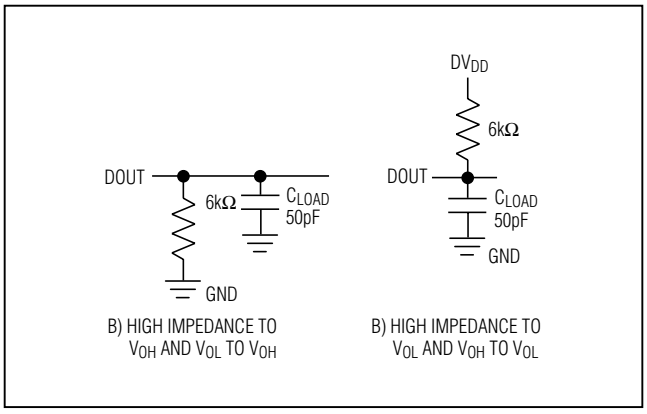


Figure 13. Load Circuits for Enable Time

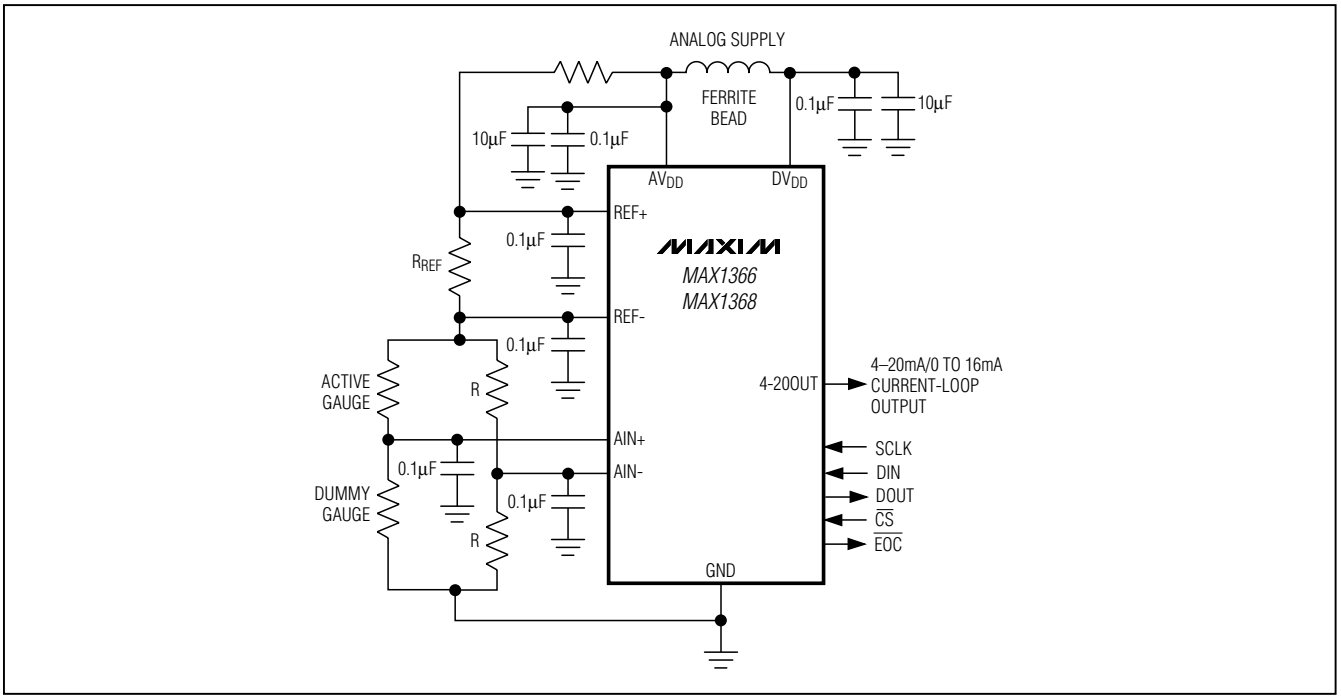


Figure 14. Strain-Gauge Application with the MAX1366/MAX1368

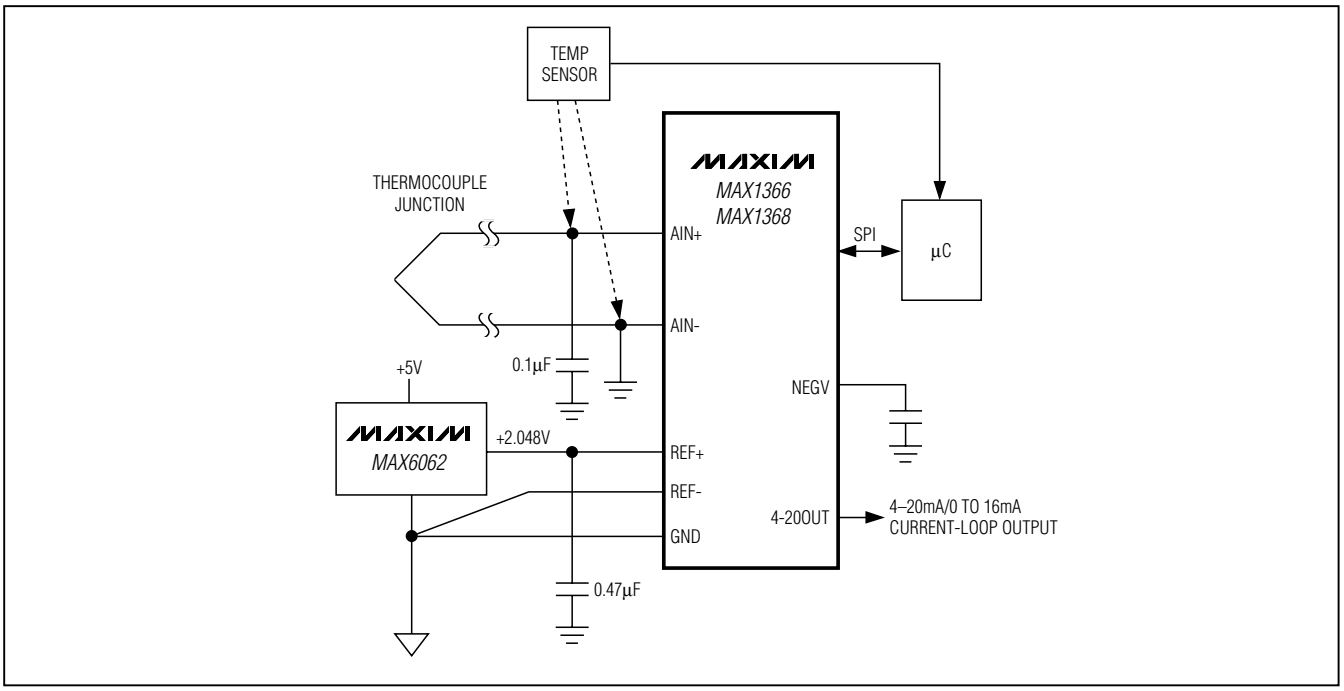


Figure 15. Thermocouple Application with the MAX1366/MAX1368

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

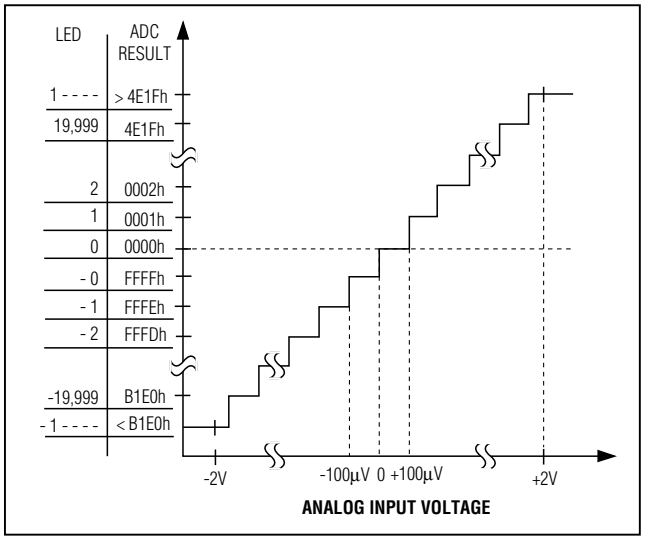


Figure 16. MAX1366 Transfer Function—±2V Range

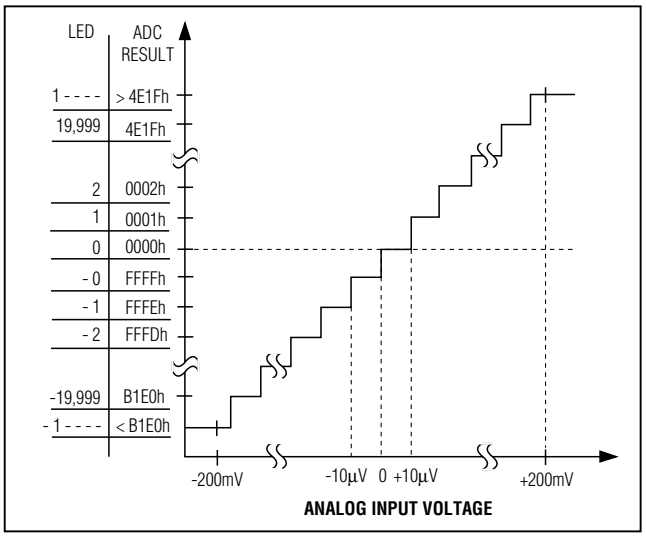


Figure 17. MAX1366 Transfer Function—±200mV Range

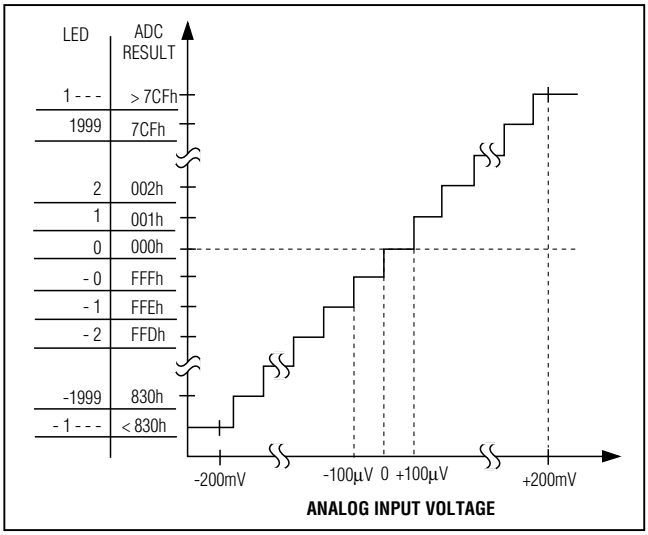


Figure 18. MAX1368 Transfer Function—±200mV Range

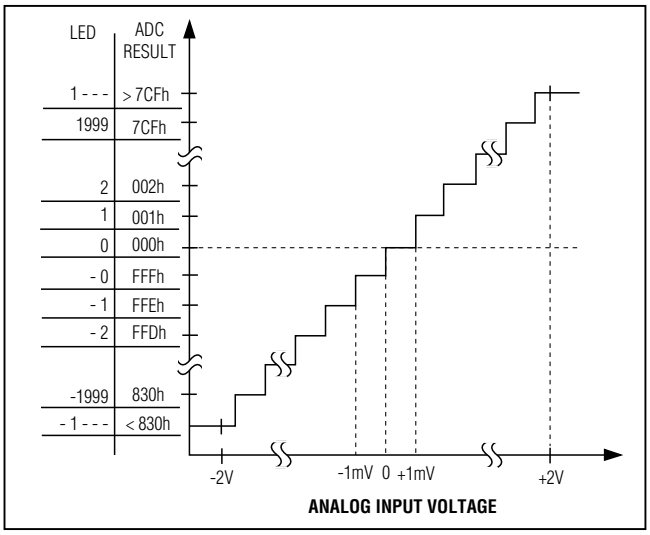


Figure 19. MAX1368 Transfer Function—±2V Range

5.2V Linear Regulator with Compensation

The MAX1366/MAX1368 feature a 5.2V linear regulator. The 5.2V regulator consists of an op amp and connections to an external depletion-mode FET. The 5.2V regulator regulates the loop voltage that powers the voltage-to-current converter and the rest of the transmitter circuitry. The regulator output voltage is available at REG_VDD and is given by the equation:

$$V_{REG\_VDD} = 2.54 \times V_{REF+}$$

The FET breakdown and saturation voltages determine the usable range of loop voltages (V_{EXT}). The external FET parameters such as V_{GS} (off), I_{DSS}, and transconductance must be chosen so that the op amp output on the REG_FORCE pin can control the FET operating point while swinging in the range from VREG_AMP to REG_VDD. See the *Selecting Depletion Mode FET* section in the *Applications Information* section.

Connect a 0.1µF capacitor between CMP and REG_FORCE to ensure stable operation of the regulator.

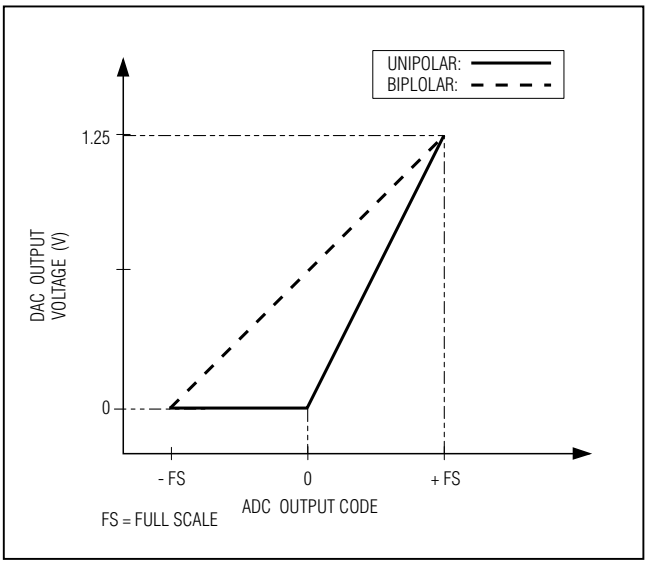


Figure 20. DAC Output Voltage vs. ADC Output Code

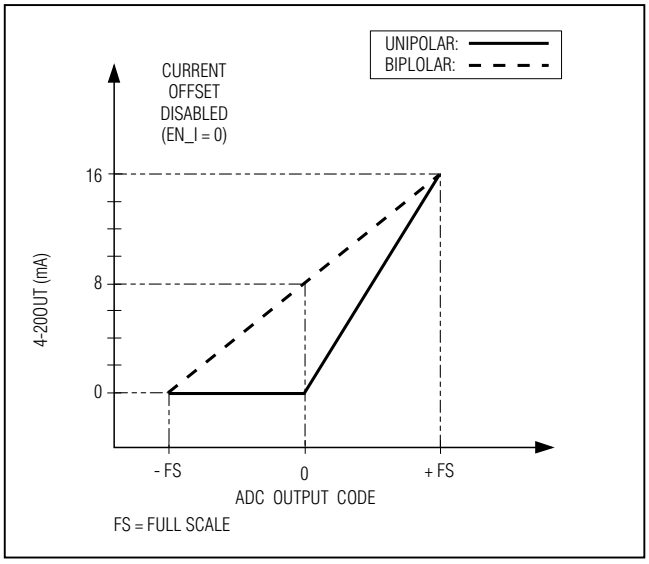


Figure 22. Output Current (4-20OUT) vs. ADC Output Code (Current Offset Disabled)

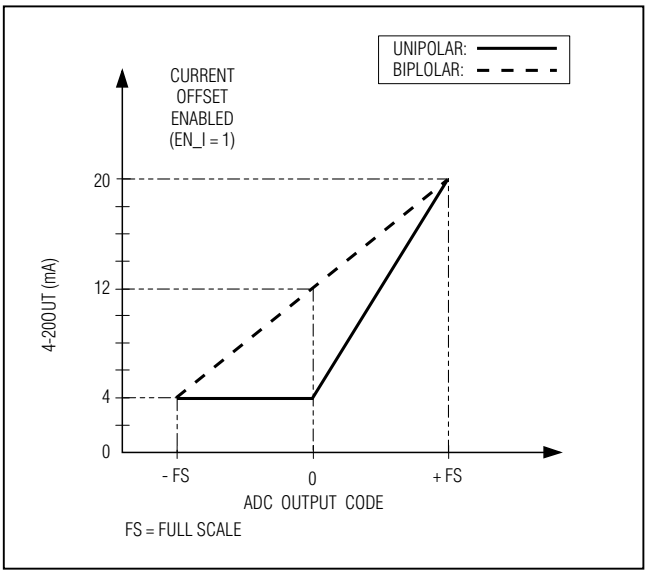


Figure 21. Output Current (4-20OUT) vs. ADC Output Code (Current Offset Enabled)

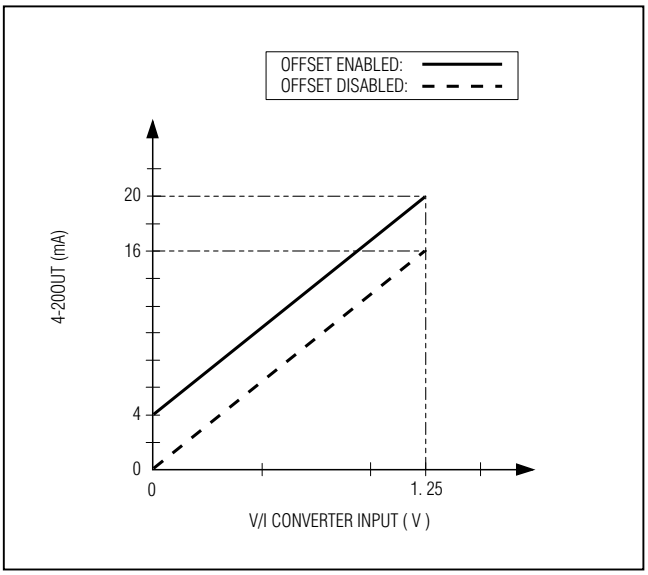


Figure 23. 4-20OUT Output Current vs. V/I Converter Input Voltage

Leading-Zero Suppression

The MAX1366/MAX1368 include a leading-zero suppression circuitry to turn off unnecessary zeros. For example, when DPSET1 and DPSET2 = [0,0], 0.0 is displayed instead of 000.0 (MAX1366). This feature saves a substantial amount of power by not lighting unnecessary LEDs.

Interdigit Blanking

The MAX1366/MAX1368 also include interdigit-blanking circuitry. Without this feature, it is possible to see a faint digit next to a digit that is completely on. The interdigit-blanking circuitry prevents ghosting over into the next digit for a short period of time. The typical interdigit blanking time is 4µs.

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Applications Information

Power-On Reset

At power-on, the serial interface, logic, LED drivers, digital filter, modulator, and DAC circuits reset. The registers return to their default values.

Serial Interface

The SPI/QSPI/MICROWIRE serial interface consists of a chip select ($\overline{CS}$), a serial clock (SCLK), a data in (DIN), a data out (DOUT), DAC chip select ($\overline{CS\_DAC}$), and an $\overline{EOC}$ output. $\overline{CS}$ and $\overline{CS\_DAC}$ enable access to registers in the MAX1366/MAX1368. $\overline{CS}$ allows a read and write to all registers of the MAX1366/MAX1368 excluding the DAC register and $\overline{CS\_DAC}$ enables a write to the DAC register (see Table 8). $\overline{EOC}$ provides an end-of-conversion signal with a period of 200ms (f_{CLK} = 4.9152MHz). The MAX1366/MAX1368 update the ADC register when $\overline{EOC}$ goes high. Data is valid in the ADC register when $\overline{EOC}$ returns low. The serial interface provides access to 13 on-chip registers, allowing control to all the power modes and functional blocks. Table 6 lists the address and read/write accessibility of all the registers excluding the DAC register.

A logic-high on $\overline{CS}$ and $\overline{CS\_DAC}$ tri-states DOUT and causes the MAX1366/MAX1368 to ignore any signals on SCLK and DIN. To clock data in or out of the internal shift register, drive $\overline{CS}$ or $\overline{CS\_DAC}$ low. SCLK synchronizes the data transfer. The rising edge of SCLK clocks DIN into the shift register, and the falling edge of SCLK clocks DOUT out of the shift register. DIN and DOUT are transferred MSB first (data is left justified). Figures 6–10 show the detailed serial-interface timing diagrams for the 8- and 16-bit read/write operations.

All communication with the MAX1366/MAX1368, with exception of the DAC register, begins with a command byte on DIN, where the first logic one on DIN is recognized as the START bit (MSB) for the command byte. The following seven clock cycles load the command into a shift register. These 7 bits specify which of the registers are accessed next, and whether a read or write operation takes place. Transitions on the serial clock after the command byte transfer, cause a write or read from the device until the correct number of bits have been transferred (8 or 16). Once this has occurred, the MAX1366/MAX1368 wait for the next command byte. $\overline{CS}$ must not go high between data transfers. If $\overline{CS}$ is toggled before the end of a write or read operation, the device mode may be unknown. Clock in 32 zeros to clear the device state and reset the interface so it is ready to receive a new command byte.

To write to the DAC register, pull $\overline{CS\_DAC}$ low and clock in 16 data bits. Data bits are clocked in MSB first (see the *DAC Operation* section).

On-Chip Registers (Excluding DAC Register)

The MAX1366/MAX1368 contain 12 on-chip registers. These registers configure the various functions of the device and allow independent reading of the ADC results and writing to the LED display. Table 6 lists the address and size of each register. The first of these registers is the status register. The 8-bit status register contains the status flags for the ADC. The second register is the 16-bit control register. This register sets the LED display controls, range modes, power-down modes, offset calibration, and the reset register function (CLR). The third register is the 16-bit overrange register, which sets the overrange limit of the analog input. The fourth register is the 16-bit underrange register, which sets the underrange limit of the analog input. Registers 5 through 7 contain the display data for the individual segments of the LED. The eighth register contains the custom offset value. The ninth register contains the 16 MSBs of the ADC conversion result. The 10th register contains the LED data. The 11th register contains the peak analog input value. The last register contains the lower 4 LSBs of the 20-bit ADC conversion result.

Table 6. Register-Address Table

REGISTER	ADDRESS RS[4:0]	NAME	WIDTH	ACCESS
1	00000	Status register	8	Read only
2	00001	Control register	16	R/$\overline{W}$
3	00010	Overrange register	16	R/$\overline{W}$
4	00011	Underrange register	16	R/$\overline{W}$
5	00100	LED segment-display register 1	16	R/$\overline{W}$
6	00101	LED segment-display register 2	16	R/$\overline{W}$
7	00110	LED segment-display register 3	8	R/$\overline{W}$
8	00111	ADC custom offset register	16	R/$\overline{W}$
9	01000	ADC result register (16 MSBs)	16	R/$\overline{W}$
10	01001	LED data register	16	R/$\overline{W}$
11	01010	Peak register	16	R/$\overline{W}$
12	10100	ADC result register 2 (4 LSBs)	8	R/$\overline{W}$
—	All other addresses	Reserved	—	—

Table 7. Segment-Current Selection

R_{ISET} (kΩ)	I_{SEG} (mA)
25	20
50	10
100	5
500	1
> 2500	LED driver disabled

Table 8. $\overline{CS}$ and $\overline{CS\_DAC}$ Table

DESCRIPTION	$\overline{CS}$	$\overline{CS\_DAC}$
Reserved.	0	0
Read or write to on-chip registers excluding the DAC register.	0	1
Write to the DAC register only.	1	0
DOUT is high impedance. DIN and SCLK are ignored.	1	1

Table 9. FET Characteristics

FET TYPE	n-CHANNEL DEPLETION MODE
I_{DS}	30mA
BV_{DS}	(V_{EXT}* - REG_VDD) min
$V_{PINCHOFF}$	REG_VDD max
Power dissipation	30mA x (V_{EXT} - REG_VDD) min

**V_{EXT} is the 7V to 30V loop voltage.*

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Control and Status Registers

Command Byte (Write Only)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
START(1)	R/$\overline{W}$	RS4	RS3	RS2	RS1	RS0	X

START: Start bit. The first 1 clocked into the MAX1366/MAX1368 is the first bit of the command byte.

(R/$\overline{W}$): Read/$\overline{Write}$. Set this bit to 1 to read from the specified register. Set this bit to zero to write to the selected register. Note that certain registers are read only. Write commands to a read-only register are ignored.

(RS4–RS0): Register address bits. RS4 to RS0 specify which register is accessed.

X: Don't care.

Status Register (Read Only)

MSB							LSB
SIGN	OVER	UNDER	LOW_BATT	DRDY	0	0	0

Default values: 00h

This register contains the status of the conversion results.

SIGN: Latched negative-polarity indicator. Latches high when the result is negative. Clears by reading the status register, unless the condition remains true.

OVER: Overrange bit. Latches high if an overrange condition occurs (the ADC result is larger than the value in the overrange register). Clears by reading the status register, unless the condition remains true.

UNDER: Underrange bit. Latches high if an underrange condition occurs (the ADC result is less than the value in the underrange register). Clears by reading the status register, unless the condition remains true.

LOW_BATT: Low-battery bit. Latches high if the voltage at the LOWBATT is lower than 2.048V (typ). Clears by reading the status register, unless the condition remains true.

DRDY: Data-ready bit. Latches high to indicate a completed conversion result with valid data. Read the ADC result register to clear this bit.

Control Register (Read/Write)

MSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SPI/$\overline{ADC}$	EXTCLK	INTREF	DPON	DPSET2	DPSET1	PD_DIG	PD_ANA
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HOLD	PEAK	RANGE	CLR	SEG_SEL	$\overline{OFFSET\_CAL1}$	OFFSET_ CAL2	ENABLE

Default values: 0000h

This register is the primary control register for the MAX1366/MAX1368. It is a 16-bit read/write register. It is used to indicate the desired clock and reference source. It sets the LED display controls, range modes, power-down modes, offset calibration, and the reset register function (CLR).

ENABLE: (Default = 1.) LED driver enable bit. When set to 1, the MAX1366/MAX1368 enables the LED display drivers. A 0 in this location disables the LED display drivers.

OFFSET_CAL2: (Default = 0.) Enhanced offset-calibration start bit (RANGE = 1). To achieve the lowest possible offset in the ±200mV input range, perform an enhanced offset calibration by setting this bit to 1. The calibration takes about nine cycles (1800ms). After the calibration completes, set this bit to zero to resume ADC conversions.

OFFSET_CAL1: (Default = 0.) Automatic offset-calibration enable bit. When set to 1, the MAX1366/MAX1368 disable automatic offset calibration. When this bit is set to zero, automatic offset calibration is enabled.

SEG_SEL: (Default = 0.) SEG_SEL segment selection bit. When set to 1, the LED segment drivers use the LED segment registers to display individual segments that can form letters or numbers or other information on the display. The LED data register is not displayed. Send the data first to the LED segment-display registers and then set this bit high.

CLR: (Default = 0.) Clear all registers bit. When set to 1, all registers reset to their power-on reset states after $\overline{CS}$ makes a low-to-high transition.

RANGE: (Default = 0.) Input range select bit. When set to zero, the input voltage range is ±2V. When set to 1, the input voltage range is ±200mV.

PEAK: (Default = 0.) Peak bit. When set to 1 (and the HOLD bit is set to zero), the LED shows the result stored in the peak register (see Table 6).

HOLD: (Default = 0.) Hold bit. When set to 1, the LED register does not update from the ADC conversion results and holds the last result on the LED. The MAX1366/MAX1368 continue to perform conversions during HOLD (Table 1).

PD_ANA: (Default = 0.) Power-down analog select bit. When set to 1, the analog circuits (analog modulator and ADC input buffers) go into the power-down mode. When set to zero, the device is in full power-up mode.

PD_DIG: (Default = 0.) Power-down digital select bit. When set to 1, the digital circuits (digital filter and LED drivers) go into power-down mode. This also resets the values of the internal SRAM in the digital filter to zeros. When set to zero, the device returns to full power-up mode. When powering down PD_DIG, power down the LED segment drivers by clearing the ENABLE bit to zero.

DPSET[2:1]: (Default = 00.) Decimal-point selection bits (Table 2 and 3).

DPON: (Default = 0.) Decimal-point enable bit (Tables 2 and 3).

INTREF: (Default = 0.) Reference select bit. For internal reference operation, set INTREF to 1. For external reference operation, set INTREF to zero.

EXTCLK: (Default = 0.) External clock select bit. The EXTCLK bit controls selection of the internal clock or an external clock source. A 1 in this location selects the signal at the CLK input as the clock source. A zero in this location selects and powers up the internal clock oscillator.

SPI/$\overline{ADC}$: (Default = 0.) Display select bit. The SPI/$\overline{ADC}$ bit controls selection of the data fed into LED data register. A 1 in this location selects SPI/QSPI/MICROWIRE data (user writes this data to the LED data register). A zero in this location selects the ADC result register data, unless hold or peak functions are active (Table 1).

Note: When changing any one of the following control bits: OFFSET_CAL1, RANGE, PD_ANA, PD_DIG, INTREF, and EXTCLK, wait 800ms before reading the ADC results.

Overrange Register (Read/Write)

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 7CF0h (for 3.5-digit, +1999)
4E1Fh (for 4.5-digit, +19,999)

The overrange register is a 16-bit read/write register (D15 is the MSB). When the conversion result exceeds the value in the overrange register, the OVER bit in the status register latches to 1. The LED shows a 1 followed by four dashes for the MAX1366 or a 1 followed by three dashes for the MAX1368 (Table 4).

The data is represented in two's-complement format.

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Underrange Register (Read/Write)

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 8300h (for 3.5-digit, -2000)

B1E0h (for 4.5-digit, -20,000)

The underrange data register is 16-bit read/write register (D15 is the MSB). When the conversion result falls below the value in the underrange register, the UNDR bit in the status register sets to 1. The LED shows a -1 followed by four dashes for the MAX1366 or a -1 followed by three dashes for the MAX1368 (Table 4).

The data is represented in two's-complement format.

Default values: 0000h

LED Segment-Display Register 1 (Read/Write)

MSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
$\overline{A1}$	$\overline{G1}$	$\overline{D1}$	$\overline{F1}$	$\overline{E1}$	$\overline{DP2}$	X	$\overline{B0}$
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{C0}$	$\overline{A0}$	$\overline{G0}$	$\overline{D0}$	$\overline{F0}$	$\overline{E0}$	$\overline{DP1}$	0

LED segment-display register 1 is a 16-bit read/write register. When the LED bit (in the control register) is set to 1, the MAX1366/MAX1368 provide direct access to individual LED segments. The bits in the LED segment-display register determine if a segment is on or off. Write a zero to turn on a segment and a 1 to turn off a segment.

$\overline{DP1}$: Segment DP driver bit of digit 1. The default value turns on the LED segment.

$\overline{E0}$: Segment E driver bit of digit 0. The default value turns on the LED segment.

$\overline{F0}$: Segment F driver bit of digit 0. The default value turns on the LED segment.

$\overline{D0}$: Segment D driver bit of digit 0. The default value turns on the LED segment.

$\overline{G0}$: Segment G driver bit of digit 0. The default value turns on the LED segment.

$\overline{A0}$: Segment A driver bit of digit 0. The default value turns on the LED segment.

$\overline{C0}$: Segment C driver bit of digit 0. The default value turns on the LED segment.

$\overline{B0}$: Segment B driver bit of digit 0. The default value turns on the LED segment.

X: Don't care.

$\overline{DP2}$: Segment DP driver bit of digit 2. The default value turns on the LED segment.

$\overline{E1}$: Segment E driver bit of digit 1. The default value turns on the LED segment.

$\overline{F1}$: Segment F driver bit of digit 1. The default value turns on the LED segment.

$\overline{D1}$: Segment D driver bit of digit 1. The default value turns on the LED segment.

$\overline{G1}$: Segment G driver bit of digit 1. The default value turns on the LED segment.

$\overline{A1}$: Segment A driver bit of digit 1. The default value turns on the LED segment.

LED Segment-Display Register 2 (Read/Write)

MSB							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
$\overline{F3}$	$\overline{E3}$	$\overline{DP4}$	$\overline{MINUS}$	$\overline{B2}$	$\overline{C2}$	$\overline{A2}$	$\overline{G2}$
							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{D2}$	$\overline{F2}$	$\overline{E2}$	$\overline{DP3}$	X	$\overline{B1}$	$\overline{C1}$	0

Default values: 0000h

LED segment-display register 2 is a 16-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1366/MAX1368 provide direct access to individual LED segments. The bits in the LED segment-display register determine if a segment is on or off. Write a zero to turn on a segment and a 1 to turn off a segment.

$\overline{C1}$: Segment C driver bit of digit 1. The default value turns on the LED segment.

$\overline{B1}$: Segment B driver bit of digit 1. The default value turns on the LED segment.

$\overline{MINUS}$: Segment minus driver bit. The default value turns on the LED minus segment. Setting this bit to 1 enables the plus sign on the LED display.

$\overline{DP3}$: Segment DP driver bit of digit 3. The default value turns on the LED segment.

$\overline{E2}$: Segment E driver bit of digit 2. The default value turns on the LED segment.

$\overline{F2}$: Segment F driver bit of digit 2. The default value turns on the LED segment.

$\overline{D2}$: Segment D driver bit of digit 2. The default value turns on the LED segment.

$\overline{G2}$: Segment G driver bit of digit 2. The default value turns on the LED segment.

$\overline{A2}$: Segment A driver bit of digit 2. The default value turns on the LED segment.

$\overline{C2}$: Segment C driver bit of digit 2. The default value turns on the LED segment.

$\overline{B2}$: Segment B driver bit of digit 2. The default value turns on the LED segment.

$\overline{DP4}$: Segment DP driver bit of digit 4. The default value turns on the LED segment (MAX1366 only).

$\overline{E3}$: Segment E driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

$\overline{F3}$: Segment F driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

LED Segment-Display Register 3 (Read/Write)

MSB							LSB
X	X	$\overline{BC\_}$	$\overline{B3}$	$\overline{C3}$	$\overline{A3}$	$\overline{G3}$	$\overline{D3}$

Default values: 00h

LED segment-display register 3 is an 8-bit read/write register. When the SEG_SEL bit (in the control register) is set to 1, the MAX1366/MAX1368 provide direct access to individual LED segments. The bits in the LED segment-display register determine if a segment is on or off. Write a zero to turn on a segment and a 1 to turn off a segment.

$\overline{D3}$: Segment D driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

$\overline{G3}$: Segment G driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

$\overline{A3}$: Segment A driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

$\overline{C3}$: Segment C driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

$\overline{B3}$: Segment B driver bit of digit 3. The default value turns on the LED segment (MAX1366 only).

$\overline{BC\_}$: Segment B and C driver bit of digit 3 (3.5 digits) or digit 4 (4.5 digits). The default value turns on the LED segment.

X: Don't care.

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ADC Custom Offset-Calibration Register 3 (Read/Write)

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

In addition to automatic offset calibration, the MAX1366/MAX1368 offer a user-defined custom offset 16-bit read/write register. The final result of the ADC conversion is the input after autocalibration minus the value in the custom offset. The custom offset value is stored in this register. D15 is the MSB. The data is represented in two's-complement format.

ADC Result Register 1 (Read Only)

MSB											LSB (MAX1368)				LSB (MAX1366)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

ADC result register 1 is a 16-bit read-only register. This register stores the 16 MSBs of the ADC result. The data is represented in two's-complement format.

For the MAX1366, the data is 16-bit and D15 is the MSB. For the MAX1368, the data is 12-bit, D15 is the MSB, and D4 is the LSB.

ADC Result Register 2 (Read Only)

MSB			LSB				
D3	D2	D1	D0	0	0	0	0

Default values: 00h

ADC result register 2 is an 8-bit read-only register. This register stores the 4 LSBs of the ADC result. Use this result with the result in ADC result register 1 to form a 20-bit two's-complement conversion result.

LED Data Register (Read/Write)

MSB											LSB (MAX1368)				LSB (MAX1366)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: 0000h

The LED data register is a 16-bit read/write register. This register updates from ADC result register 1 or from the serial interface by selecting the SPI/$\overline{\text{ADC}}$ bit in the control register. The data is represented in two's-complement format.

For the MAX1366, the data is 16-bit and D15 is the MSB. For the MAX1368, the data is 12-bit, D15 is the MSB, and D4 is the LSB, followed by 4 trailing sub-bits.

LED Data Register (Read/Write)

MSB										LSB (MAX1368)					LSB (MAX1366)
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Default values: B1E0h

The peak data register is a 16-bit read-only register. Set the PEAK bit to 1 to enable the PEAK function. This register stores the peak value of the ADC conversion result. First, the current ADC result is saved to the PEAK register, then the new ADC conversion result is compared to this value. If the new value is larger than the value in the peak register, the MAX1366/MAX1368 save the new value to the peak register. If the new value is less than the value in the peak register, the value in the peak register remains unchanged. Set the PEAK bit to zero to clear the value in the PEAK register.

The data is represented in two's-complement format.

For the MAX1366, the data is 16-bit and D15 is the MSB. For the MAX1368, the data is 12-bit, D15 is the MSB, and D4 is the LSB followed by 4 trailing sub-bits.

DAC Operation

For the MAX1366/MAX1368, a voltage proportional to the ADC input is available at DACVOUT. Connect DACVOUT to CONV_IN for normal operation. (See Figure 20 for DAC transfer function).

In normal operation, pull DACDATA_SEL low to use the ADC output as the DAC input. Pull DACDATA_SEL high to allow data to be written to the DAC register using the SPI/QSPI/MICROWIRE interface. Once DACDATA_SEL is pulled high, the three digital inputs ($\overline{CS\_DAC}$, DIN, and SCLK) load the digital input data serially into the DAC. (See Figure 11.)

To clock data into the DAC shift register, drive $\overline{CS\_DAC}$ low. SCLK synchronizes the data transfer. Immediately, following $\overline{CS\_DAC}$ high-to-low transition, the data shifts synchronously into the serial shift register on the rising edge of the serial clock input (SCLK). After 16 data bits have been loaded into the serial input register, the data latches to the DAC register on the rising edge of $\overline{CS\_DAC}$. The DAC output updates on the next conversion clock (2.5Hz). DIN is transferred MSB first.

Reference

ADC Reference

The MAX1366/MAX1368 reference sets the full-scale range of the ADC transfer function. With a nominal 2.048V reference, the ADC full-scale range is ±2V with RANGE = GND. With RANGE = DV_{DD}, the full-scale range is ±200mV. A decreased reference voltage decreases full-scale range (see the *Transfer Functions* section).

The MAX1366/MAX1368 accept either an external reference or an internal reference (INTREF). The INTREF logic selects the reference mode (see the *Control Register (Read/Write)* section). The default power-on state sets the MAX1366/MAX1368 to use the external reference with the INTREF bit cleared to zero.

For internal-reference operation, set the INTREF bit to one, connect REF- to GND, and bypass REF+ to GND with a 4.7µF capacitor. The internal reference provides a nominal 2.048V source between REF+ and GND. The internal-reference temperature coefficient is typically 40ppm/°C.

For external-reference operation, set INTREF to GND. REF+ and REF- are fully differential. For a valid external-reference input, V_{REF+} must be greater than V_{REF-}. Bypass REF+ and REF- with a 0.1µF or greater capacitor to GND in external-reference mode.

Figure 14 shows the MAX1366/MAX1368 operating with an external single-ended differential reference. In this figure, REF- is connected to the top of the strain gauge and REF+ is connected to the midpoint of the resistor-divider of the supply.

Figure 15 shows the MAX1366/MAX1368 operating with an external single-ended reference. In this figure, REF- is connected to GND and REF+ is driven with an external 2.048V reference. Bypass REF+ to GND with a 0.1µF capacitor.

DAC Reference

The DAC of the MAX1366/MAX1368 accepts either an external reference or an internal reference. For external-reference operation, disable the DAC reference buffer by setting REFSELE to DV_{DD} and connect a voltage source to REF_DAC.

For internal-reference operation, enable the DAC reference buffer by setting REFSELE to GND. In this mode, leave REFDAC floating.

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In either internal or external reference operation, bypass REF_DAC with a 0.1µF capacitor to GND. Choose a reference with output impedance (load regulation equivalent) of 100mΩ or less, such as the MAX6126. For best performance, use an external source from the ADC and DAC.

Offset Calibration

The MAX1366/MAX1368 offer on-chip offset calibration. The device offset calibrates during every conversion when the OFFSET_CAL1 bit is zero in the control register. Enhanced offset calibration is only needed in the MAX1366 when the RANGE bit = 1. It is performed on demand by setting the OFFSET_CAL2 bit to 1.

Enhanced Offset Calibration

Enhanced offset calibration is a more accurate calibration method that is needed in the case of the ±200mV range and 4.5-digit resolution. The MAX1366 performs enhanced calibration on demand by setting the OFFSET_CAL2 bit to 1.

Power-Down Modes

The MAX1366/MAX1368 feature independent power-down control of the analog and digital LED driver's circuitry.

Writing a 1 to the PD_DIG and PD_ANA bits in the control word, powers down the analog and digital circuitry, reducing the supply current to 268µA (typ). PD_DIG powers down the digital filter, while PD_ANA powers down the analog modulator and ADC input buffers. Writing a zero to the ENABLE bit in the control word powers down the LED drivers.

Peak

The MAX1366/MAX1368 feature peak-detection circuitry. When activated (PEAK bit = 1), the devices display only the highest voltage measured to the LED.

Hold

The MAX1366/MAX1368 feature data-hold circuitry. When activated (HOLD bit = 1), the device holds the current reading on the LED.

Low Battery

The MAX1366/MAX1368 feature a low-battery detection input. When the voltage at LOWBATT drops below 2.048V (typ), LOWBATT in the status register goes high.

Strain-Gauge Measurement

Connect the differential inputs of the MAX1366/MAX1368 to the bridge network of the strain gauge. In Figure 14, the analog supply voltage powers the bridge network and the MAX1366/MAX1368, along with the reference voltage. The MAX1366/MAX1368 handle an analog input voltage range of ±200mV and ±2V full scale. The analog/reference inputs of the parts allow the analog input range to have an absolute value of anywhere between -2.2V and +2.2V.

Thermocouple Measurement

Figure 15 shows a connection from a thermocouple to the MAX1366/MAX1368. In this application, the MAX1366/MAX1368 take advantage of the on-chip input buffers that allow large source impedances on the front end. The decoupling capacitors reduce noise pickup from the thermocouple leads. To place the differential voltage from the thermocouple at a suitable common-mode voltage, the AIN- input of the MAX1366/MAX1368 is biased to GND. Use an external temperature sensor, such as the DS75, and a microcontroller to perform cold-junction temperature compensation.

Transfer Functions

ADC Transfer Functions

Figures 16–19 show the transfer functions of the MAX1366/MAX1368. The output data is stored in the ADC data register in two's complement.

The transfer function for the MAX1366 with AIN+ - AIN- ≥ 0 and RANGE = GND is:

$$(1)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right)$$

The transfer function for the MAX1366 with AIN+ - AIN- < 0 and RANGE = GND is:

$$(2)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right)+1$$

The transfer function for the MAX1368 with AIN+ - AIN- ≥ 0 and RANGE = GND is:

$$(3)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right)$$

The transfer function for the MAX1368 with AIN+ - AIN- < 0 and RANGE = GND is:

$$(4)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right)+1$$

The transfer function for the MAX1366 with AIN+ - AIN- ≥ 0 and RANGE = DV_{DD} is:

$$(5)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10$$

The transfer function for the MAX1366 with AIN+ - AIN- < 0 and RANGE = DV_{DD} is:

$$(6)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 20{,}000\right) \times 10 + 1$$

The transfer function for the MAX1368 with AIN+ - AIN- ≥ 0 and RANGE = DV_{DD} is:

$$(7)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10$$

The transfer function for the MAX1368 with AIN+ - AIN- < 0 and RANGE = DV_{DD} is:

$$(8)\quad COUNT = 1.024\left(\frac{V_{AIN+} - V_{AIN-}}{V_{REF+} - V_{REF-}} \times 2000\right) \times 10 + 1$$

DAC Transfer Functions

Figure 20 shows the DAC transfer function for the MAX1366/MAX1368 in unipolar and bipolar modes.

The transfer function for the DAC in the MAX1366/MAX1368 unipolar mode is:

Note: The input at V_{CONV_IN} expects a source impedence of typically 6kΩ when driving V_{CONV_IN} externally.

$$V_{DACVOUT} = \frac{N}{32{,}768 - 1} \times V_{REF}$$

where N = two's complement ADC output code.

In unipolar mode, $V_{DACVOUT}$ is equal to 0V for all two's complement ADC codes less than zero (see Figure 21).

The transfer function for the DAC in the MAX1366/MAX1368 in bipolar mode is:

$$V_{DACVOUT} = \frac{N + 19{,}999}{6536} \times V_{REF}$$

where N = two's complement ADC output.

Writing into the DAC Independently

A user can independently write to the DAC but cannot input codes greater than +19,999 or less than -19,999. In bipolar mode, a -19,999 DAC code provides 4mA (0mA) output current and a +19,999 DAC code provides a 20mA (16mA) output current.

Voltage-to-Current Transfer Function

Figures 20 and 21 show the MAX1366/MAX1368 transfer function of the output current (4-20OUT) versus the ADC output code.

Figure 23 shows the MAX1366/MAX1368 transfer function of the output current (4-20OUT) versus the input voltage of the V/I converter.

The transfer function for the MAX1366/MAX1368 with the current offset enabled (EN_I is high) is:

$$IOUT \cong \frac{16mA}{1.25} \times V_{CONV\_IN} + 4mA$$

The transfer function for the MAX1366/MAX1368 with the current offset disabled (EN_I is low) is:

$$IOUT \cong \frac{16mA}{1.25} \times V_{CONV\_IN}$$

Supplies, Layout, and Bypassing

Power up AV_{DD} and DV_{DD} before applying an analog input and external-reference voltage to the device. If this is not possible, limit the current into these inputs to 50mA. When the analog and digital supplies come from the same source, isolate the digital supply from the analog supply with a low-value resistor (10Ω) or ferrite bead. For best performance, ground the MAX1366/MAX1368 to the analog ground plane of the circuit board. Avoid running digital lines under the device as this can couple noise onto the IC. Run the analog ground plane under the MAX1366/MAX1368 to minimize coupling of digital noise. Make the power-supply lines to the MAX1366/MAX1368 as wide as possible to provide low-impedance paths and reduce the effects of glitches on the power-supply line. Shield fast-switching signals, such as clocks, with digital ground to avoid radiating noise to other sections of the board. Avoid running clock signals near the analog inputs. Avoid crossover of digital and analog signals. Running traces that are on opposite sides of the board at right angles to each other reduces feedthrough effects. A microstrip technique is best, but is not always possible with double-sided boards. With this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side. Good decoupling is important when using high-resolution ADCs. Decouple the supplies with 0.1µF ceramic capacitors to GND. Place these components as close to the device as possible to achieve the best decoupling.

Selecting Segment Current

A resistor from ISET to ground sets the current for each LED segment. See Table 7 for more detail. Use the following formula to set the segment current:

$$I_{SEG} = \left(\frac{1.20V}{R_{ISET}}\right) \times 400$$

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R_{ISET} values below 25kΩ increase the I_{SEG}. However, the internal current-limit circuit limits the I_{SEG} to less than 30mA. At higher I_{SEG} values, proper operation of the device is not guaranteed. In addition, the power dissipated may exceed the package power-dissipation limit.

Choosing Supply Voltage to Minimize Power Dissipation

The MAX1366/MAX1368 drive a peak current of 25.5mA into LEDs with a 2.2V forward-voltage drop when operated from a supply voltage of at least 3.0V. Therefore, the minimum voltage drop across the internal LED drivers is 0.8V (3.0V - 2.2V = 0.8V). The MAX1366/MAX1368 sink when the outputs are operating and the LED segment drivers are at full current (8 x 25.5mA = 204mA). For a 3.3V supply, the MAX1366/MAX1368 dissipate 224.4mW ((3.3V - 2.2V) x 204 = 224.4mW). If a higher supply voltage is used, the driver absorbs a higher voltage, and the driver's power dissipation increases accordingly. However, if the LEDs used have a higher forward-voltage drop than 2.2V, the supply voltage must be raised accordingly to ensure that the driver always has at least 0.8V headroom. For an LEDV supply voltage of 2.7V, the maximum LED forward voltage is 1.9V to ensure 0.8V driver headroom. The voltage drop across the drivers with a nominal +5V supply (5.0V - 2.2V = 2.8V) is almost three times the drop across the drivers with a nominal 3.3V supply (3.3V - 2.2V = 1.1V). Therefore, the driver's power dissipation increases three times. The power dissipation in the part causes the junction temperature to rise accordingly. In the high ambient temperature case, the total junction temperature may be very high (> +125°C). At higher junction temperatures, the ADC performance degrades. To ensure the dissipation limit for the MAX1366/MAX1368 is not exceeded and the ADC performance is not degraded; a diode can be inserted between the power supply and LEDV.

Selecting Depletion-Mode FET

An external depletion-mode FET (DMOS) works in conjunction with the regulator circuit to supply the V/I converter with loop power. REG_FORCE regulates the gate of the DMOS so that the drain voltage is 5.2V (typ) and allows the 4–20mA (0 to 16mA) loop to be directly powered from a 7V to 30V supply. DMOS I_{DS} consists of the current output at 4-20OUT, a 4mA offset current, and 1mA (typ) consumed by the V/I converter.

For offset-enabled mode (EN_I = 1):

$$I_{DS} = I_{4\text{-}20OUT} + 4mA + 1mA$$

For offset-disabled mode (EN_I = 0):

$$I_{DS} = I_{4\text{-}20OUT} + 1mA$$

where I_{DS} is the current in the DMOS.

Table 9 provides the FET characteristics for selecting an external DMOS transistor. The DN25D FET transistor from Supertex meets all the requirements of Table 7. Other suitable transistors include ND2020L and ND2410L from Siliconix.

Connect a 0.1µF capacitor between CMP and REG_FORCE to ensure stable regulator compensation.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. This straight line is either a best-straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. INL for the MAX1366/MAX1368 is measured using the end-point method.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of ±1 LSB. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Rollover Error

Rollover error is defined as the absolute-value difference between a near positive full-scale reading and near negative full-scale reading. Rollover error is tested by applying a full-scale positive voltage, swapping AIN+ and AIN-, and adding the results.

Zero-Input Reading

Ideally, with AIN+ connected to AIN-, the MAX1366/MAX1368 LED displays zero. Zero-input reading is the measured deviation from the ideal zero and the actual measured point.

Gain Error

Gain error is the amount of deviation between the measured full-scale transition point and the ideal full-scale transition point.

Common-Mode Rejection (CMR)

CMR is the ability of a device to reject a signal that is common to both input terminals. The common-mode signal can be either an AC or a DC signal or a combination of the two. CMR is often expressed in decibels.

Normal-Mode 50Hz and 60Hz Rejection (Simultaneously)

Normal-mode rejection is a measure of how much output changes when 50Hz and 60Hz signals are injected into only one of the differential inputs. The MAX1366/MAX1368 sigma-delta converter uses its internal digital filter to provide normal-mode rejection to both 50Hz and 60Hz power-line frequencies simultaneously.

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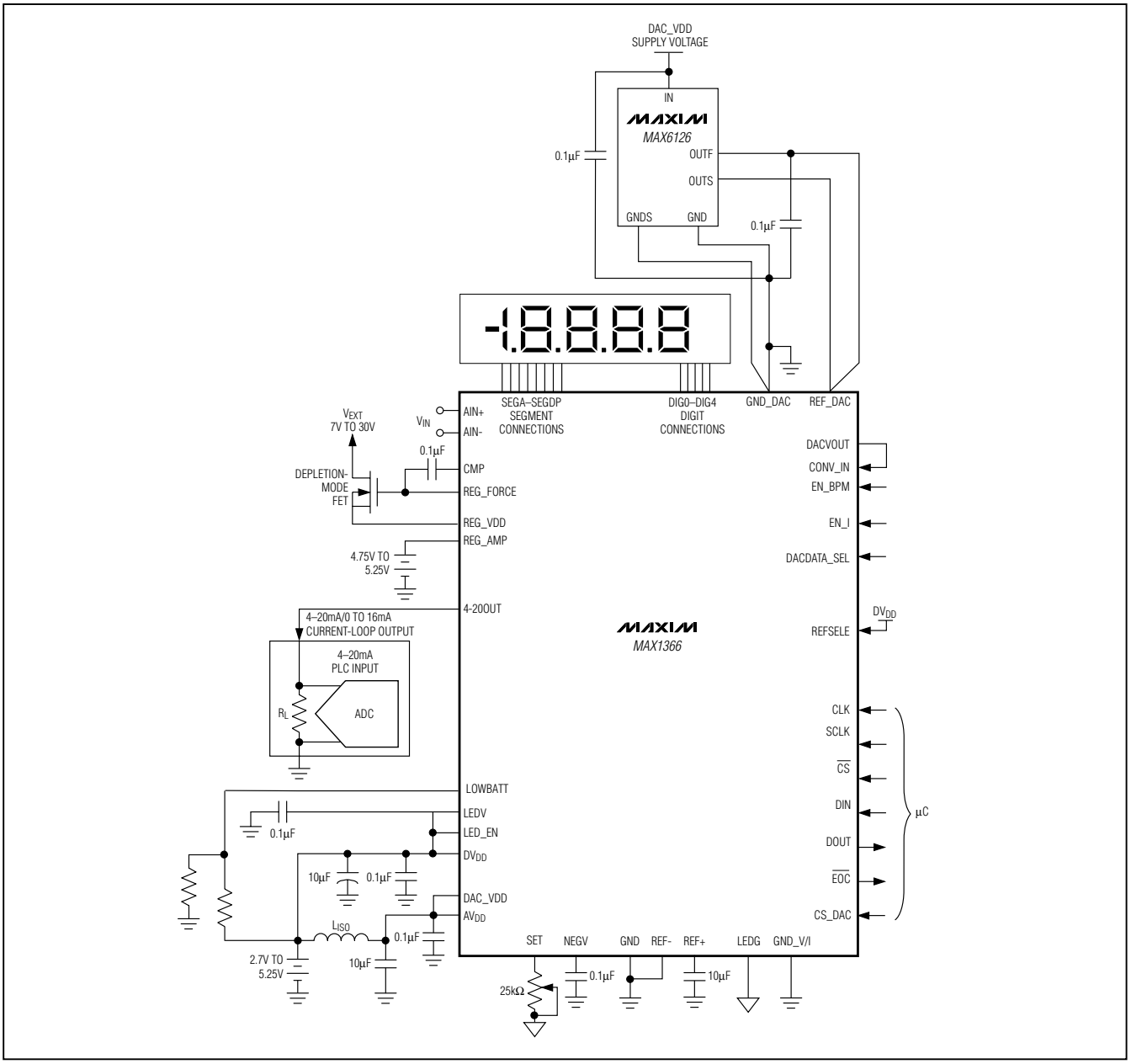
Power-Supply Rejection (PSR)—ADC

PSR is a measure of the data converter's level of immunity to power-supply fluctuations. PSR assumes that the converter's linearity is unaffected by changes in the power-supply voltage. Power-supply rejection ratio (PSRR) is the ratio of the input signal change to the change in the converter output. PSRR is typically measured in dB.

Power-Supply Rejection—V/I Converter

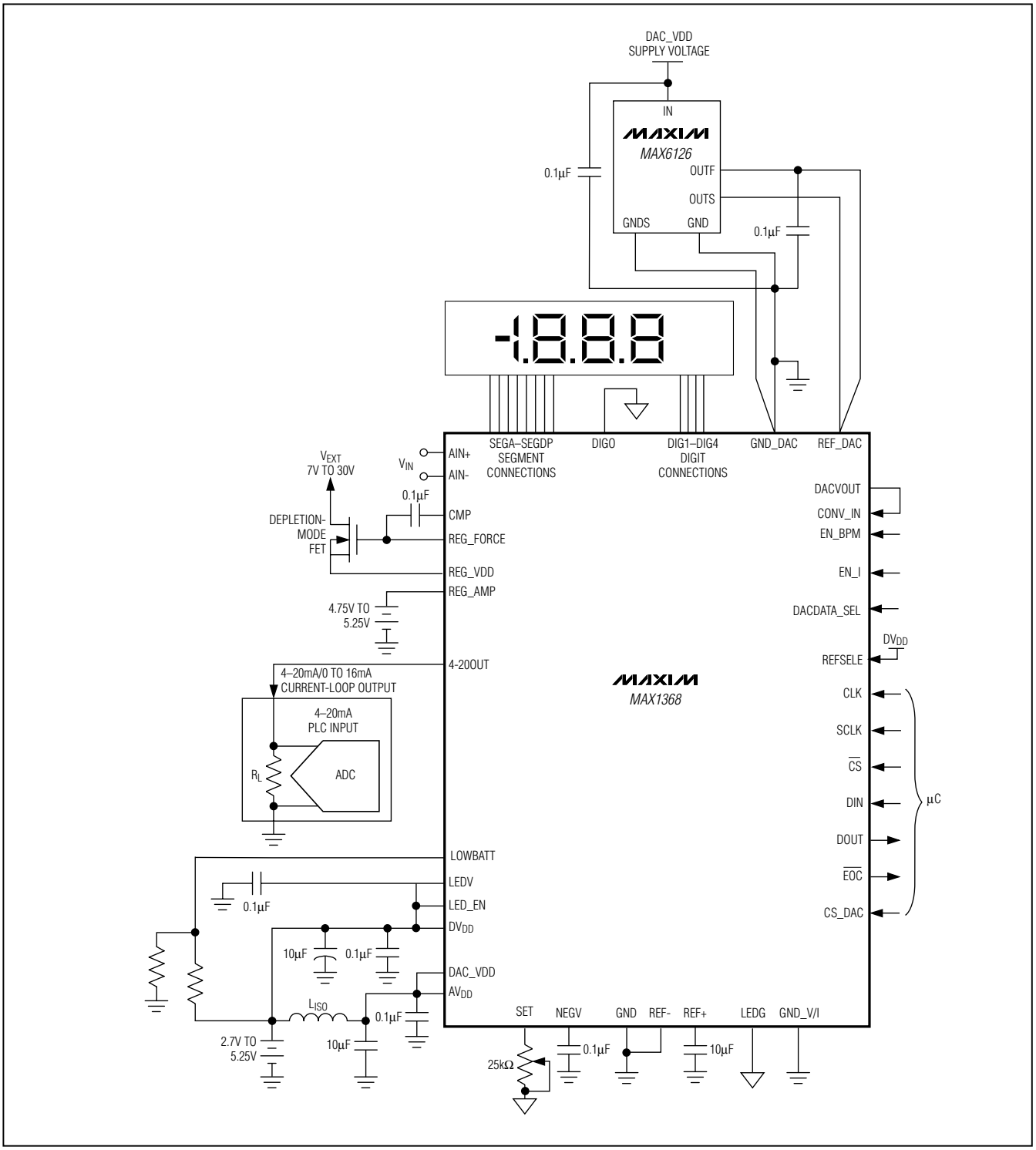
PSR is a measure of the data converter's level of immunity to power-supply fluctuations. PSR assumes that the converter's linearity is unaffected by changes in the power-supply voltage. Note that the V/I converter current output (4–20mA) power-supply rejection is with respect to the 7V to 30V loop supply.

MAX1366 Typical Operating Circuit

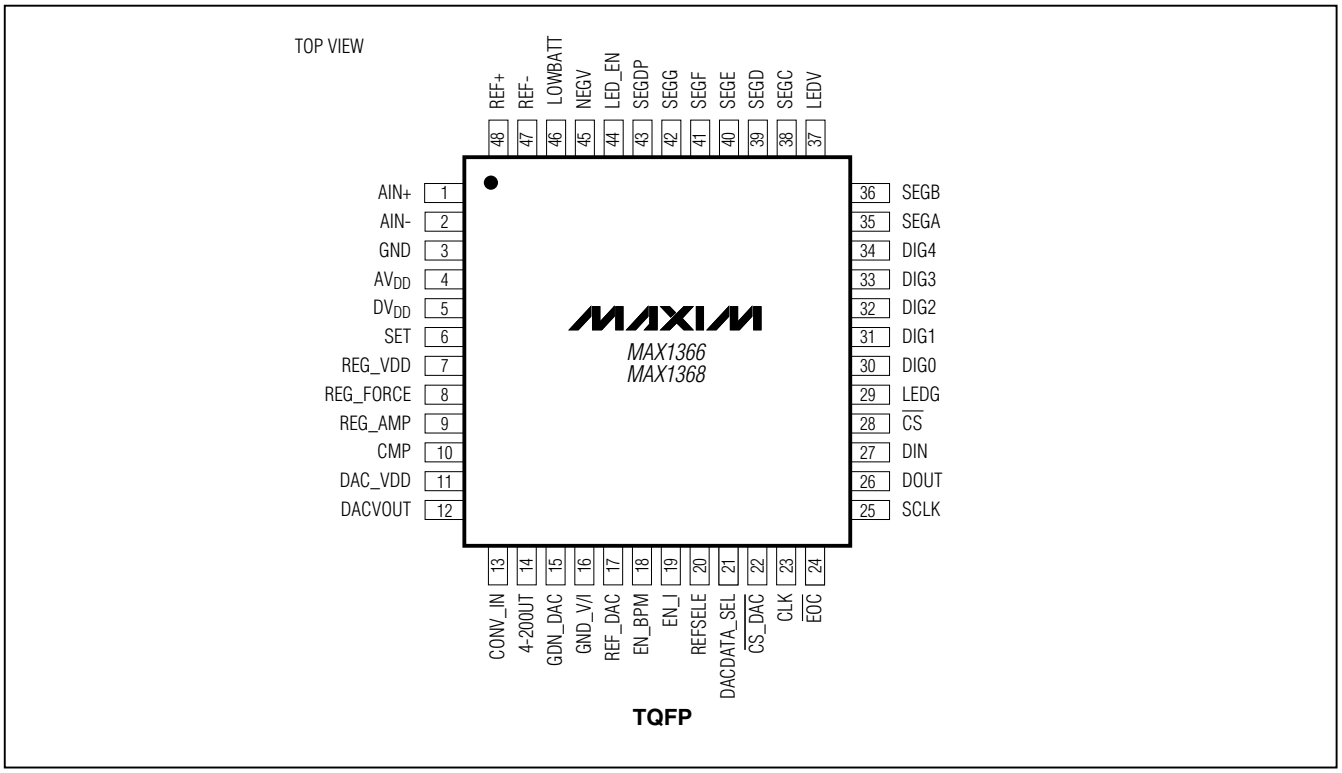


Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

MAX1368 Typical Operating Circuit



Pin Configuration



Chip Information

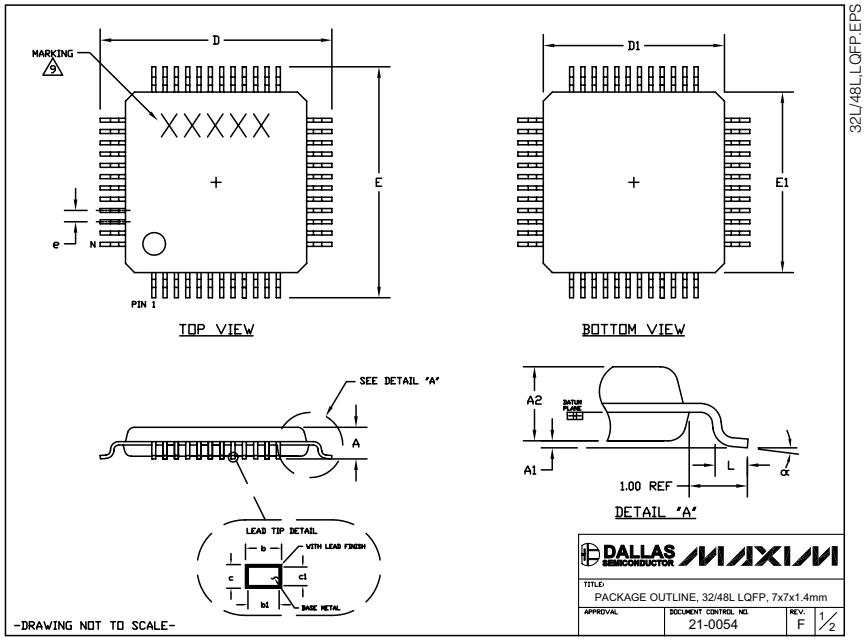
TRANSISTOR COUNT: 83,463

PROCESS: CMOS

Microcontroller-Interface, 4.5-/3.5-Digit Panel Meters with 4–20mA Output

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
10. NUMBER OF LEADS ARE SHOWN FOR REFERENCE ONLY.

JEDEC VARIATION	BBA		BBC	
	MIN.	MAX.	MIN.	MAX.
A	--	1.60	--	1.60
A1	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D1	6.90	7.10	6.90	7.10
E	8.90	9.10	8.90	9.10
E1	6.90	7.10	6.90	7.10
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
b1	0.30	0.40	0.17	0.23
c	0.09	0.20	0.09	0.20
c1	0.09	0.16	0.09	0.16
N	32		48	
α	0°	7°	0°	7°
PKG. CODES	C32-1; C32-2; C48-1; C48-2; C48-3; C48-4F; C48-5; C48-6; C48-9F			

-DRAWING NOT TO SCALE-
DALLAS SEMICONDUCTOR MAXIM
TITLE:
PACKAGE OUTLINE, 32/48L LQFP, 7x7x1.4mm
APPROVAL
DOCUMENT CONTROL NO.
21-0054
REV.
F
2/2