LED7708

16 channels x 85 mA LED driver with boost controller and 4-wire serial interface

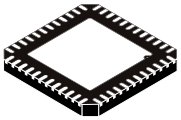
Datasheet —production data

Features

- Boost controller section
  - 3.6 V to 36 V input voltage range (LDO)
  - Adaptive output voltage for high efficiency
  - Internal +5 V LDO for gate driver supply
  - Internal +3.3 V LDO for device supply
  - High performance external MOSFET driver
  - 250 kHz to 1 MHz switching frequency
  - Programmable OV and OC protection
  - Fixed frequency peak current-mode control
  - External synchronization for multi-device application
  - Overtemperature alert and thermal shutdown
- LED array driver section
  - 16 channels with 85 mA/ch current capability
  - ±2% channel current accuracy
  - ±2% channel-to-channel current matching
  - LED short-circuit and open channel fault detection and management
  - 4-wire, 30 MHz serial interface
  - 16 x16-bit, 1x256-bit or 1x192-bit serial data formats
  - Grouped or independent channel PWM control
  - Selectable 12/16-bit grayscale brightness control for local dimming
  - Programmable internal dimming oscillator
  - Programmable grayscale latency
  - Master/slave chain configuration supported

Applications

- TV and monitor backlight units for LCD panels
- Medium and large size LCD panel backlights
- RGB/RGGB backlight solutions



VFQFPN 7x7x1.0 48L
(pitch 0.50)

Description

The LED7708 has been specifically designed to supply several LEDs starting from a single low-voltage rail. It integrates a boost controller, sixteen current generators and a 4-wire serial interface. The boost controller regulates the output voltage in an adaptive way, according to the LED requirements, resulting in an improved overall efficiency. All the current generators are 40 V-rated, allowing the LED7708 to drive several LEDs in series on each channel. The channels can be put in parallel for higher output current.

The brightness of the LEDs is controlled by using the serial interface. A selectable 12-bit or 16-bit grayscale brightness control allows independent PWM on each channel. A programmable on-chip dimming oscillator is provided for external circuitry simplification. The device has dedicated pins to lock to an external synchronization with other devices (master or slave) for noise reduction in multi-device applications. The LED7708 implements basic protection (OVP, OCP and thermal shutdown) as well as LED array protection. It can detect and manage open-LED and shorted-LED faults and different fault-management options are available in order to cover most application needs.

Table 1. Device summary

Order codes	Package	Packing
LED7708	VFQFPN-48 7x7 (exposed pad)	Tube
LED7708TR		Tape and reel

This is information on a product in full production. www.st.com

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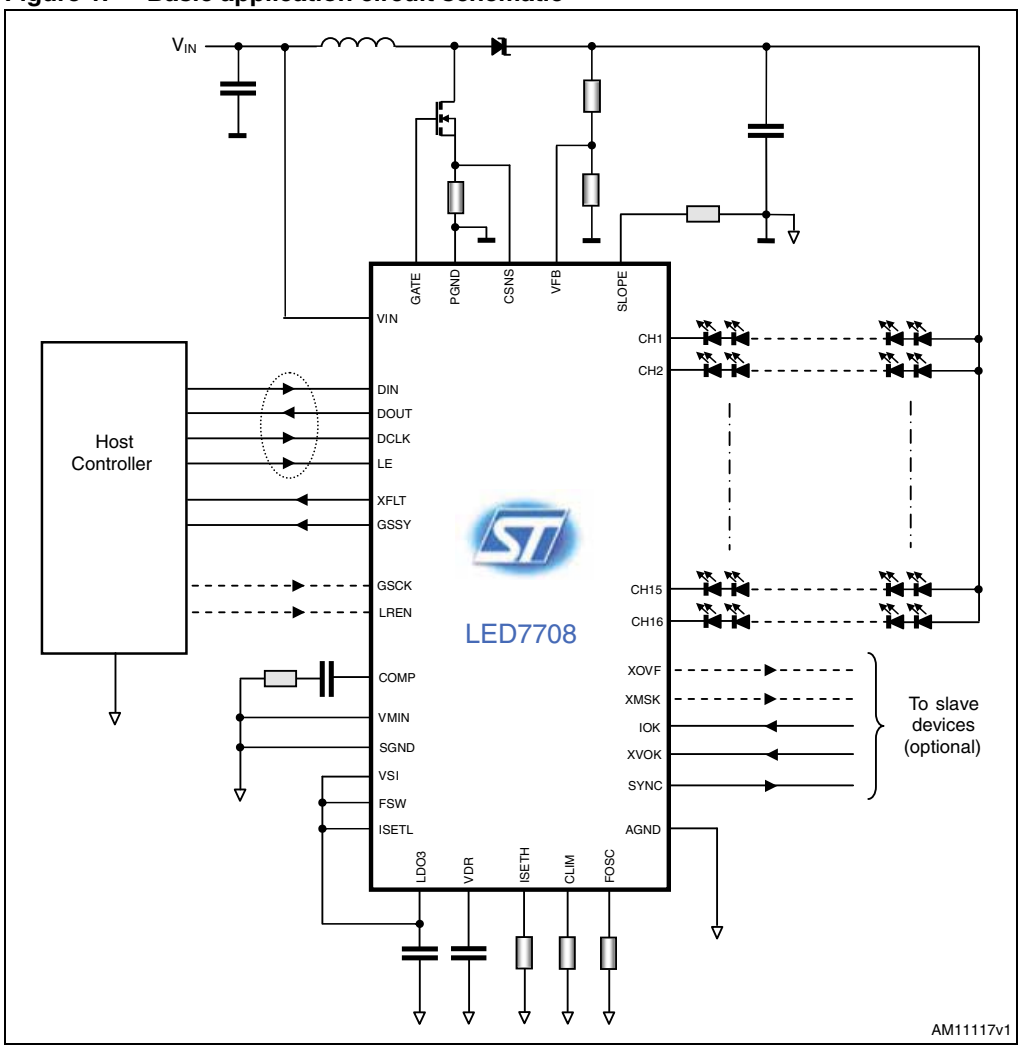
1 Typical application circuit

Figure 1. Basic application circuit schematic



2 Pin function

Figure 2. Pin connection (through top view)

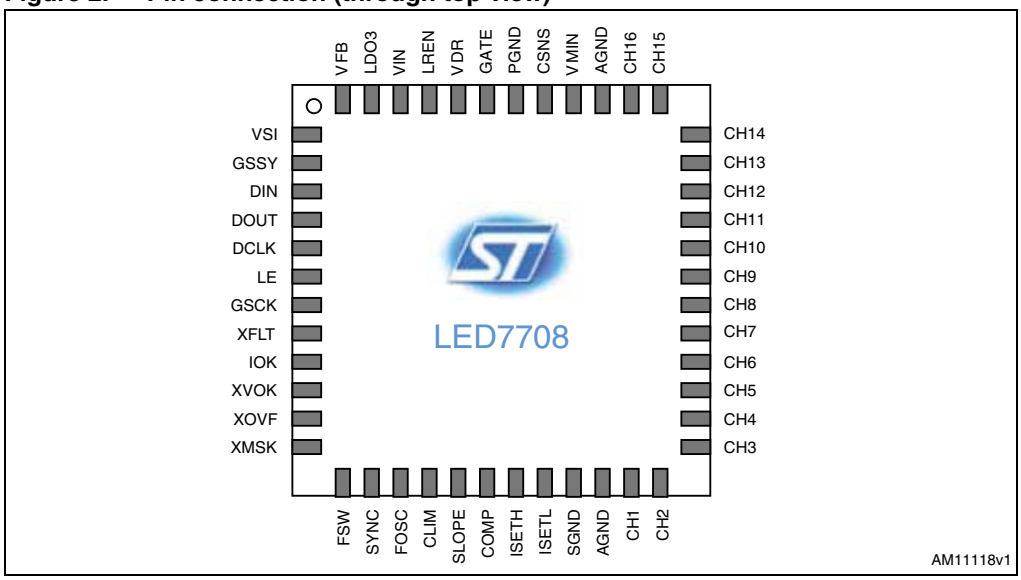


Table 2. Pin description

Pin		Function
1	VSI	Serial interface (SI) core and digital I/O buffer supply input. Connect to LDO3 or to an external supply (3 V-5 V). Insert a 100 nF bypass ceramic capacitor between this pin and SGND. Connect to the host controller's supply when possible.
2	GSSY	Grayscale synchronization output or VSYNC input. When the internal dimming generation is set, a pulse at the end of each dimming cycle is provided for data stream synchronization. Also used as dimming synchronization input to lock the dimming cycles on the vertical sync pulses.
3	DIN	Serial interface data input.
4	DOUT	Serial interface data out.
5	DCLK	Serial interface data clock.
6	LE	Serial interface latch enable.
7	GSCK	Grayscale clock I/O. When the internal dimming oscillator is used, the grayscale clock is provided at this pin. The pin becomes the grayscale clock input if the internal dimming oscillator is disabled (see FOSC pin).
8	XFLT	Fault signal, open drain output. The pin goes low when a faulty condition occurs.
9	IOK	Channel current OK handshake I/O. Used for extended output voltage regulation in multi-device applications. Used by slave devices to request a higher output voltage to the master. A 100 k pull-up resistor to LD03 is required.
10	XVOK	Channel voltage OK I/O (inverted). Used for extended output voltage regulation in multi-device applications. Used by slave devices to request an output voltage reduction to the master. A 100 k pull-up resistor to LD03 is required.

Table 2. Pin description (continued)

Pin		Function
11	XOVF	Internal DAC overflow I/O. Used for extended output voltage regulation and fault management in multi-device applications. It is used to inform slave devices that the maximum output voltage has been reached. A 100 k pull-up resistor to LD03 is required.
12	XMSK	Fault detection masking I/O. This signal is used for extended output voltage regulation & fault management in multi-device applications. It is used to avoid incorrect fault detection by forcing slave devices to ignore LED-short detection during output voltage steering. A 100 k pull-up resistor to LD03 is required.
13	FSW	Switching frequency selection / synchronization input. Used to set the desired switching frequency of the boost controller. Also used as synchronization input.
14	SYNC	Boost converter synchronization output. The buffered switching clock signal is provided at this pin to eventually synchronize other SMPS in the host system.
15	FOSC	Dimming oscillator frequency. A resistor to ground sets the frequency of the internal grayscale clock dimming oscillator. If set high, the internal dimming oscillator is disabled and the GSCK pin becomes the clock input (see GSCK pin).
16	CLIM	Boost section current limit setting. A resistor between this pin and SGND sets the boost converter current limit.
17	SLOPE	Slope compensation setting. A resistor between this pin and SGND is required to set the proper amount of slope compensation to avoid sub-harmonic instability.
18	COMP	Transconductance amplifier output. Connect a simple RC series between this pin and SGND to properly compensate the loop-gain of the boost converter.
19	ISETH	Output current setting (on). Connect a resistor between this pin and SGND to set the current sunk by each channel during the on-phase of the dimming.
20	ISETL	Output current setting (off). Connect a resistor between this pin and SGND to set the current sunk by each channel during the off-phase of the dimming (LED biasing). Connect to LDO3 to disable the bias current.
21	SGND	Signal ground. Common return for signals and settings.
22	AGND	Analog Ground. Common return for the current generators (channels).
23	CH1	Driver output (channel) #1.
24	CH2	Driver output (channel) #2.
25	CH3	Driver output (channel) #3.
26	CH4	Driver output (channel) #4.
27	CH5	Driver output (channel) #5.
28	CH6	Driver output (channel) #6.
29	CH7	Driver output (channel) #7.
30	CH8	Driver output (channel) #8.
31	CH9	Driver output (channel) #9.
32	CH10	Driver output (channel) #10.
33	CH11	Driver output (channel) #11.
34	CH12	Driver output (channel) #12.
35	CH13	Driver output (channel) #13.

Table 2. Pin description (continued)

Pin		Function
36	CH14	Driver output (channel) #14.
37	CH15	Driver output (channel) #15.
38	CH16	Driver output (channel) #16.
39	AGND	Analog ground. Common return for the current generators (channels).
40	VMIN	Minimum output voltage setting. Multi-level input (high, low, floating or resistor to SGND). Used in conjunction with the VFB pin to set the best output voltage range swing for a given LED array. See related section for further details.
41	CSNS	External MOSFET current sense input. Connect to the sensing resistor in series with the power switch (source of the power MOSFET node).
42	PGND	Power ground. Reference for the external MOSFET current sensing circuit and return for the gate driver.
43	GATE	External MOSFET gate driver output. Connected to the gate of the power MOSFET.
44	VDR	Gate driver supply. Internally connected to the 5 V LDO regulator. Bypass with a 1 µF ceramic capacitor to PGND as close as possible to the chip.
45	LREN	3.3 V linear regulator enable. When high or floating, the internal 3.3 V linear regulator is used to supply the device. Also used to turn off the device for power consumption reduction. To be left floating the internal 3.3 V LDO is overdriven by an external 3.3 V supply rail.
46	VIN	Input of the LDO linear regulators. Bypass with a 1µF ceramic capacitor to ground as close as possible to the chip.
47	LDO3	3.3 V device supply and internal 3.3 V linear regulator output. Bypass with a 1 µF ceramic capacitor to ground as close as possible to the chip.
48	VFB	Output voltage feedback for the boost controller. Connect to the central tap of the output resistor divider. See the related section for details.

3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Pin	Min.	Max.	Unit
	Maximum pin voltage	VIN, CH1 to CH16	-	40	V
		LDO3	-	VIN+0.3 3.6	
		COMP, SYNC, ISETH, ISETL, SLOPE, CLIM, FOSC, VFB, XOVF, VMIN	-	LDO3+0.3 3.6	
		VSI	-	6	
		DCLK, LE, DIN, GSCK, DCLK, DOUT, GSSY	-	VSI+0.3 6	
		IOK, XMASK, XVOK, XFLT, FSW, LREN,	-	6	
		VDR	-	6 VIN+0.3	
		GATE	-	VDR+0.3 6	
		CSNS	-	LDO3+0.3 3.6	
	Continuous channel current	CH1 to CH16	-	90	mA
	Maximum current generator power dissipation	CH1 to CH16	-	0.5	W
ESD	ESD Rating	Human body model JEDEC JESD22-A114	-	2	kV

Table 4. Thermal data

Symbol	Parameter	Conditions	Min.	Max.	Unit
P_D	Power dissipation(1)	T_A = 25 °C			W
		T_A = 50 °C			
		T_A = 85 °C			
$T_{J,OP}$	Operating junction temperature		-40	150	°C

Table 4. Thermal data (continued)

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{STG}	Storage temperature range		-50	150	
$R_{th,JA}$	Junction-ambient thermal resistance			30	°C/W

1. Device soldered to the STEVAL-ILL035V1 demonstration board.

4 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC Characteristics					
V_{VIN}	VIN pin input voltage range		3.6	36	V
V_{LDO3}	LDO pin input voltage range	VIN, LDO3 and VDR shorted together	3.0	3.6	
V_{VDR}	VDR pin input voltage range	VDR and VIN shorted together	3.0	5.5	
V_{CHx}	Channel voltage range			36	
V_{VSI}	Serial interface supply voltage		3.0	5.5	
I_{CHx}	Channel continuous current		20	85	mA
	Channel current when OFF (adjustable)		2	200	µA
AC Characteristics (V_{SI} = 3.3 V)					
f_{GSC}	Grayscale clock frequency			25	MHz
f_{DCLK}	Serial clock frequency			30	
f_{SW}	Boost converter switching frequency		200	1000	kHz
$T_{w,DCLK}$	DCLK pulse width		20		ns
$T_{w,GSC}$	GSC pulse width		20		
$T_{w,LE}$	LE pulse width		15		
$T_{su,DIN}$	DIN setup time		5		
$T_{h,DIN}$	DIN hold time		5		
$T_{su,LE}$	LE setup time		5		
$T_{h,LE}$	LE hold time		5		

5 Electrical characteristics

(V_{IN} = 12 V; T_{AMB} = 25 °C and VSI connected to LDO3 if not otherwise specified.)

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply section						
	LREN turn-on threshold				1.4	V
	LREN turn-off threshold		1			µA
	LREN pull-up current			3		
$V_{UVLO,ON}$	LDO3 undervoltage lockout upper threshold			2.9	3.0	V
$V_{UVLO,OFF}$	LDO3 undervoltage lockout lower threshold		2.6	2.7		
$V_{VSI,ON}$	VSI turn-on threshold			3.0	3.1	
$V_{VSI,OFF}$	VSI turn-off threshold		2.6	2.7		
V_{LDO3}	3.3 V LDO output voltage	3.6 V ≤V_{VIN} ≤28 V I_{LDO3}=0 mA, DEN=0	3.2	3.3	3.4	mV
	3.3 V LDO load regulation	V_{VIN}=3.6 V, DEN=0 0 mA ≤I_{LDO3} ≤40 mA		30	100	
	3.3 V LDO drop-out voltage	I_{LDO3}=40 mA, V_{LDO3}=3.2 V	180	270		
V_{VDR}	5 V LDO output voltage	6 V ≤V_{VIN} ≤28 V I_{VDR}=0 mA, DEN=1	4.5	5.0	5.5	V
	5 V LDO load regulation	V_{VIN}=6 V, DEN=1 0 mA ≤I_{VDR}≤40 mA		60	200	mV
	5 V LDO drop-out voltage	I_{VDR} =40 mA, V_{VDR}=4.5 V	150	200		mV
Boost controller						
$t_{ON,min}$	Minimum switching on-time			100	170	ns
f_{SW}	Default switching frequency	FSW to LDO3	550	610	670	kHz
	Synchronization input frequency		180		1020	
K_{FSW}	Switching frequency constant	R_{FSW} = 100 kΩ	4.4 x10^{10}	5.0 x10^{10}	5.6 x10^{10}	Hz • Ω
$I_{GATE,Pk}$	Gate driver current capability	C_L=3.3 nF, sourcing		1.9		A
		C_L=3.3 nF, sinking		2.1		
$t_{r,GATE}$	Gate driver rise time (10 to 90%)	C_L=3.3 nF		9		ns
$t_{f,GATE}$	Gate driver fall time (90 to10%)			10		

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	FSW synchronization input low level				0.5	V
	FSW synchronization input high level		2.2			
	SYNC output duty cycle	FSW connected to LDO3	25	30	35	%
	SYNC output high level	I_{SYNC}=1 mA	V_{LDO3} -0.3 V			V
	SYNC output low level	I_{SYNC}=-1 mA			0.4	
	Adjustable power MOSFET current sensing voltage	R_{CLIM}=100 kΩ		100		mV
		R_{CLIM}=300 kΩ		300		
Power consumption						
I_{VIN1}	Shutdown current (SI off, LED drivers off, SMPS off, LDOs off)	LREN low, VSI low			30	µA
I_{VIN2}	Shutdown current (SI active, LED drivers off, SMPS off, LDOs on)	LREN floating VSI to LDO3 DEN=0		300	450	
I_{VIN3}	Quiescent current (LED drivers off, boost section not switching)	LREN floating; VSI, FOSC and ISETL to LDO3; DIN, DCLK, LE, GSCK and GSSY to GND; V_{CHx}=2 V; R_{ISETH}=60 kΩ		4		mA
I_{VIN4}	Operating current (serial interface active, boost not switching)	LREN floating VSI and FOSC to LDO3, DIN and DCLK toggling at 15 MHz, DOUT, GSSY and GSCK floating, LE to GND. V_{CHx}=2 V, R_{ISETH}=60 kΩ		7		
I_{VSI1}	Standby current (DIN, DCLK and LE to SGND, LED drivers off, SMPS off, LREN floating)	VSI = 3.3 V		7		µA
		VSI = 5.0 V		9		
OV protection, output regulation						
$V_{FB,OVP}$	Overvoltage protection reference threshold	V_{MIN} tied to GND	1.275	1.30	1.325	V
		V_{MIN} to LDO3	1.105	1.13	1.155	
		R_{VMIN}=220 kΩ	0.985	1.01	1.035	
		V_{MIN} floating	0.765	0.8	0.815	
$V_{FB,OVP}$	OVP hysteresis			6		mV

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{DAC,FB}$	Maximum internal reference voltage for output regulation	VMIN to GND	1.136	1.161	1.186	V
		VMIN to LDO3	0.967	0.992	1.017	
		R_{VMIN}=220 kΩ	0.847	0.872	0.897	
		VMIN floating	0.630	0.655	0.680	
	Minimum internal reference voltage for output regulation	VMIN to GND	0.836	0.861	0.886	
		VMIN to LDO3	0.667	0.692	0.717	
		R_{VMIN}=220 kΩ	0.547	0.572	0.597	
		VMIN floating	0.330	0.355	0.380	
Current generators						
ΔI_{CHxn}	Maximum output current accuracy with respect to nominal value(1)	V_{CHx}=0.6 V, 20 mA ≤ I_{CHx} ≤85 mA		±2%	±3%	
ΔI_{CHxy}	Maximum channel-to-channel output current mismatch(1) (all channels active)	V_{CHx}=0.6 V, R_{ISETH}=60 kΩ (I_{CHx}=20 mA)		±2%		
V_{CHx}	Minimum master channel feedback voltage	R_{ISETH}=60 kΩ, CRS=0		500	600	mV
		R_{ISETH}=15 kΩ, CRS=1		700	800	
V_{RW}	Regulation window amplitude	R_{ISETH}=60 kΩ, RWAS=0	190	250	310	
		R_{ISETH}=60 kΩ, RWAS=1	400	500	600	
$I_{CHx,OFF1}$	Off-state channels current	V_{CHx}=10 V, R_{ISETL}=50 kΩ	70	80	90	µA
$I_{CHx,OFF2}$		V_{CHx}=10 V, ISETL to LDO3		1	2	
$V_{TH,ISETL}$	ISETL input threshold $I_{CHx, OFF2}$		V_{LDO3-1}			V
K_{ISETH}	Output current high-state constant	20 mA ≤ I_{CHx} ≤85 mA	1164	1200	1236	
K_{ISETL}	Output current low-state constant		3.5	4.0	4.5	
Serial interface						
	DIN, DCLK, LE, GSCK, GSSY low level input threshold	VSI=LDO3=3.3 V			1.32	V
	DIN, DCLK, LE, GSCK, GSSY high level input threshold		1.6			
	DOUT and GSSY output low level	VSI=LDO3=3.3 V I_{LOAD}=-200 µA			1.22	
	DOUT and GSSY output high level	VSI=LDO3=3.3 V I_{LOAD}=200 µA	1.75			

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Fault management						
$V_{CHx,FLT1}$	LED short-circuit detection threshold	DTS0=1& DTS1=0	3.0	3.2	3.4	V
$V_{CHx,FLT2}$		DTS0=0& DTS1=1	6.2	6.4	6.6	
$V_{CHx,FLT3}$		DTS0=1& DTS1=1	7.7	8.0	8.3	
	XFLT output low level	$I_{XFLT, SINK}$=4 mA		200	220	mV
Dimming oscillator						
K_{OSC}	Internal dimming oscillator constant	R_{FOSC}=33.2 kΩ	3.86 x10^{11}	4 x10^{11}	4.14 x10^{11}	Hz•Ω
$F_{GSCK,OSC}$	Internal dimming oscillator frequency	R_{FOSC}=100 kΩ		4		MHz
		R_{FOSC}=16 kΩ		25		
Thermal flag and protection						
T_{OTA}	Overtemperature alert threshold			125		°C
	Overtemperature alert hysteresis			20		
T_{OTP}	Overtemperature protection threshold			155		

1. Channel current accuracy is calculated as:

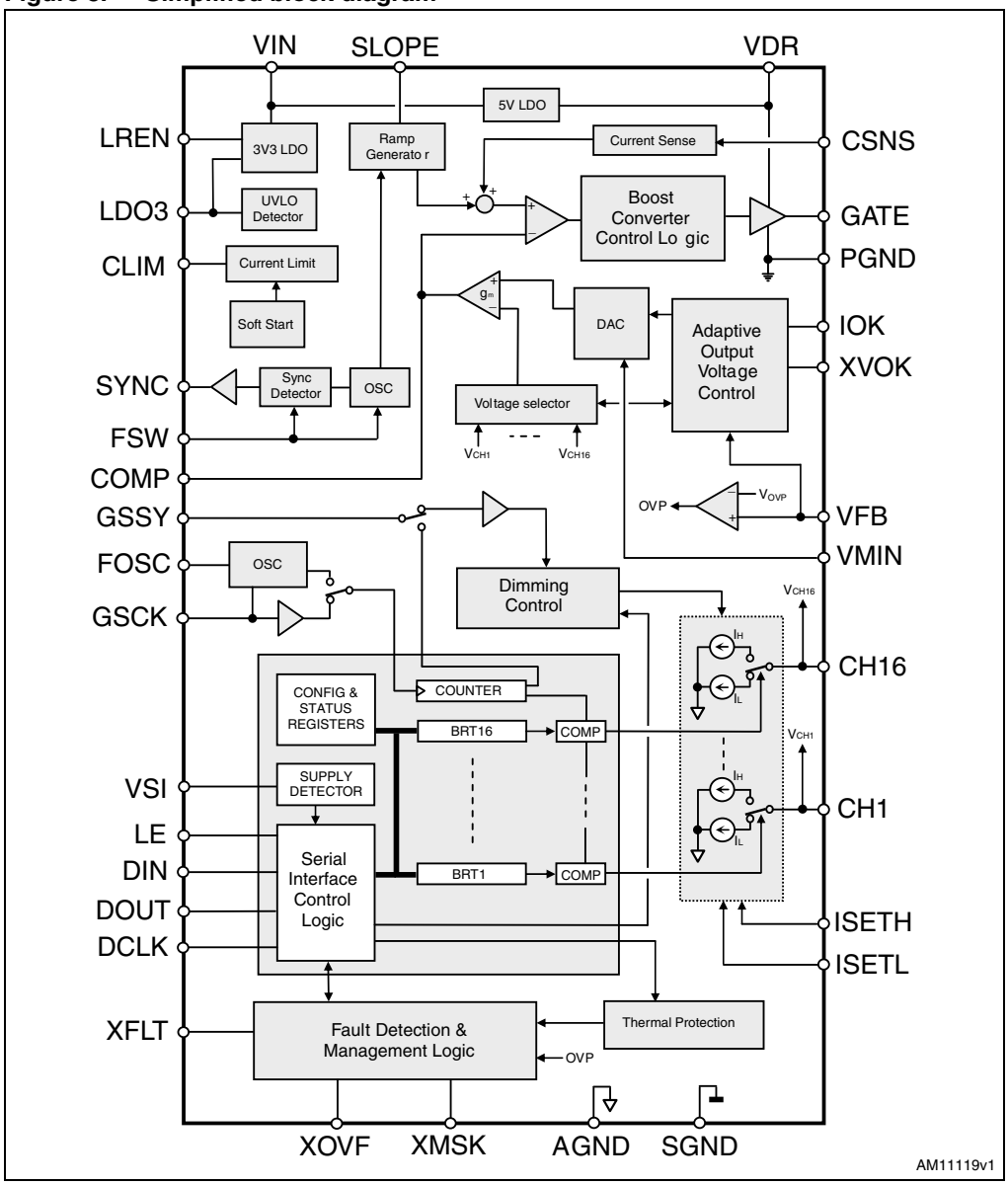
$$\Delta I_{CHX} = \max\frac{(|I_{CHX} - I_{TARGET}|)}{I_{TARGET}} \bullet 100$$

$$\Delta I_{CHY} = \max\frac{(|I_{CHX} - I_{CHY}|)}{I_{TARGET}} \bullet 100$$

where X, Y=1..16, X≠Y.

6 Block diagram

Figure 3. Simplified block diagram



7 Device description

The LED7708 is an LED driver that integrates a boost controller, sixteen current generators and a 4-wire serial interface. It has been specifically designed for driving the LED backlight in medium to large LCD panels.

The device is controlled by a 4-wire serial interface and can operate both as standalone driver and as master driver in conjunction with other slave devices.

Basic and advanced dimming functions are supported in order to meet different application requirements. Regardless of the dimming control technique, the LED7708 can optimize the power dissipation by controlling the output voltage of the boost converter. Two internal linear regulators derive the device supply (3.3 V) and the gate driver supply (5 V) from a single power rail.

7.1 Device supply

The LED7708 integrates two low drop-out linear regulators to derive the +3.3 V (typ.) main supply and the +5 V supply for the gate driver. The VIN pin is the input terminal for both linear regulators. The output of the 3.3 V LDO is the LDO3 pin, the output of the 5 V LDO is the VDR pin. The 3.3 V LDO (LDO3 pin) is active if the LREN (linear regulator enable) pin is left floating or externally set high (see *Section 5: Electrical characteristics* for the thresholds involved).

The serial interface I/O stage is supplied through the VSI pin. This pin is used to enable the serial interface and it allows the setting of the logic level of the serial interface signals (3.3 V or 5 V) at the same time. The serial interface can be powered by the internal 3.3 V LDO (by simply connecting the LDO3 pin to the VSI pin) or by an external source, usually the same supply rail as the host controller.

When an external +3.3 V source is available, it is possible to bypass the 3.3 V LDO by connecting VIN, VDR and LDO3 together to the +3.3 V rail; in this case the gate driver is supplied at 3.3 V too and a super-logic level MOSFET is required as the power switch.

The 3.3 V regulator is self-protected against overcurrent and thermal damage thanks to a foldback mechanism. The continuous current capability of the 3.3 V LDO is calculated to not exceed the junction temperature limit in worst power dissipation conditions.

A 1 µF MLCC on the LDO3 pin is required for ripple filtering and LDO output stability.

The LDO3 pin is internally connected to the undervoltage lockout (UVLO) protection; the upper and lower UVLO thresholds are reported in *Section 5: Electrical characteristics*. When the voltage at the LDO3 pin falls below the lower UVLO threshold, the device is turned off (non-latched condition). The device turns on when the voltage at the LDO3 pin crosses the upper UVLO threshold. Crossing the lower and upper thresholds in sequence performs the so called “power-on reset” (POR). The POR sequence is used, as well as toggling the internal DEN bit (see internal registers), when the device is asked to restore normal operation after a latched fault condition. The 5 V linear regulator, whose output is connected to the VDR pin, is turned off when the device is disabled, while the 3.3 V linear regulator is controlled by the LREN pin only.

8 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC Characteristics					
V_{VIN}	VIN pin input voltage range		3.6	36	V
V_{LDO3}	LDO pin input voltage range	VIN, LDO3 and VDR shorted together	3.0	3.6	
V_{VDR}	VDR pin input voltage range	VDR and VIN shorted together	3.0	5.5	
V_{CHx}	Channel voltage range			36	
V_{VSI}	Serial interface supply voltage		3.0	5.5	
I_{CHx}	Channel continuous current		20	85	mA
	Channel current when OFF (adjustable)		2	200	µA
AC Characteristics (V_{SI} = 3.3 V)					
f_{GSC}	Grayscale clock frequency			25	MHz
f_{DCLK}	Serial clock frequency			30	
f_{SW}	Boost converter switching frequency		200	1000	kHz
$T_{w,DCLK}$	DCLK pulse width		20		ns
$T_{w,GSC}$	GSC pulse width		20		
$T_{w,LE}$	LE pulse width		15		
$T_{su,DIN}$	DIN setup time		5		
$T_{h,DIN}$	DIN hold time		5		
$T_{su,LE}$	LE setup time		5		
$T_{h,LE}$	LE hold time		5		

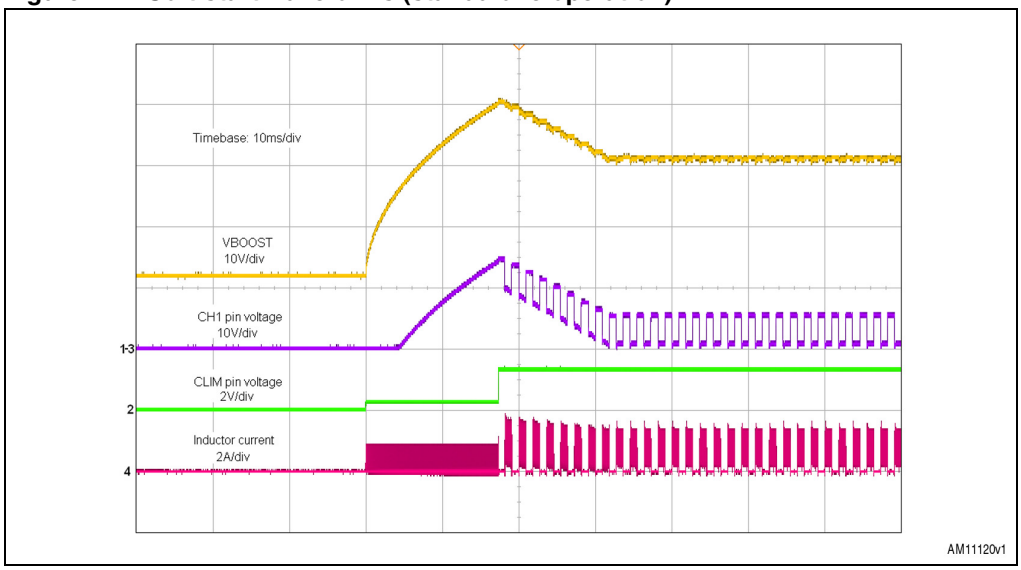
8.1 Device power-up and soft-start

The VSI pin (supply input for the serial interface) has a high level threshold lower than the upper UVLO threshold at the LDO3 pin, ensuring that the serial interface is enabled prior to the device being turned on. Anyway, after the POR, the DEN (device enable) bit of the internal DEVCFG0 control register is low (default value) and the device is off. The soft-start sequence takes place as soon as this bit is asserted.

If the LED7708 is set to operate in standalone, the soft-start procedure takes place in two steps (*Figure 4*):

1. The switching frequency is reduced to one fourth of the nominal value and the boost current limit is set to 20%. This phase finishes approximately 1 ms after the output voltage reaches the maximum value (not the OVP level). During this phase the channels are disabled.
2. Both the switching frequency and the boost current limit are released to their respective nominal values and then the channels are enabled.

Figure 4. Soft-start waveforms (standalone operation)



A slightly different soft-start procedure takes place if the LED7708 is set to operate as master in conjunction with other slave devices:

1. The switching frequency is reduced to one eighth of the nominal value and the boost current limit is set to 20%. This phase finishes approximately 1 ms after the output voltage reaches the maximum value (not the OVP level). During this phase the channels are active.
2. The switching frequency is increased to half the nominal value. This phase is held for approximately 2 ms.
3. The switching frequency is further increased to the nominal value while the current limit changes to 40% (~5 ms duration).
4. The current limit is released to its nominal values.

8.2 Device shutdown

The device is turned off by clearing the DEN bit of the DEVCFG0 register. The content of most of the internal registers is not cleared acting on the DEN bit.

The LREN pin can be also used to turn the device on and off whenever the internal 3.3 V LDO is used to supply the LED7708 (POR). In this case the content of the internal registers is lost.

8.3 Boost controller section and output voltage control

The boost section of the LED7708 consists of:

- Fixed-frequency current-mode step-up controller
- Output voltage optimization loop
- External MOSFET gate driver
- Related protection circuitry.

8.3.1 Output voltage optimization

The output voltage of the boost section is the supply rail for the LED strings and is regulated in an adaptive way to improve the overall efficiency. A dedicated digital-to-analog converter (DAC) is used to change the reference voltage of the loop and the output voltage is adjusted in order to keep the power dissipation of the LED driving section to the minimum level.

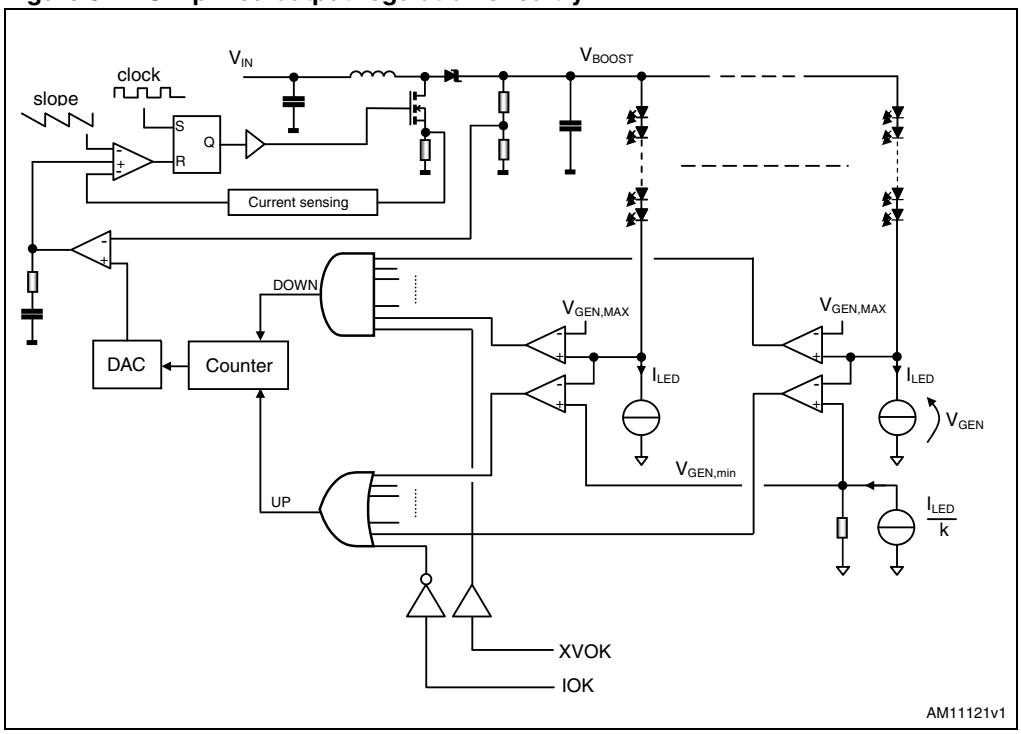
The optimization is achieved by keeping the voltage drop across the channels inside a fixed window (regulation window) and its amplitude can be selected between two values (300 mV and 600 mV) by acting on the internal registers. The lower threshold of the regulation window (V_{RWL}) is a function of the set LED current (*Equation 1*) and the upper threshold (V_{RWH}) is therefore determined.

Equation 1

$$V_{RWL} = K_W \cdot R_{ISETH}$$

Figure 5 shows the simplified regulation circuit.

Figure 5. Simplified output regulation circuitry



During normal operation, the regulation algorithm is the following:

- if at least one active channel has a voltage drop below the lower threshold, the internal DAC counts up and the output voltage is increased
- if all the active channels have a voltage drop higher than the upper threshold, the internal DAC counts down and the output voltage is reduced.

Therefore, the possible operating configurations are shown in *Table 8*.

Table 8. Output voltage states during regulation

Output voltage	Condition
Excessive	All the channels have their voltage above the upper threshold of the regulation window.
Optimal	All the channels have their voltage inside the regulation window.
Regulated	Most of the channels have their voltage inside the regulation window; the remaining channels have a voltage drop above the upper threshold.
Insufficient	At least one channel has its voltage drop below the lower threshold of the regulation window.

The algorithm can also manage faulty conditions that may occur on the LED array (open channels and LED short-circuit) in order to prevent excessive power dissipation.

The LED7708 has been designed to interface with other slave devices and can provide them with the correct LED supply voltage by extending the above mentioned output voltage optimization. For this purpose, some handshake signals have been reserved:

Table 9. Handshake signals summary

Pin	Function
IOK	Used by the slaves to increase the output voltage (algorithm is overdriven)
XVOK	Used by the slaves to ask for an output voltage reduction
XOVF	Used by the master to inform that the maximum output voltage has been reached (each slave uses this information to tag as “faulty” its open channels)
XMSK	Used by the master to inform the slaves that the output voltage is out of regulation and the LED fault detection must be masked to prevent false detection

The two signals IOK and XVOK are connected (wired-or) to all the slave devices sharing the same output voltage rail: if a channel has a low-voltage drop (below V_{RWL}), the device that owns that channel forces low the IOK signal. In a similar way, the XVOK is released if the voltage across all the channels of a slave is higher than required (above V_{RWH}). The wire-or connection of this signal ensures that the output voltage reduction takes place only if all the slaves (and the master itself) need this operation. Refer to the special functions section for a detailed explanation of the daisy chain connection between the master and slave devices.

The boost converter is always active regardless of how many channels are active (i.e. even if all channels are off) in order to improve the load transient dynamic response.

The output voltage regulation can be enabled/disabled (the OVRE bit of the DEVCFG0 register), allowing the user to perform the optimization continuously or on demand.

In real applications, the spread of the forward voltage of the LEDs may cause the channels to have different voltage drops. In any case, the leading channel (i.e. the channel requiring the highest voltage to drive its LED string) is kept inside the regulation window.

The reference voltage, provided by the internal DAC, spans between the minimum and maximum values, programmable through the VMIN pin (see *Section 5: Electrical characteristics*).

As a consequence, the output voltage can be varied by the device in the following range:

Equation 2

$$V_{BOOST,min} = \left(\frac{R_1 + R_2}{R_1}\right) \cdot V_{VFB,min}$$

Equation 3

$$V_{BOOST,MAX} = \left(\frac{R_1 + R_2}{R_1}\right) \cdot V_{VFB,MAX}$$

where R1 and R2 are the resistors of the divider connected to the output rail and V_{VFB} is the reference voltage at the VFB pin.

The LED7708 regulates the output voltage in order to optimize the overall efficiency and, to do this, it needs to read the voltage drop across the active current generators. Unfortunately, in some cases (e.g. during the soft-start phase or when all the channels are set to 0% brightness), the current generators are off and there is no useful information coming from them. Therefore the output voltage is regulated to the minimum value (*Equation 2:*). It must be ensured that the minimum output voltage is below the minimum expected output voltage

in order to guarantee enough steering room for the optimization. Because of the significant dependence of the LED forward voltage with temperature, this must be taken into account when calculating the minimum expected output voltage.

The best way to proceed when designing the external components is the following:

1. Determine the output voltage range required by the LED strings, considering V_F spread and temperature variation:

$$V_{LED} = \max_{i=1}^{N_{ROWS}} \left(\sum_{j=1}^{m_{LEDS}} V_{F,j} \right)$$

2. Calculate the middle-point of the output voltage range $V_{BOOST,middle}$.
3. Calculate the output divider through *Equation 4* and *5*.
4. Calculate the resulting four output voltage ranges (VMIN setting options).
5. Select the output voltage range closest to the one calculated at point 1.

Equation 4

$$R_2 = \frac{(V_{BOOST,middle} - V_{VFB})}{V_{VFB}} \cdot R_1$$

Equation 5

$$\frac{V_{BOOST,MAX}}{R_1 + R_2} \leq 100\mu A$$

8.3.2 Boost converter loop

The voltage drop of each current generator is sent to the minimum voltage selector: the lowest one is used as feedback and sent to the window comparator, whose outputs are used to increase or decrease the loop-counter. The digital outputs of the counter are connected to the DAC and the target reference is generated. As previously mentioned, this reference voltage is compared to a partition of the output voltage: the difference is translated into an error current at the output of the trans-conductance amplifier (see *Figure 4*, COMP pin).

At this point the compensation network, externally connected to the COMP pin, provides the programmed trip level for the inductor current. An additional slope compensation ramp is mixed, as usual, to avoid possible sub-harmonic instability when the boost converter operates in continuous conduction mode (CCM). The SLOPE pin allows the proper setting of the amount of slope compensation connecting a simple resistor RSLOPE between the SLOPE pin and ground. The compensation ramp of a master device starts at 35% (typ.) of each switching period.

The boost converter switching frequency can be set in the 200 kHz-1 MHz range by connecting the FSW pin to ground through a resistor, calculated according to *Equation 6*:

Equation 6

$$R_{FSW} = \frac{K_F}{f_{SW}}$$

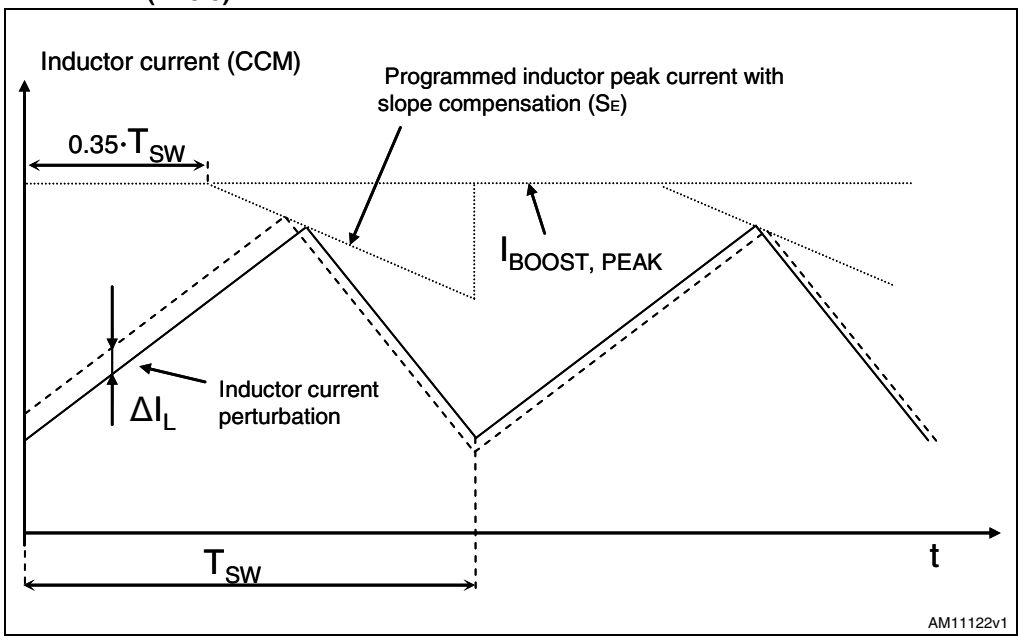
In addition, when the FSW pin is tied to LDO3, the LED7708 uses a default 610 kHz fixed switching frequency, allowing the saving of a resistor in minimum component-count applications.

The FSW pin can also be used as synchronization input, allowing the LED7708 to operate both as master or slave device. If a clock signal having a frequency within the capture range is applied to this pin, the device locks synchronized. The minimum pulse width which allows the synchronizing pulses to be detected is 270 ns (typ.). The SYNC pin is a synchronization output and provides a 35% (typ.) duty cycle clock when the LED7708 is set as master or a replica of the FSW pin when it is set as slave. It is used to connect multiple devices in a daisy chain configuration or to synchronize other switching converters running in the system with the LED7708. When an external synchronization clock is applied to the FSW pin, the internal oscillator is overdriven and the external power MOSFET is ignited on the rising edge of the synchronization signal while the slope compensation ramp starts on the falling edge of the same signal. For this reason, the duty cycle of the external synchronization clock should be 30% to 40% to prevent sub-harmonic instability when the boost converter is working in continuous-conduction mode (CCM).

8.3.3 Slope compensation

The constant frequency, peak current-mode topology has the advantage of very easy loop compensation with output ceramic caps (reduced cost and size of the application) and fast transient response. In addition, the intrinsic peak current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor. On the other side, this topology has a drawback: there is inherent open loop instability when operating with a duty cycle greater than 0.5. This phenomenon is known as “sub-harmonic instability” and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called “slope compensation”. As seen in *Figure 6*, when the switching duty cycle is higher than 0.5, the small perturbation ΔIL dies away in subsequent cycles thanks to the slope compensation and the system reverts to a stable situation.

Figure 6. Effect of slope compensation on small inductor current perturbation (D>0.5)



The SLOPE pin allows to properly set the amount of slope compensation connecting a simple resistor R_{SLOPE} between the SLOPE pin and the output. The compensation ramp starts at 35% (typ.) of each switching period and its slope is given by the following equation:

Equation 7

$$S_E = \frac{K_S}{R_{SLOPE}}$$

where $K_S = 4.0\ s^{-1}$ and S_E is the slope ramp in [A/s].

To avoid sub-harmonic instability, the compensating slope should be at least half the slope of the inductor current during the off-phase when the duty cycle is greater than 50%. The value of R_{SLOPE} can be calculated according to *Equation 8*.

Equation 8

$$R_{SLOPE} \leq \frac{2 \cdot K_s \cdot L \cdot (V_{OUT} - V_{IN} - 0.7V)}{(V_{OUT} - V_{IN})}$$

8.3.4 External MOSFET control

The LED7708 employs an external MOSFET as the power switch for the boost converter.

The internal gate driver is capable of sourcing and sinking up to 1 A and it is supplied through the VDR pin, internally connected to the +5 V LDO. A 1 µF decoupling capacitor, connected between the VDR pin and PGND, is highly recommended. When an external +5 V supply is available, the whole device can be supplied by connecting both the VDR and VIN pins to this rail.

Detailed information about the MOSFET gate driver can be found in *Section 5: Electrical characteristics*.

The current flowing through the power MOSFET is sensed during the on-phase by measuring the voltage drop across an external sensing resistor (connected between the source of the MOSFET and PGND). The overcurrent condition is detected by comparing the sensed voltage with an internal threshold. This threshold can be set in the 100 mV - 300 mV range according to the resistor connected between the CLIM pin and ground. The sensing resistors are often available in few values: once a suitable one has been selected, the resistor at the CLIM pin is calculated according to the following equation:

Equation 9

$$R_{CLIM} = \frac{(R_{SNS} \cdot I_{MOS,OCP} + K_{C2})}{K_{C1}}$$

where K_{C1} = 1.63 x 10^{-5} V and K_{C2} = 3.1 x 10^{-2} A.

The maximum allowed peak current depends on the external MOSFET capability.

The actual maximum peak current is given by the above equations as long as duty cycle is below 35% and decreases as duty cycle increases beyond 35%, depending on the slope compensation setting. If an overcurrent (OC) condition occurs, the boost controller turns-off the external MOSFET and skips subsequent switching cycles until the current is above the programmed level.

In the case of a light load condition, the COMP pin voltage may fall below 0.8 V (typ.). In this case the boost controller stops switching until the error amplifier forces the COMP voltage to rise. The above voltage at the COMP pin corresponds to about 25% of full current limit.

In a boost converter, the RMS current through the internal MOSFET depends on both the input and output voltages, according to *Equation 10* (DCM) and *11* (CCM).

Equation 10

$$I_{MOS,rms} = \frac{V_{IN} \cdot D}{F_{SW} \cdot L}\sqrt{\frac{D}{3}}$$

Equation 11

$$I_{MOS,rms} = I_{OUT}\sqrt{\left(\frac{D}{(1-D)^2} + \frac{1}{12}\left(\frac{V_{OUT}}{I_{OUT} \cdot f_{SW} \cdot L}\right)^2 (D(1-D))^3\right)}$$

The current limitation works by clamping the COMP pin voltage proportionally to R_{BILIM}. The peak inductor current is limited to the above threshold decreased by the slope compensation contribution.

8.4 Current generators section

The LED-driving section consists of 16 current generators connected to the internal control logic. Each channel can sustain up to 40 V and sink up to 85 mA. The brightness of the LEDs connected to the LED7708 is controlled by switching the current between a maximum value (on-phase) and a minimum one (off-phase) at a given dimming frequency (PWM control).

The two current levels are set by connecting a resistor on both the ISETH and ISETL pins:

Equation 12

$$I_{CHX,ON} = \frac{K_H}{R_{ISETH}}$$

where K_H= 1200 V.

Equation 13

$$I_{CHX,OFF} = \frac{K_L}{R_{ISETL}}$$

where K_L= 4.0 V.

The lower level is generally used to keep the voltage across the LED string under control during the off-phase of the dimming period; if a zero-current low level is required, the ISETL pin must be connected to the device supply rail (LDO3).

The current generators of the LED7708 have been designed to be grouped (i.e. connected in parallel) if required by the application. For stability reasons, the parallelization of the current generators should be done when the programmed current is above 40 mA per channel.

The current accuracy among different devices is guaranteed to be lower than ±2% through the full output current range (20 mA-85 mA). Two current ranges are selectable in order to optimize the overall current accuracy.

Table 10 provides some typical output currents for standard E96 values.

Table 10. LED current vs. external resistor setting

Nominal LED current $I_{CHX,ON}$ [mA]	R_{ISETH} [kΩ] E96 series (1%)	Actual LED current $I_{CHX,ON}$ [mA]
85	14.3	83.9
75	16.2	74.1
60	20.0	60.0
50	24.3	49.4
40	30.1	39.9
30	40.2	29.9
20	60.4	19.9
15	80.6	14.9

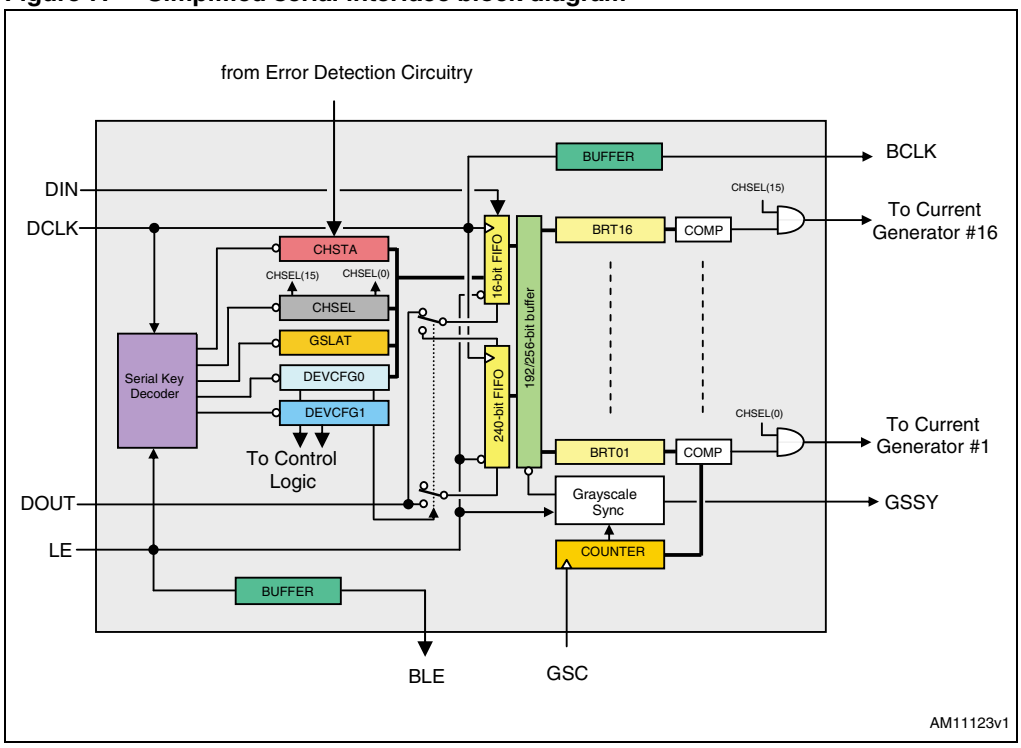
Unused channels should be disabled through the CHSEL register and can be physically left floating or shorted to ground.

8.5 Serial interface

8.5.1 Serial interface architecture

The LED7708 is equipped with a 4-wire serial interface (SI) to allow full control of its functionalities by the host controller. The LED7708 uses four pins (DIN, DOUT, DCLK and LE) to connect itself to the serial bus. The serial interface supports a data clock frequency up to 30 MHz.

Figure 7. Simplified serial interface block diagram



8.5.2 Serial interface internal registers

The internal registers are organized in control registers and brightness registers. Access to the desired register is performed by encoding the destination address via a serial key on the bus (a serial key consists of a certain number of clock pulses during the high-state of the LE signal). All the internal registers are 16 bits wide.

Table 11. Internal registers

Control registers	Brightness registers
DEVCFG0 DEVCFG1 GSLAT CHSTA CHSEL	BRT01 to BRT16

8.5.3 Internal registers access

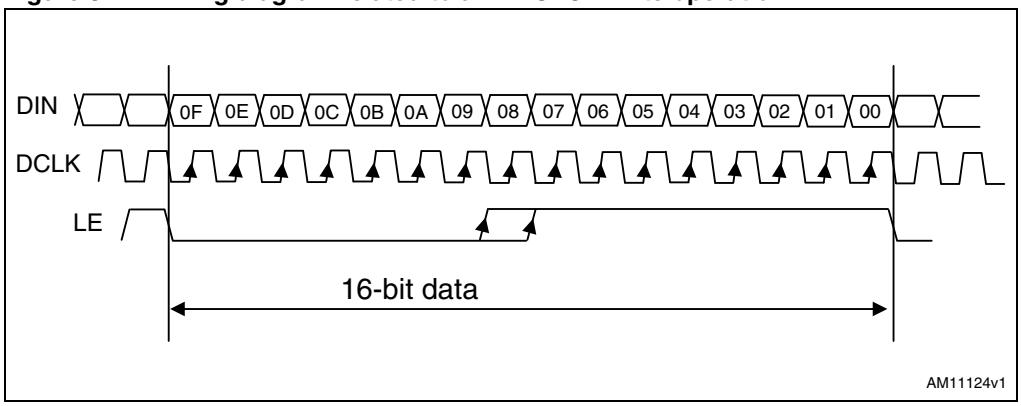
The LED7708 is capable of supporting different data formats to satisfy different application needs. The control registers are accessed one at a time by using 16-bit read/write operations, while the brightness registers can be loaded in sequence (16x16-bit) or in a single shot (1x256-bit). An additional data format (1x192-bit) allows data flow optimization when only 12 bits are used for brightness control. After the startup sequence, the 16x16-bit data format is set by default. *Figure 8* details the signal timing for a write operation to the DEVCFGx registers. *Table 12* summarizes the available operations:

Table 12. Internal register operations encoding

DCLK rising edges with LE=1	Operation
1	Data latch (BRTxx)
2-3	Global latch (BRTxx)
4-5	Write CHSEL
6-7	Read CHSTA
8-9	Write DEVCFGx(*)
10-11	Read DEVCFGx(1)
12-13	Write GSLAT

1. The content of the shift register is loaded into DEVCFG0 or DEVCFG1 according to the DEST bit (the most significant bit, common to both registers). The data bits are shifted in starting from the most significant one (MSB first).

Figure 8. Timing diagram related to a DEVCFGx write operation



8.5.4 Brightness data formats

The format for the brightness data is chosen by acting on the BDFS (brightness data format selector) and the BRLS (brightness register length selector) bits of the DEVCFG1 register.

Table 13. Brightness data formats

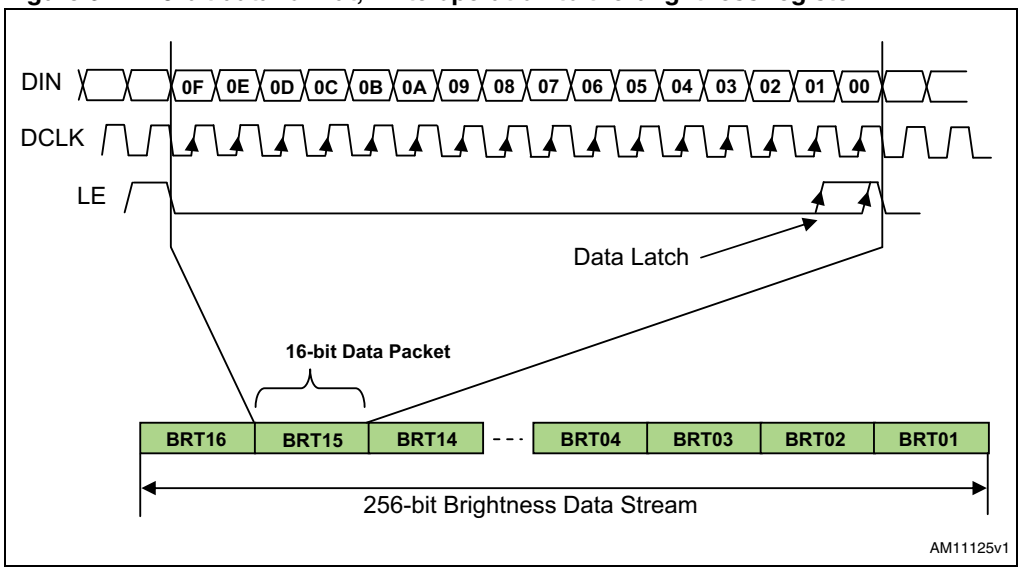
BDFS	BRLS	Brightness data format
0	0	16x16, 12-bit (the 4 most significant bits are not used)
0	1	16x16, 16-bit
1	0	192x1, 12-bit
1	1	256x1, 16-bit

16x16-bit data format (BDFS=0, BRLS=X)

The brightness registers BRT01:BRT16 are sequentially loaded at the end of 16-bit write operations. The LE is managed to encode two serial keys: one for the so called “data latch” operation and another to encode the final “global latch” operation. Therefore, a complete brightness data transfer to the LED7708 consists of 15 “data latch” operations followed by a single “global latch” operation.

If the 4096 steps (12-bit) brightness control is used (BRLS low), the four most significant bits of each brightness register are unused. The brightness registers are written from BRT16 to BRT01 with auto-decrement after each write operation (the LE signal of the last write operation to BRT01 must encode a “global latch”).

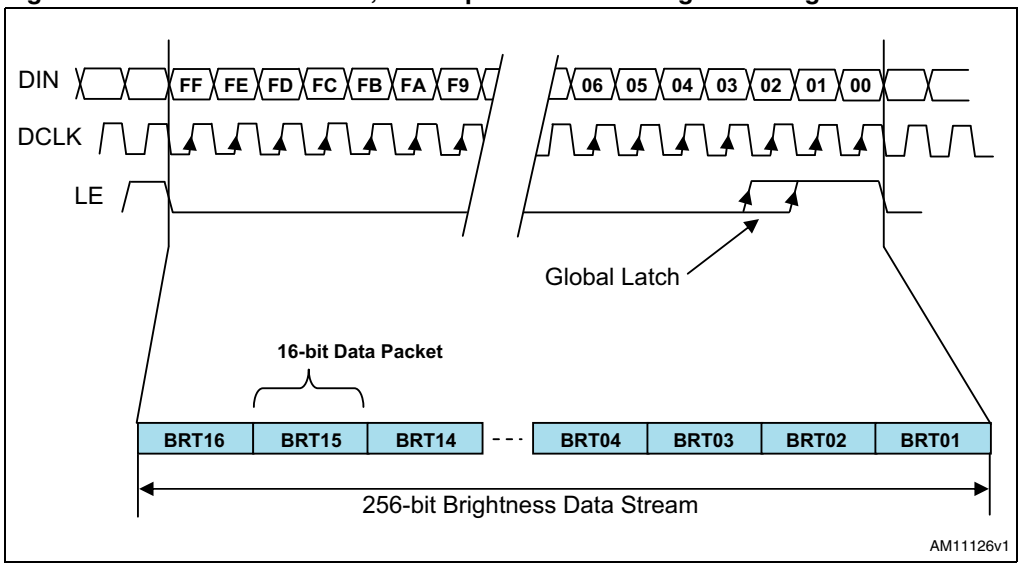
Figure 9. 16-bit data format, write operation to the brightness register



1x256-bit data format (BDFS=1, BRLS=1)

This option allows a complete brightness data transfer in a single 256-bit write operation. The brightness registers BRT01:BRT16 are simultaneously loaded at the falling edge of the LE signal. Only 65536 steps (16-bit) brightness control is supported by this data format.

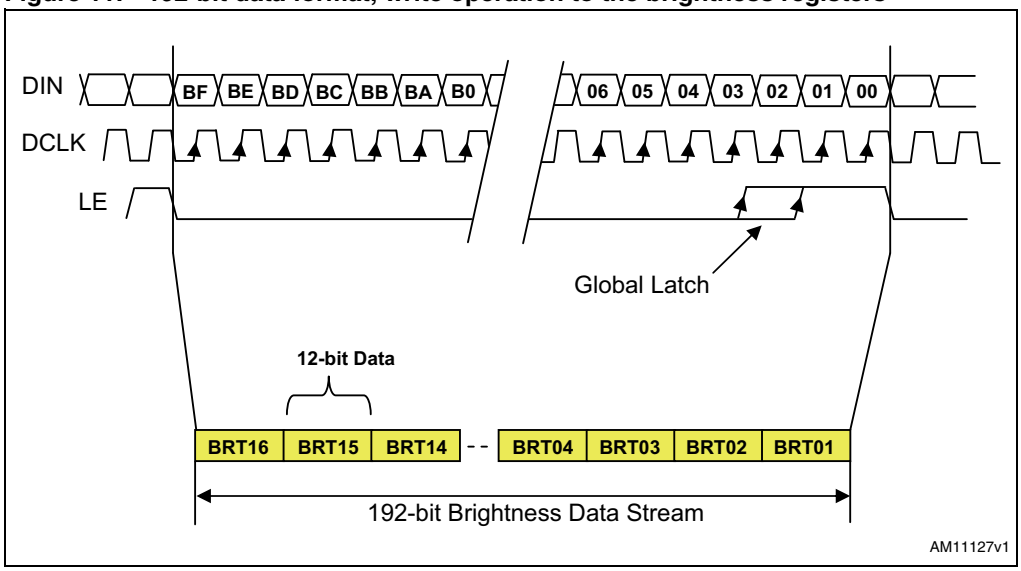
Figure 10. 256-bit data format, write operation to the brightness registers



1x192-bit data format (BDFS=1, BRLS=0)

The brightness registers BRT01:BRT16 are simultaneously loaded at the end of a single 192-bit single write operation. This option is similar to the 1x256-bit format but optimizes the serial bus communication when 12 bits only are used for the brightness control.

Figure 11. 192-bit data format, write operation to the brightness registers



Normally, the serial data coming from the DIN pin is clocked out at the DOUT pin. Optionally, the LED7708 can continuously transmit the status of the control registers when the continuous status reading (CSRD) bit of the DEVCFG0 register is asserted. In this case the device replaces (with a 16-clock-cycle delay) the received brightness data stored in the FIFO with the CHSTA, CHSEL, LATENCY, DEVCFG0 and DEVCFG1 content. This option is useful to get the device status without interrupting the brightness data flow.

The continuous status reading is available only with 1x256-bit and 1x192-bit data formats. See *Section 8.8.2* for details.

8.5.5 Brightness registers (BRTxx)

The BRT16:01 registers are 16-bit wide, write-only registers where the brightness levels, received through the serial interface, are stored. These registers may be 12 or 16 bits wide, depending on the BRLS and BDFS bits of the DEVCFG1, see *Table 15*. The LED7708 supports two brightness control options: group dimming and grayscale dimming.

The first option uses BRT01 only to set the desired brightness to all the channels, while the second one allows independent brightness level on each channel (all BRTxx registers are used). Group dimming and grayscale dimming modes are selected through the GSME bit of the DEVCFG0 register.

The PWM signals at the outputs are generated by comparing the content of the BRT16:01 registers to a 16-bit or 12-bit counter, according to BRLS and BDFS bit status. The clock source for the counter can be either external or internal, depending on the FOSC pin status. See *Section 8.6.1: Internal dimming oscillator* for details.

All the brightness registers are not directly connected to the digital comparators of the grayscale circuitry: a 256-bit buffer is used to store the value. The content of the buffer is transferred to the brightness registers at the end of the LE pulse (falling edge) or at the end of the current dimming cycle according to the selected option (See the DASS bit of the DEVCFG1 register for details).

8.5.6 DEVCFG0 register

Table 14. DEVCFG0 register

Bit	Position	Attribute	Default	Description
DEN	0	R/W	0	Device enable 0= device off 1= device on
EDMI	1	Read only	1	Error detection mode indicator 0= valid data on CHSTA 1= error detection in progress or output voltage not optimized
OVFW	2	Read only	0	Regulation DAC overflow 0= regulation DAC in range 1= regulation DAC overflow
OTAF	3	Read only	0	Overtemperature alert flag 0= die temp <120 °C 1= die temp >130 °C

Table 14. DEVCFG0 register (continued)

Bit	Position	Attribute	Default	Description
OCAD	4	R/W	0	Open channel auto disconnection 0= open channels not disconnected 1= open channels auto-disconnection
SCAD	5	R/W	0	Shorted channel auto disconnection 0= shorted channels not disconnected 1= shorted channels auto-disconnection
CFP	6	Read only	0	Critical fault protection 0= no protection occurred 1= OV or OT protection occurred
RWAS	7	R/W	0	Regulation window amplitude selection 0= 300 mV regulation window 1= 600 mV regulation window
DTS0	8	R/W	0	LED short detection threshold selection (See *Table 17*).
DTS1	9	R/W	0	
GSME	10	R/W	0	Grayscale mode enable 0= group dimming mode 1= grayscale dimming mode
CRS†	11	R/W	0	Current range selector† 0= lower current range (20 mA-45 mA) 1= upper current range (40 mA-85 mA)
OVRS	12	Read only	0	Output voltage regulation status 0= output voltage not optimized 1= output voltage optimized
OVRE	13	R/W	0	Output voltage regulation enable 0= output voltage regulation disabled 1= output voltage regulation enabled
SDMS†	14	R/W	0	Slave device mode selection† 0= no slave devices 1= slave devices connected
DEST	15	R/W	X	Destination register address 0= FIFO loaded into DEVCFG0 1= FIFO loaded into DEVCFG1

Warning: (†) In order to prevent damage to the device or to the external circuitry, these bits are locked when the DEN bit of DEVCFG0 is asserted.

8.5.7 DEVCFG1 register

Table 15. DEVCFG1 register

Bit	Position	Attribute	Default	Description
ADJ0	0	R/W	0	Current gain adjust
ADJ1	1	R/W	0	
ADJ2	2	R/W	0	
ADJ3	3	R/W	0	
ADJ4	4	R/W	0	
ADJ5	5	R/W	0	
CGRS	6	R/W	1	Current gain range selector 0= range 1 selected 1= range 2 selected See *Section 8.8.1: Current generators gain adjust*.
LAT16	7	R/W	0	Bits #16 and #17 of dimming latency (See GSLAT register)
LAT17	8	R/W	0	
BDFS	9	R/W	0	Brightness data format selector 0= 16x16-bit format 1= 1x256-bit or 1x192-bit format
BRLS	10	R/W	0	Brightness registers length selector 0= 12-bit resolution 1= 16-bit resolution
DTIN	11	R/W	0	Dimming timing inversion selector 0= dimming cycle off-phase first 1= dimming cycle on-phase first
DASS	12	R/W	0	Data synchronization selector 0= brightness data immediately updated at the falling edge of LE 1= brightness data updated at the end of the current dimming cycle
DSYS†	13	R/W	0	Dimming synchronization selector† 0= GSSY pin is pulse output 1= GSSY pin is trigger input
CSRD	14	R/W	0	Continuous status reading 0= continuous status reading disabled 1= continuous status reading enabled
DEST	15	R/W	X	Destination register address 0= FIFO loaded into DEVCFG0 1= FIFO loaded into DEVCFG1

Warning: In order to prevent damage to the device or to the external circuitry, these bits are locked when the DEN bit of DEVCFG0 is asserted.

Table 16. Available LED short detection thresholds

DTS1	DTS0	LED short-circuit detection threshold
0	0	LED short detection disabled
0	1	LED short detection threshold fixed to 3.4 V
1	0	LED short detection threshold fixed to 6.8 V
1	1	LED short detection threshold fixed to 8.4 V

8.5.8 GSLAT register

The latency is used to insert a programmable delay at the beginning of each dimming period to implement a certain amount of scanning. The scanning technique is basically a way to improve the dynamic performance of an LCD panel by powering the backlight only when the pixels are stable.

The GSLAT register is a write-only register and stores the 16 less significant bits of the dimming period latency. The additional two most significant bits are located in the DEVCFG1 register (LAT16 and LAT17 bits). Thanks to the 18-bit wide latency, the LED7708 is capable of supporting down to 20% of scanning waveform (see *Section 8.6: Dimming options* for details).

8.5.9 CHSEL register

The CHSEL register is a readable/writable configuration register. Every bit of this register allows the user to enable/disable the channels. Independent control of the channels (e.g. scrolling backlight or phase shift) can be achieved by acting on this register.

Table 17. CHSEL register

Bit	Position	Attribute	Meaning
CHSEL0 to CHSEL15	0	R/W	1= the corresponding channel is active. 0= the corresponding channel is disabled.
	1		
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12		
	13		
	14		
	15		

8.5.10 CHSTA register

The CHSTA register is a read only status register. Each bit of this register shows the status of the corresponding channel. After the error detection sequence takes place, the channels which have an excessive voltage drop (LED short-circuit) or that are unable to regulate the nominal current (open channels) are tagged as faulty and the related CHSTA bits are asserted.

The CHSEL register is not affected by the error detection sequence. The channels disabled by clearing the corresponding bits of the CHSEL register are not involved in the error detection and the corresponding bits of the CHSTA register are forced low. The CHSTA register is automatically overwritten during subsequent error detection occurrences.

Table 18. CHSTA register

Bit	Position	Attribute	Meaning
CHSTA0 to CHSTA15	0	Read only	0= The channel is working properly or is not used (the corresponding CHSEL bit is cleared) 1= The channel is open or an LED short-circuit has been detected during the error detection sequence
	1		
	2		
	3		
	4		
	5		
	6		
	7		
	8		
	9		
	10		
	11		
	12		
	13		
	14		
	15		

If at least one bit of the CHSTA register is asserted after the error detection sequence, the XFLT pin is tied low. Both the CHSTA register and the XFLT pin are reset by clearing the DEN bit of DEVCFG0 or by performing a POR.

8.5.11 Internal registers initialization

The internal registers show the following configuration after a POR.

Table 19. Default configuration of internal registers after POR

Register	Value (binary)
DEVCFG0	0000 0000 0000 0010
DEVCFG1	0000 0000 0100 0000
GSLAT	0000 0000 0000 0000
BRTxx	0000 0000 0000 0000
CHSEL	0000 0000 0000 0000
CHSTA	0000 0000 0000 0000

The content of the internal registers, except the read-only bits of DEVCFG0 and DEVCFG1 (i.e. CFP, OVRS, OVFW and EDMI), is not affected when the DEN bit is cleared.

Warning: In order to prevent damage to the device or to the external circuitry, some bits of DEVCFG0 and DEVCFG1 registers (CRS, SDMS and DSYS) are locked when DEN is high.

8.6 Dimming options

The brightness of the LEDs connected to the output channels can be basically controlled in two ways, depending on the status of the GSME bit of the DEVCFG1 register:

- Group dimming mode (GSME=0): common dimming performed by using the brightness value received through the serial interface and stored in the BRT01 register: all the channels have the same PWM duty cycle;
- Grayscale dimming mode (GSME=1): independent PWM dimming on each channel performed by loading the BRT01:BRT16 brightness registers.

In practice, a third way to control the brightness of the LEDs should rely on an intensive use of the CHSEL register by the host controller. The direct control of the CHSEL register, combined with either the group dimming or the grayscale dimming, allows the user to implement particular dimming algorithms.

Once the dimming control mode has been chosen through the GSME bit, the source of the clock for the PWM generation (grayscale clock) must be selected. The LED7708 can use either an external clock source or its internal high-frequency oscillator.

8.6.1 Internal dimming oscillator

The LED7708 has a programmable oscillator dedicated to the dimming circuitry.

The output clock is provided at the GSCK pin for the slave devices. If the FOSC pin is forced high, the oscillator is turned off and the GSCK pin becomes the grayscale clock input.

Table 20. FOSC pin setting options

FOSC pin setting	Oscillator	GSCK pin function
High (to LDO3)	OFF	Grayscale clock input
Resistor to GND	Active (4 MHz-25 MHz)	Grayscale clock output

The oscillator frequency is simply set by connecting a resistor between the FOSC pin and ground:

Equation 14

$$f_{GSCK} = \frac{K_{OSC}}{R_{FOSC}}$$

Equation 15

$$f_{DIM} = \frac{f_{OSC}}{2^N}$$

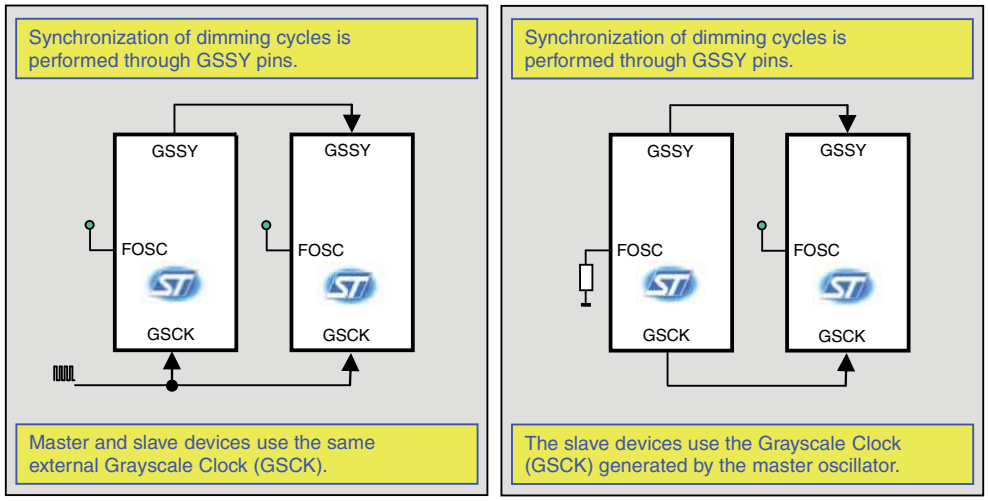
Table 21. Function of pins involved in dimming control

Pin	Function
GSCK	Input or output, depending on FOSC pin status; FOSC high: grayscale clock input, internal oscillator disabled. FOSC to resistor: grayscale clock output. The clock, internally generated by the dimming oscillator, is provided at this pin.
FOSC	Internal oscillator frequency setting. See above.
GSSY	Input or output pin, depending on DSYS bit value. Used for dimming synchronization. See *Table 21*.

Table 22. Dimming synchronization control

DSYS	Dimming sync selector (locked if DEN is asserted)
0	The GSSY pin is set as output and provides a pulse at the end of each dimming cycle. The device continuously performs a latency+dimming sequence.
1	The GSSY pin is set as input. The ongoing dimming sequence is reset as soon as a rising edge on the GSSY input is detected; a new latency+dimming cycle is triggered by the falling edge on this pin.

Figure 12. Dimming signals and synchronization

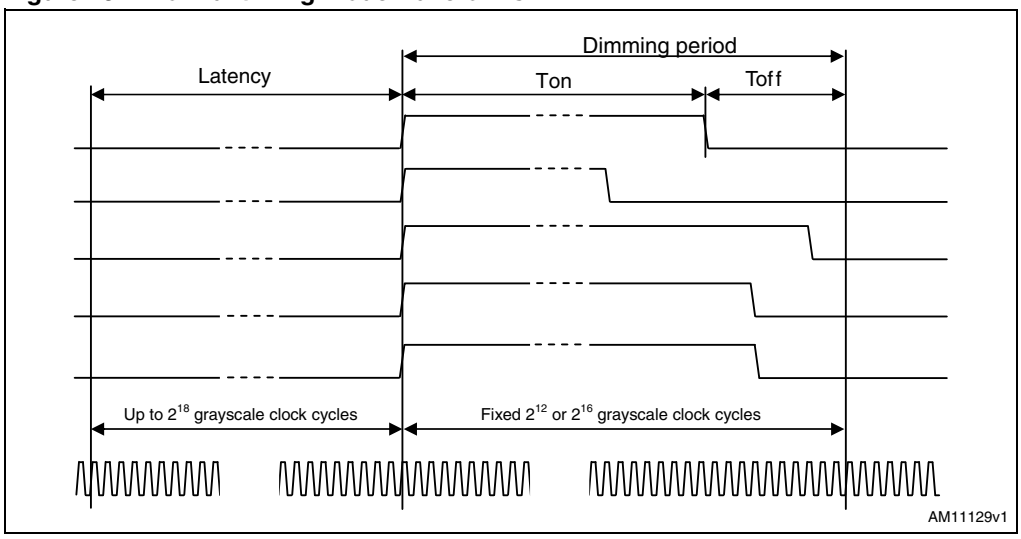


8.6.2 Dimming waveforms

Normal dimming mode

In normal timing mode the basic cycle is represented by a latency period followed by a dimming period starting with the on-phase (current generators active). This option is selected by clearing the DTIN (dimming timing inversion) bit of the DEVCGF1 register.

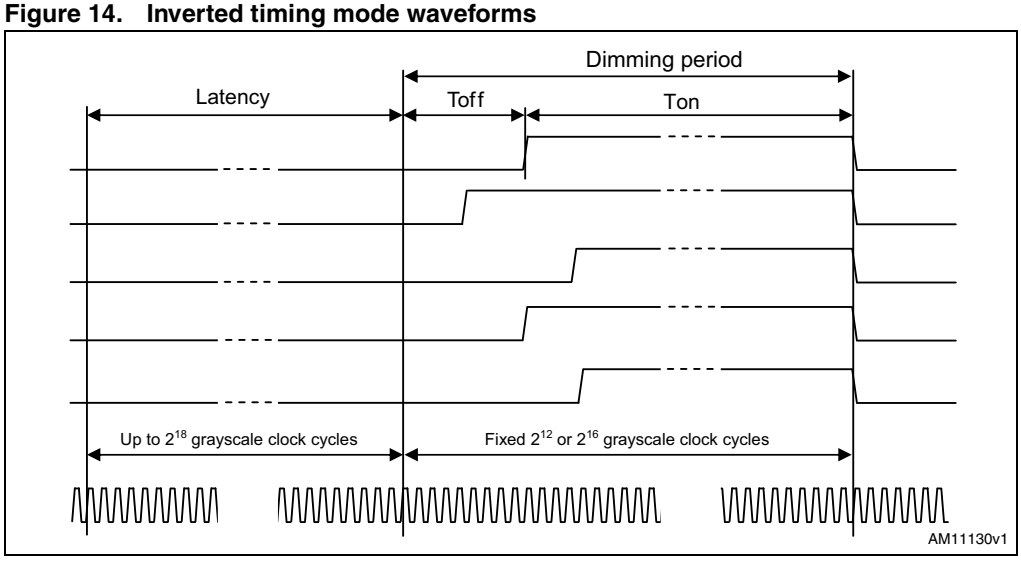
Figure 13. Normal timing mode waveforms



Inverted dimming mode

In inverted dimming mode, the basic cycle is represented by a latency period followed by a dimming period starting with the off-phase (current generators turned off). This option, normally used when a common turn-off is required, is selected by asserting the DTIN (dimming timing inversion) bit of the DEVCGF1 register.

Figure 14. Inverted timing mode waveforms

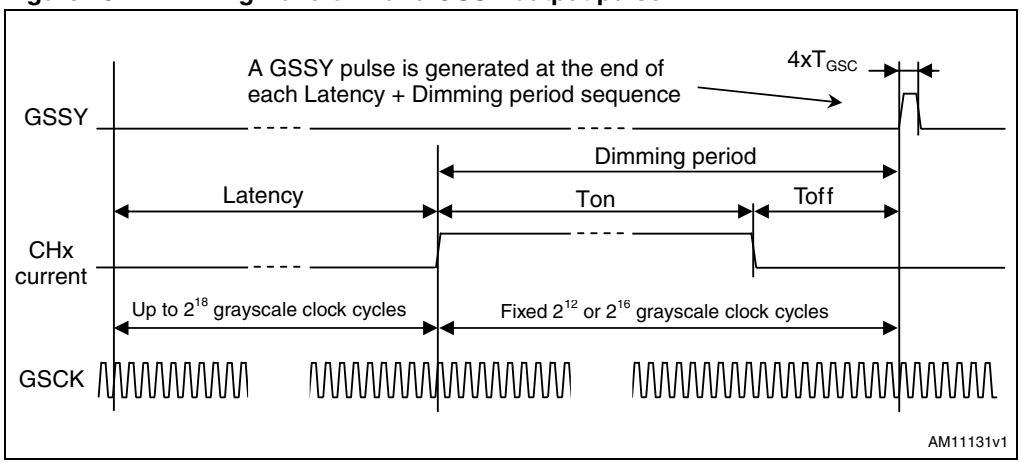


8.6.3 Grayscale synchronization

Grayscale sync (GSSY) used as synchronization output

When the DSYS bit of the DEVCFG1 register is set low, the GSSY pin of the LED7708 is set as output. A $4xT_{GSC}$ high level pulse is provided at the GSSY pin at the end of each dimming cycle (latency followed by a dimming period).

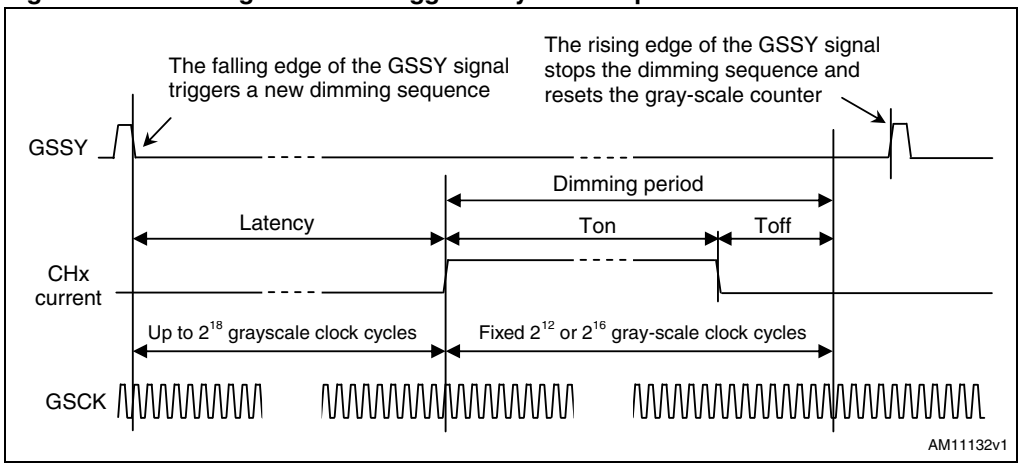
Figure 15. Dimming waveform and GSSY output pulse



Grayscale sync (GSSY) used as synchronization input

When the DSYS bit of the DEVCFG1 register is set high, the GSSY pin of the LED7708 is set as input. This option can be used to lock the dimming cycles (latency followed by a dimming period) to the vertical sync signal (VSYNC) coming from the video processor. The minimum pulse duration is $2xT_{GSC}$. As soon as the GSSY signal goes high, the ongoing dimming sequence is stopped and the grayscale counter is reset. A new dimming sequence is triggered when the GSSY pin goes low.

Figure 16. Dimming waveform triggered by GSSY input



8.7 Fault management

The LED7708 includes some protection to prevent damage to itself and to the backlight. In order to satisfy these requirements, the following protection has been implemented:

Table 23. Detected faulty conditions

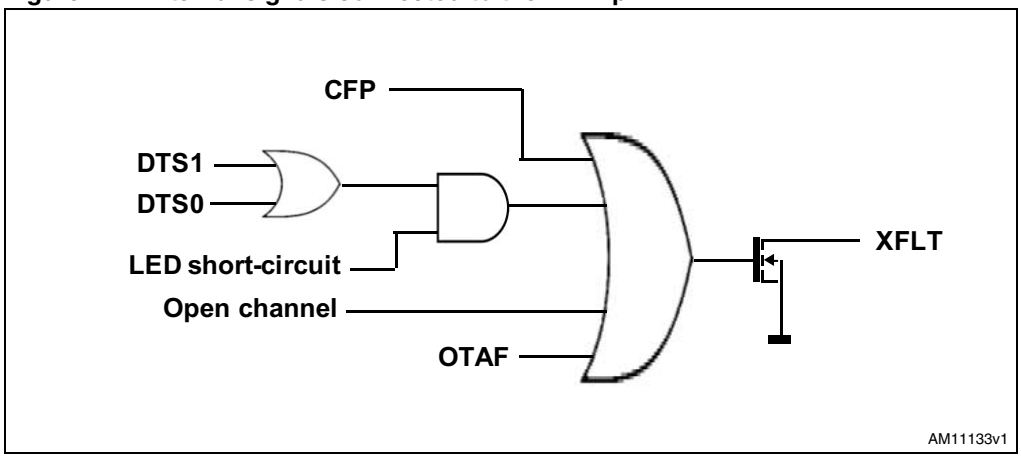
Faulty Condition	Involved Section
Boost output overvoltage (OV)	Boost controller
External MOSFET overcurrent (OC)	
Open channel	Current generators
Excessive channel voltage (LED short-circuit)	
Overtemperature protection	Whole device

The XFLT pin is an open drain output (active low) and is affected by the following faulty conditions:

Table 24. XFAULT pin behavior

Detected fault	Involved flag	XFLT status
Overvoltage protection	OVPF	Low
Overtemperature alert	OTAF	Low
Open channel	CHSTA16:CHSTA01	Low
LED short-circuit	CHSTA16:CHSTA01	Low

Figure 17. Internal signals connected to the XFLT pin



8.7.1 Overvoltage protection

The LED7708 protects itself and the external components from excessive output voltage by monitoring the voltage at the VFB pin. The overvoltage threshold is given by the following equation, where R1 and R2 are the resistors of the output divider:

Equation 16

$$V_{OUT,OVP} = \frac{R_1 + R_2}{R_2} \cdot V_{FB,OV}$$

Once the voltage at the VFB pin has crossed the related threshold, the LED7708 shuts down, the CFP (critical fault protection) flag of the DEVCFG0 register is asserted, the XFLT pin is set low and the condition is latched.

Normal operation is restored by toggling the DEN bit of the DEVCFG0 register or by performing a POR.

8.7.2 Overtemperature alert and thermal protection

The LED7708 implements a two-level thermal protection. When the junction temperature rises above 130 °C (typ.), the overtemperature alert flag (OTAF) is asserted and the XFLT pin goes low. The OTAF flag is cleared as soon as the chip temperature drops below 125 °C (typ.). This bit is used by the host controller to enable output voltage regulation if temporarily disabled.

If the temperature of the chip crosses 150 °C, the device shuts down. Automatic restart occurs as soon as the temperature drops to 130 °C.

8.7.3 Overcurrent protection

Overcurrent occurring in the power MOSFET is managed by skipping subsequent switching cycles until the faulty condition is present. The XFLT pin is not affected. See also *Section 8.3.3* for details.

8.7.4 LED short-circuit and open channel faults

The faults that can occur to the current generators section are basically the following:

- one or more open (floating) channels
- excessive voltage drop (shorted LEDs).

The LED7708 manages these faulty conditions following a particular algorithm.

When a channel opens, its voltage drop falls to zero: the output voltage regulation circuitry tags it as “probably faulty” and increases the output voltage. If the “open” condition is temporary, the voltage drop across the generator is self-recovered and the output voltage is corrected. In case of a real open channel, the regulation DAC reaches the maximum value (DAC overflow) and the OVFW bit of the DEVCFG0 register is asserted.

The LED7708 can automatically disconnect the open channels if required. Therefore, if the open channels auto-disconnection (OCAD) bit of the DEVCFG0 register is asserted, the faulty channel is suddenly turned off, excluded from the regulation loop and the output voltage is quickly adjusted to the optimal level. During the open channel detection (i.e. when the regulation DAC is rolling up), the LED short-circuit detection circuitry is masked to avoid false detection due to the high output voltage.

If the OCAD bit is cleared, the output voltage is kept to the maximum value and the fault management is demanded to the host controller (XFLT pin low).

In case of LED short-circuit, the voltage across the related channel increases. The LED7708 compares the drop across each channel with a fixed threshold in order to detect this

condition. Four options can be chosen by acting on the DTS1:DTS0 bits of the DEVCFG0 register (see *Table 16*).

To prevent false triggering, the LED short-circuit detection is masked if the output voltage is out of regulation (i.e. the OVRS bit of the DEVCFG0 is low). Each channel detected as faulty (open or shorted) sets the corresponding bit of the CHSTA register.

The fault management algorithm can operate only if the channels are active and at a minimum (10 µs typ.) PWM on-time is required at the outputs in order to detect the faulty condition. After the detection of a “probably open channel”, the device begins to ramp-up the output voltage, but this operation cannot be performed if the involved channel is turned off (no feedback information available). In this case, the algorithm should wait until the channel is turned on again, leading to a delayed output voltage steering because of the dimming function. This situation can induce excessive power dissipation on the other channels (high-voltage drop for a long period). To prevent this, the LED7708 automatically forces the “probably open channel” to remain on (regardless of its programmed status) until the maximum output voltage has been reached (confirmation of open channel fault) or the output current has been recovered. Once the algorithm has recognized the open condition, the faulty channel is excluded from the regulation loop and the output voltage is quickly decreased to the optimal value in order to avoid excessive power dissipation (only if the OCAD bit is asserted). Therefore, the open channel/LED-short fault detection algorithm can operate in a transparent way without the need to stop the dimming function.

8.8 Special function

8.8.1 Current generators gain adjust

The gain of the current generators can be varied by changing the ADJ5:ADJ0 bits of the DEVCFG1 register (64 steps). Two selectable ranges are provided by asserting/clearing the current gain range selector (CGRS) bit of the DEVCFG1 register. After POR, the current gain is unitary and can be changed according to the following formulas:

Equation 17

$$G_{CGRS=1} = 1 + G_D \cdot \frac{0.5}{64}$$

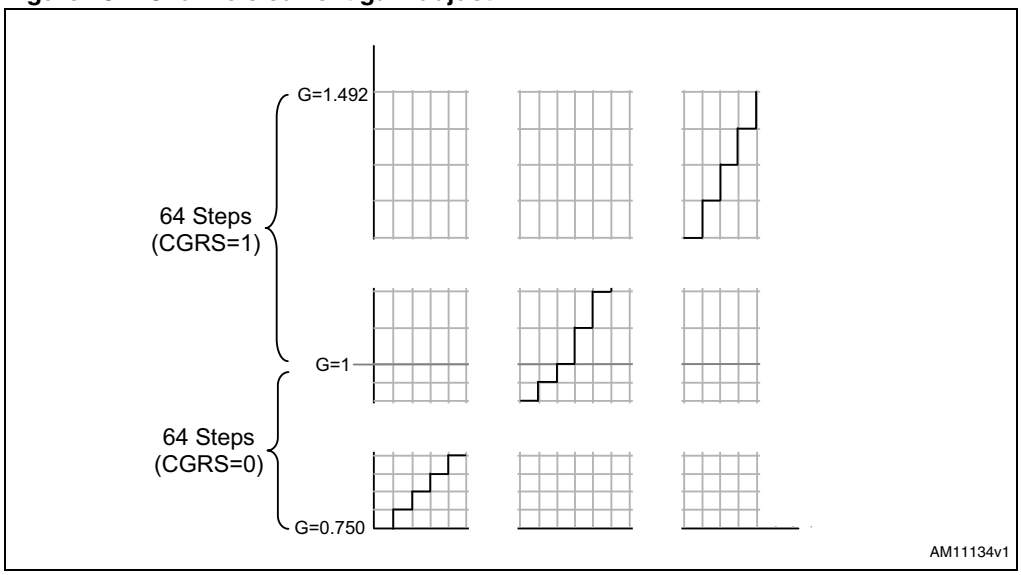
Equation 18

$$G_{CGRS=0} = 0.75 + G_D \cdot \frac{0.25}{64}$$

Equation 19

$$G_D = ADJ5x2^5 + ADJ4x2^4 + ADJ3x2^2 + ADJ2x2^2 + ADJ1x2 + ADJ0$$

Figure 18. Channels current gain adjust



8.8.2 Continuous status reading

The continuous status-reading is a feature that allows the content of the internal registers to be obtained without stopping the brightness data flow. The content of the DEVCFG0, DEVCFG1, CHSEL, CHSTA and GSLAT is automatically loaded into the FIFO after the brightness data has been moved to the buffer. This feature is supported in 1x1256-bit and 1x192-bit data formats only.

Figure 19. Continuous reading mode disabled, 1x256-bit data format

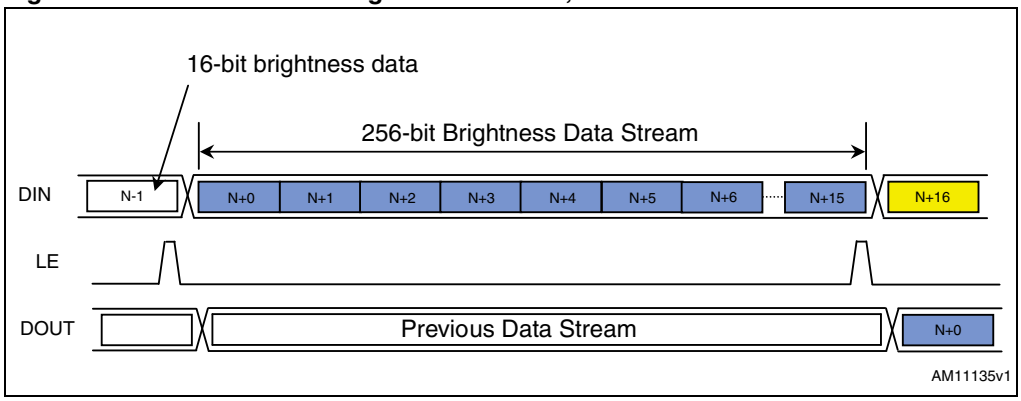
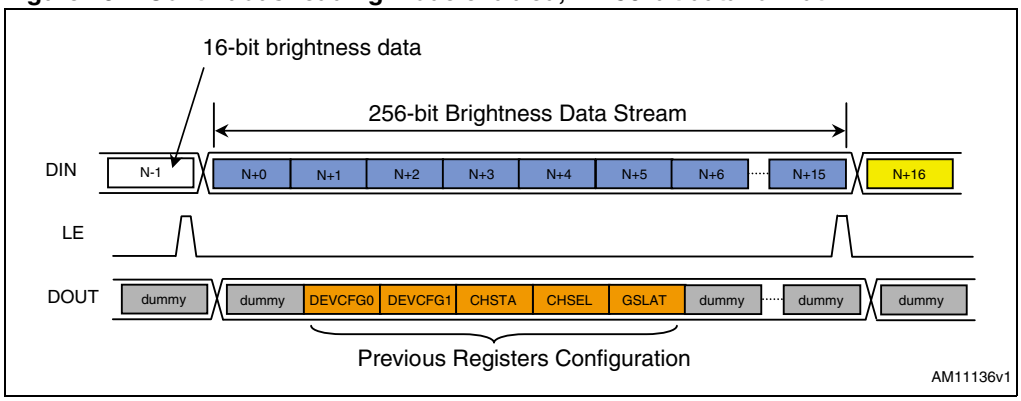


Figure 20. Continuous reading mode enabled, 1x256-bit data format



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 25. VFQFPN48 (7 x 7 x 1.0 mm.) package mechanical data

Dim.	(mm.)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1		0.02	0.05
A2		0.65	1.00
A3		0.25	
b	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd		0.08	

Figure 21. VFQFPN48 (7 x 7 x 1.0 mm.) package outline

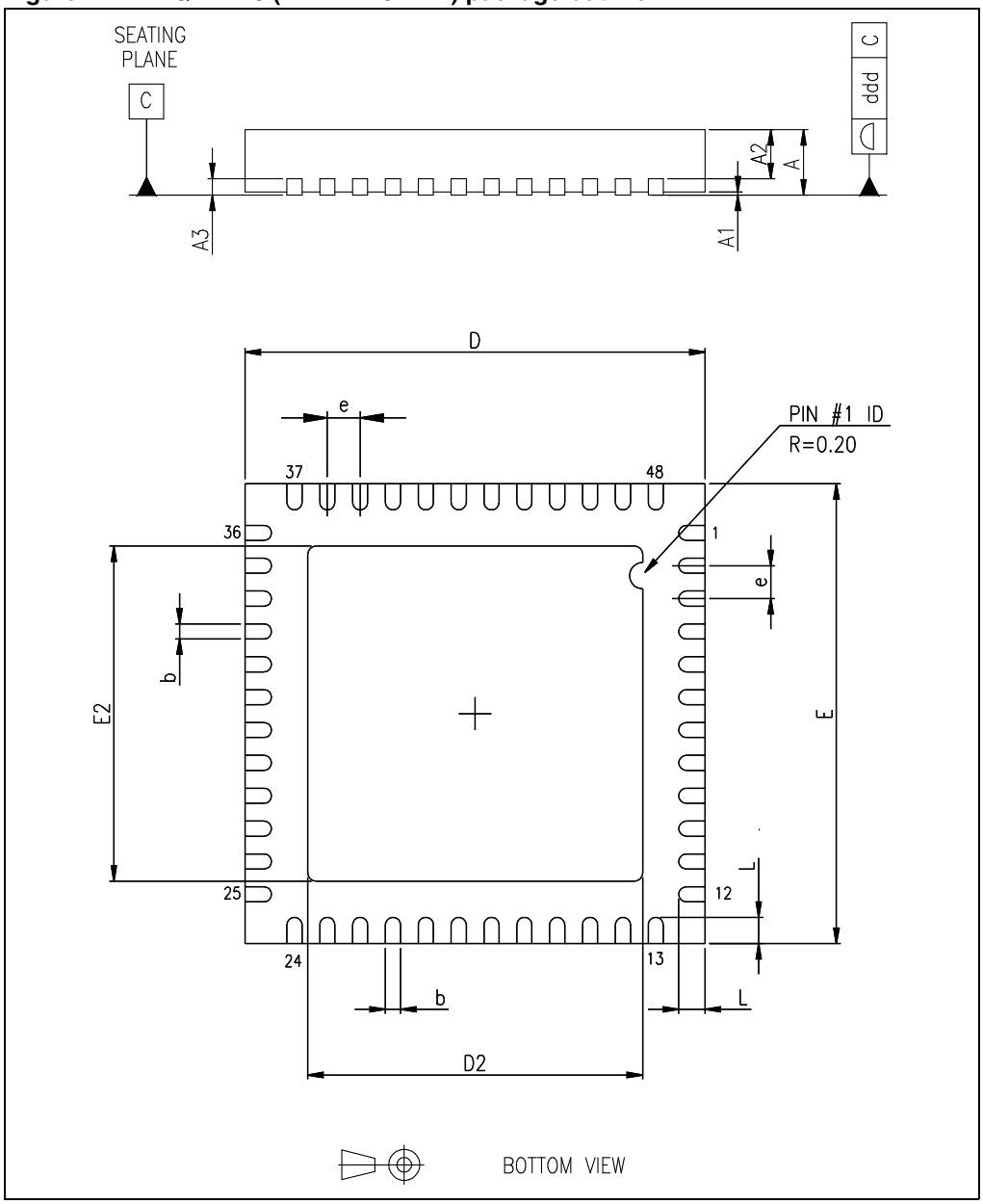
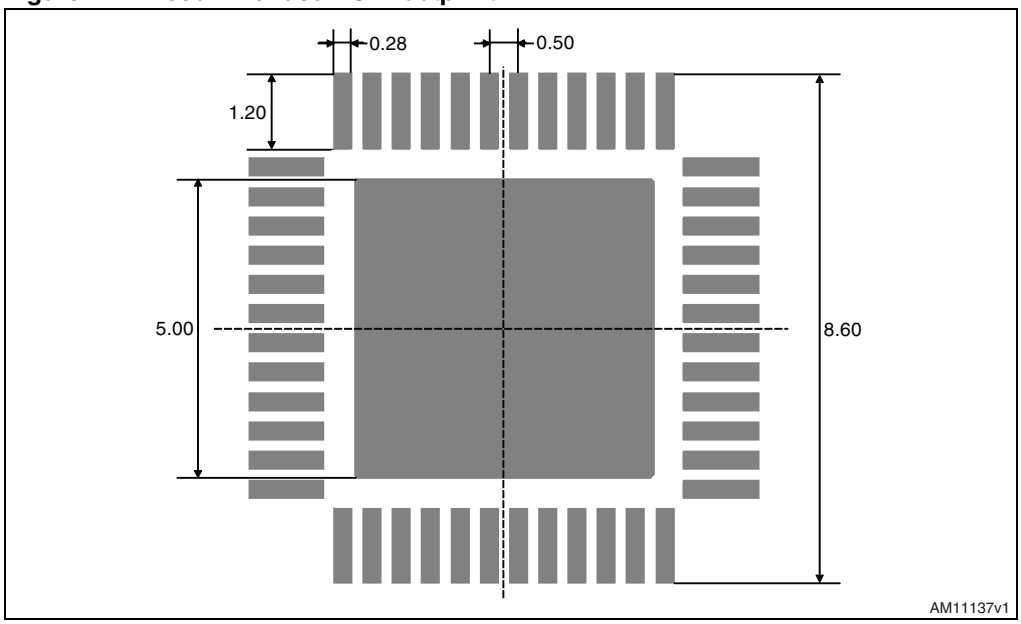


Figure 22. Recommended PCB footprint



10 Revision history

Table 26. Document revision history

Date	Revision	Changes
07-May-2012	1	Initial release.

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