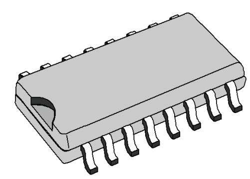
HVLED815PF

Offline LED driver with primary-sensing and high power factor up to 15 W

Datasheet — production data

Features

- High power factor capability (> 0.9)
- 800 V, avalanche rugged internal 6 Ω Power MOSFET
- Internal high-voltage startup
- Primary sensing regulation (PSR)
- +/- 5% accuracy on constant LED output current
- Quasi-resonant (QR) operation
- Optocoupler not needed
- Open or short LED string management
- Automatic self supply



SO16N

Table 1. Device summary

Order code	Package	Packaging
HVLED815PF	SO16N	Tube
HVLED815PFTR		Tape & Reel

Applications

- AC-DC LED driver bulb replacement lamps up to 15 W, with high power factor
- AC-DC LED drivers up to 15 W

Description

The HVLED815PF is a high-voltage primary switcher intended for operating directly from the rectified mains with minimum external parts and enabling high power factor (> 0.90) to provide an efficient, compact and cost effective solution for LED driving. It combines a high-performance low-voltage PWM controller chip and an 800 V, avalanche-rugged Power MOSFET, in the same package. There is no need for the optocoupler thanks to the patented primary sensing regulation (PSR) technique. The device assures protection against LED string fault (open or short).

This is information on a product in full production. www.st.com

Contents

1 Principle application circuit and block diagram

1.1 Principle application circuit

Figure 1. Principle application circuit for high power factor LED driver

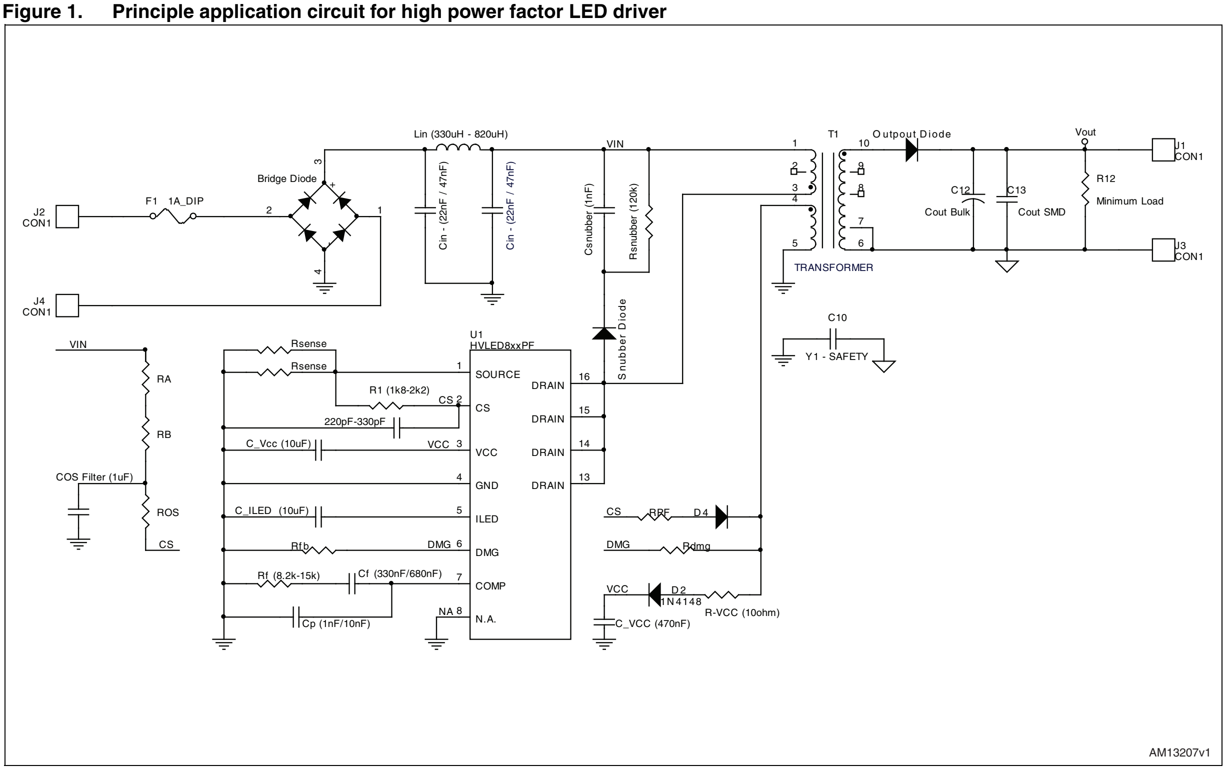
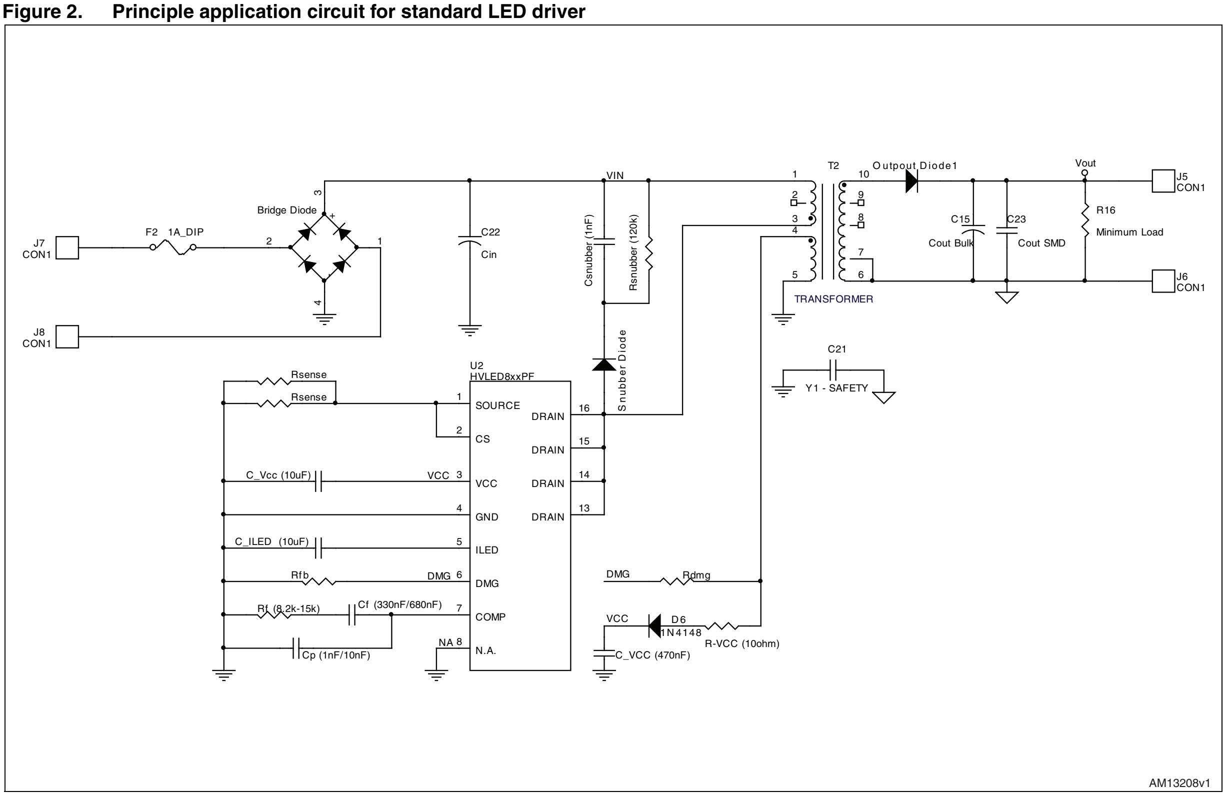
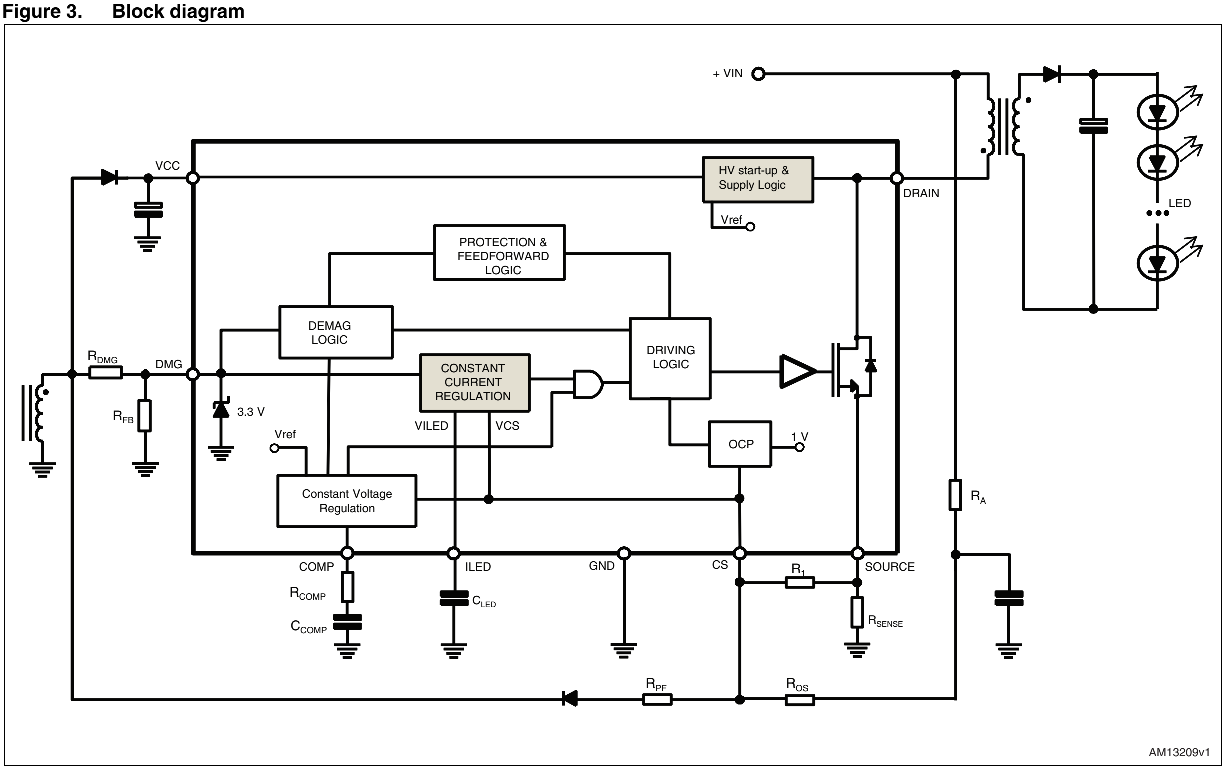


Figure 2. Principle application circuit for standard LED driver



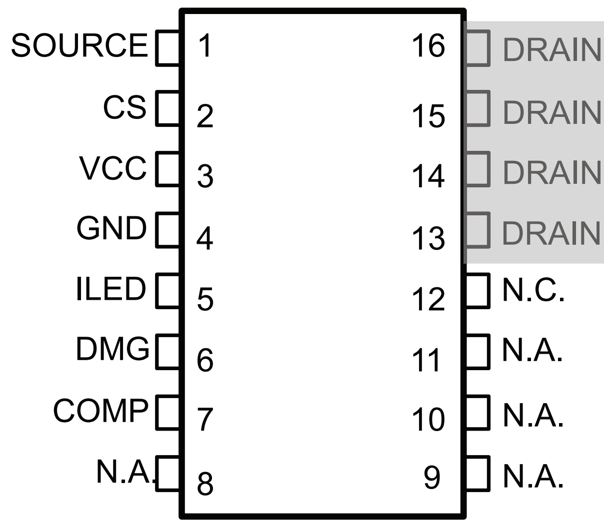
1.2 Block diagram

Figure 3. Block diagram



2 Pin description and connection diagrams

Figure 4. Pin connection (top view)



2.1 Pin description

Table 2. Pin description

N.	Name	Function
1	SOURCE	Source connection of the internal power section.
2	CS	Current sense input. Connect this pin to the SOURCE pin (through an R1 resistor) to sense the current flowing in the MOSFET through an R_{SENSE} resistor connected to GND. The CS pin is also connected through dedicated ROS, RPF resistors to the input and auxiliary voltage, in order to modulate the input current flowing in the MOSFET according to the input voltage and therefore achieving a high power factor. See dedicated section for more details. The resulting voltage is compared with the voltage on the ILED pin to determine MOSFET turn-off. The pin is equipped with 250 ns blanking time after the gate-drive output goes high for improved noise immunity. If a second comparison level located at 1 V is exceeded, the IC is stopped and restarted after V_{CC} has dropped below 5 V.
3	VCC	Supply voltage of the device. A capacitor, connected between this pin and ground, is initially charged by the internal high-voltage startup generator; when the device is running, the same generator keeps it charged in case the voltage supplied by the auxiliary winding is not sufficient. This feature is disabled in case a protection is tripped. A small bypass capacitor (100 nF typ.) to GND may be useful to get a clean bias voltage for the signal part of the IC.

Table 2. Pin description (continued)

N.	Name	Function
4	GND	Ground. Current return for both the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to a trace going to this pin and kept separate from any pulsed current return.
5	ILED	Constant current (CC) regulation loop reference voltage. An external capacitor C_{LED} is connected between this pin and GND. An internal circuit develops a voltage on this capacitor that is used as the reference for the MOSFET's peak drain current during CC regulation. The voltage is automatically adjusted to keep the average output current constant.
6	DMG	Transformer demagnetization sensing for quasi-resonant operation and output voltage monitor. A negative-going edge triggers the MOSFET turn-on, to achieve quasi-resonant operation (zero voltage switching). The pin voltage is also sampled-and-held right at the end of transformer demagnetization to get an accurate image of the output voltage to be fed to the inverting input of the internal, transconductance-type, error amplifier, whose non-inverting input is referenced to 2.5 V. The maximum I_{DMG} sunk/sourced current must not exceed ± 2 mA (AMR) in all the Vin range conditions. No capacitor is allowed between the pin and the auxiliary transformer.
7	COMP	Output of the internal transconductance error amplifier. The compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the voltage control loop.
8	N.a.	Not available. These pins must be connected to GND.
9-11	N.a.	Not available. These pins must be left not connected.
12	N.c.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
13 to 16	DRAIN	Drain connection of the internal power section. The internal high-voltage startup generator sinks current from this pin as well. Pins connected to the internal metal frame to facilitate heat dissipation.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
R_{thJP}	Thermal resistance, junction-to-pin	10	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	110	°C/W
P_{TOT}	Maximum power dissipation at T_A = 50 °C	0.9	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Junction temperature range	-40 to 150	°C

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{DS}	1, 13-16	Drain-to-source (ground) voltage	-1 to 800	V
I_D	1, 13-16	Drain current [1]	1	A
Eav	1, 13-16	Single pulse avalanche energy ($Tj = 25\ °C$, $I_D = 0.7\ A$)	50	mJ
V_{CC}	3	Supply voltage (Icc < 25 mA)	Self limiting	V
I_{DMG}	6	Zero current detector current	±2	mA
V_{CS}	2	Current sense analog input	-0.3 to 3.6	V
Vcomp	7	Analog input	-0.3 to 3.6	V

1. Limited by maximum temperature allowed.

3.2 Electrical characteristics

Table 5. Electrical characteristics[1] [2]

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power section						
$V_{(BR)DSS}$	Drain-source breakdown	$I_D < 100\ \mu A$; $Tj = 25\ °C$	800			V
I_{DSS}	OFF-state drain current	$V_{DS} = 750\ V$; $Tj = 125\ °C$ [3] See *Figure 5*			80	µA
$R_{DS(on)}$	Drain-source ON-state resistance	Id = 250 mA; Tj = 25 °C		6	7.4	Ω
		Id = 250 mA; Tj = 125 °C [3]			14.8	
C_{OSS}	Effective (energy-related) output capacitance	[3] See *Figure 6*				
High-voltage startup generator						
V_{START}	Min. drain start voltage	$I_{charge} < 100\ \mu A$	40	50	60	V
I_{CHARGE}	V_{CC} startup charge current	$V_{DRAIN} > V_{Start}$; $V_{CC}<V_{CCOn}$ Tj = 25 °C	4	5.5	7	mA
		$V_{DRAIN} > V_{Start}$; $V_{CC}<V_{CCOn}$	+/- 10%			
$V_{CC\_RESTART}$	V_{CC} restart voltage (V_{CC} falling)	[4]	9.5	10.5	11.5	V
		After protection tripping		5		

Table 5. Electrical characteristics[1] [2] (continued)

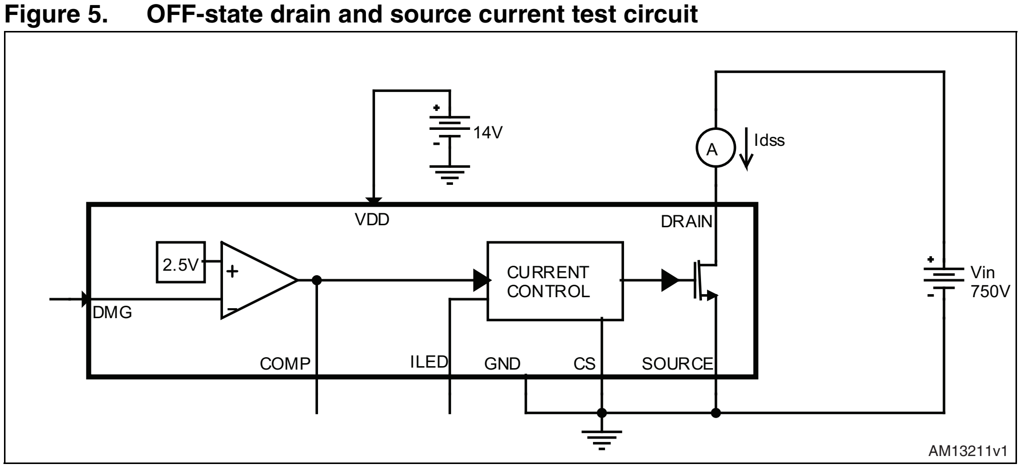
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	11.5		23	
V_{CC_ON}	Turn-on threshold	[4]	12	13	14	V
V_{CC_OFF}	Turn-off threshold	[4]	9	10	11	V
V_Z	Internal Zener voltage	Icc = 20 mA	23	25	27	V
Supply current						
$I_{CC\_START-UP}$	Startup current	See *Figure 7*		200	300	µA
Iq	Quiescent current	See *Figure 8*		1	1.4	mA
I_{CC}	Operating supply current at 50 kHz	See *Figure 9*		1.4	1.7	mA
$Iq_{(fault)}$	Fault quiescent current	See *Figure 10*		250	350	µA
Startup timer						
T_{START}	Start timer period		105	140	175	µs
$T_{RESTART}$	Restart timer period during burst mode		420	500	700	µs
Demagnetization detector						
I_{Dmgb}	Input bias current	V_{DMG} = 0.1 to 3 V		0.1	1	µA
V_{DMGH}	Upper clamp voltage	I_{DMG} = 1 mA	3.0	3.3	3.6	V
V_{DMGL}	Lower clamp voltage	I_{DMG} = - 1 mA	-90	-60	-30	mV
V_{DMGA}	Arming voltage	Positive-going edge	100	110	120	mV
V_{DMGT}	Triggering voltage	Negative-going edge	50	60	70	mV
T_{BLANK}	Trigger blanking time after MOSFET turn-off	$V_{COMP} \geq 1.3$ V		6		µs
		V_{COMP} = 0.9 V		30		
Line feedforward						
R_{FF}	Equivalent feedforward resistor	I_{DMG} = 1 mA		45		Ω
Transconductance error amplifier						
V_{REF}	Voltage reference	Tj = 25 °C	2.45	2.51	2.57	V
		[3] Tj = -25 to 125 °C and V_{CC} = 12 V to 23 V	2.4		2.6	
gm	Transconductance	$\Delta I_{COMP} = \pm 10$ µA V_{COMP} = 1.65 V	1.3	2.2	3.2	ms
Gv	Voltage gain	[5] Open loop		73		dB
GB	Gain-bandwidth product	[5]		500		KHz

Table 5. Electrical characteristics(1) (2) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{COMP}	Source current	V_{DMG} = 2.3 V, V_{COMP} = 1.65 V	70	100		µA
	Sink current	V_{DMG} = 2.7 V, V_{COMP} = 1.65 V	400	750		µA
V_{COMPH}	Upper COMP voltage	V_{DMG} = 2.3 V		2.7		V
V_{COMPL}	Lower COMP voltage	V_{DMG} = 2.7 V		0.7		V
V_{COMPBM}	Burst-mode threshold			1		V
Hys	Burst-mode hysteresis			65		mV
Current reference						
V_{ILEDx}	Maximum value	V_{COMP} = V_{COMPL}	1.5	1.6	1.7	V
V_{CLED}	Current reference voltage		0.192	0.2	0.208	V
Current sense						
t_{LEB}	Leading-edge blanking	(5)		330		ns
T_D	Delay-to-output (H-L)			90	200	ns
V_{CSx}	Max. clamp value	(4) dVcs/dt = 200 mV/µs	0.7	0.75	0.8	V
V_{CSdis}	Hiccup-mode OCP level	(4)	0.92	1	1.08	V

1. V_{CC}=14 V (unless otherwise specified).
2. Limits are production tested at Tj=Ta=25 °C, and are guaranteed by statistical characterization in the range Tj -25 to +125 °C.
3. Not production tested, guaranteed statistical characterization only.
4. Parameters tracking each other (in the same section).
5. Guaranteed by design.

Figure 5. OFF-state drain and source current test circuit



Note: The measured IDSS is the sum between the current across the startup resistor and the effective MOSFET's OFF-state drain current.

Figure 6. COSS output capacitance variation

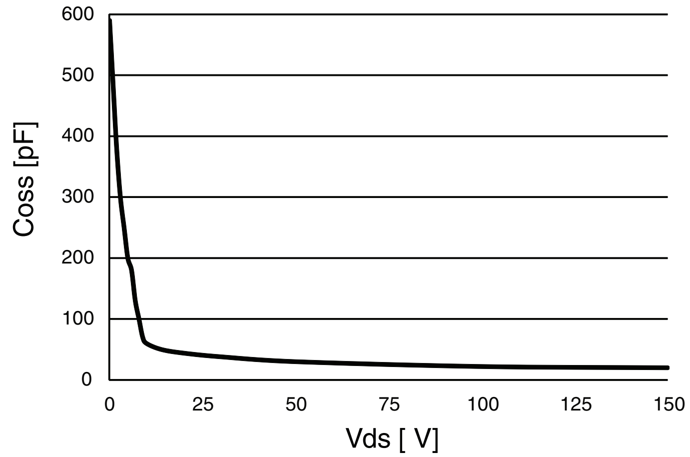


Figure 7. Startup current test circuit

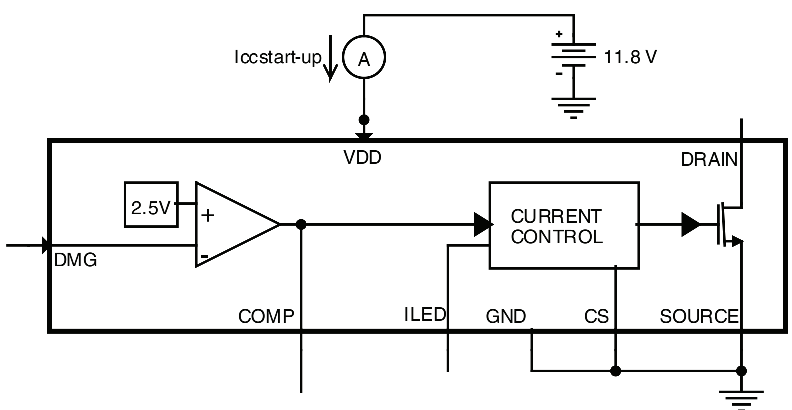
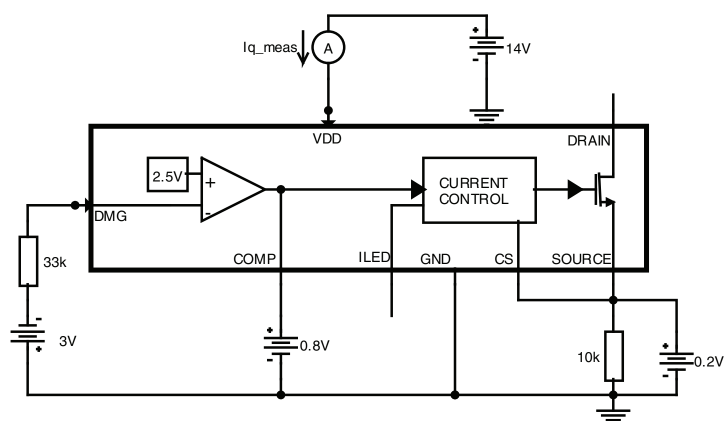
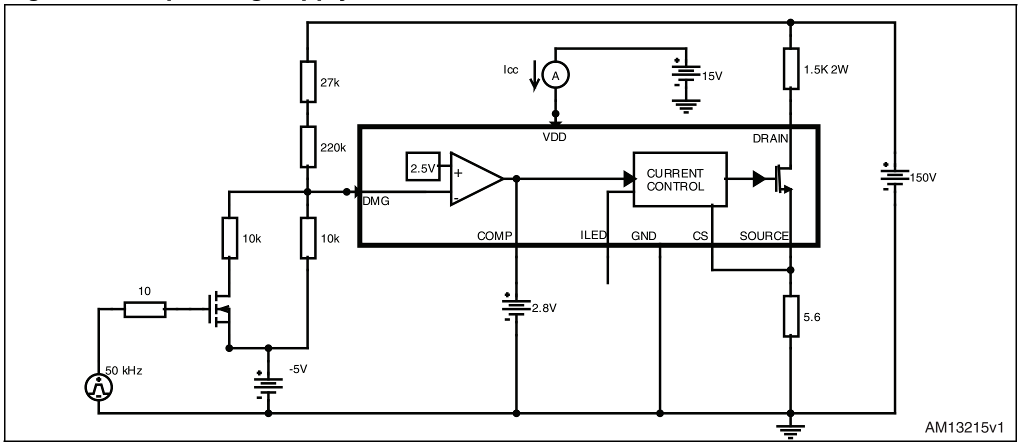


Figure 8. Quiescent current test circuit



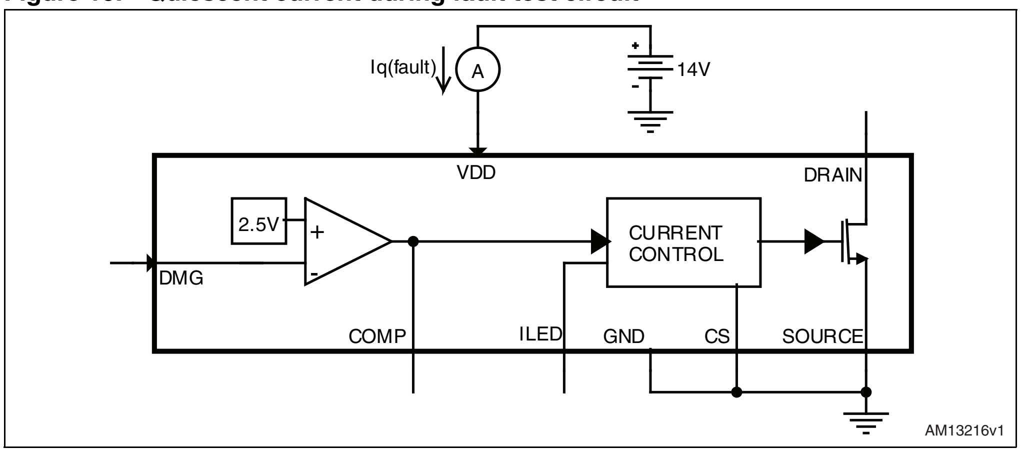
$$Iq = Iq_{meas} - \frac{0.11 * 3V}{3.3k\Omega} - 100\mu A$$

Figure 9. Operating supply current test circuit



Note: The circuit across the DMG pin is used for switch-on synchronization.

Figure 10. Quiescent current during fault test circuit



4 Device description

The HVLED815PF is a high-voltage primary switcher intended for operating directly from the rectified mains with minimum external parts to provide high power factor (> 0.90) and an efficient, compact and cost effective solution for LED driving. It combines a high-performance low-voltage PWM controller chip and an 800 V, avalanche-rugged Power MOSFET, in the same package.

The PWM is a current-mode controller IC specifically designed for ZVS (zero voltage switching) flyback LED drivers, with constant output current (CC) regulation using primary sensing feedback (PSR). This eliminates the need for the optocoupler, the secondary voltage reference, as well as the current sense on the secondary side, while still maintaining a good LED current accuracy. Moreover, it guarantees a safe operation when short-circuit of one or more LEDs occurs.

The device can also provide a constant output voltage regulation (CV): it allows the application to be able to work safely when the LED string opens due to a failure.

In addition, the device offers the shorted secondary rectifier (i.e. LED string shorted due to a failure) or transformer saturation detection.

Quasi-resonant operation is achieved by means of a transformer demagnetization sensing input that triggers MOSFET turn-on. This input serves also as both output voltage monitor, to perform CV regulation, and input voltage monitor, to achieve mains-independent CC regulation (line voltage feedforward).

The maximum switching frequency is top-limited below 166 kHz, so that at medium-light load a special function automatically lowers the operating frequency while still maintaining the operation as close to ZVS as possible. At very light load, the device enters a controlled burst-mode operation that, along with the built-in high-voltage startup circuit and the low operating current of the device, helps minimize the residual input consumption.

Although an auxiliary winding is required in the transformer to correctly perform CV/CC regulation, the chip is able to power itself directly from the rectified mains. This is useful especially during CC regulation, where the flyback voltage generated by the winding drops.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Figure 11. SO16N mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
c	0.17		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
k	0		8°
ccc			0.10

Figure 12. SO16N drawing

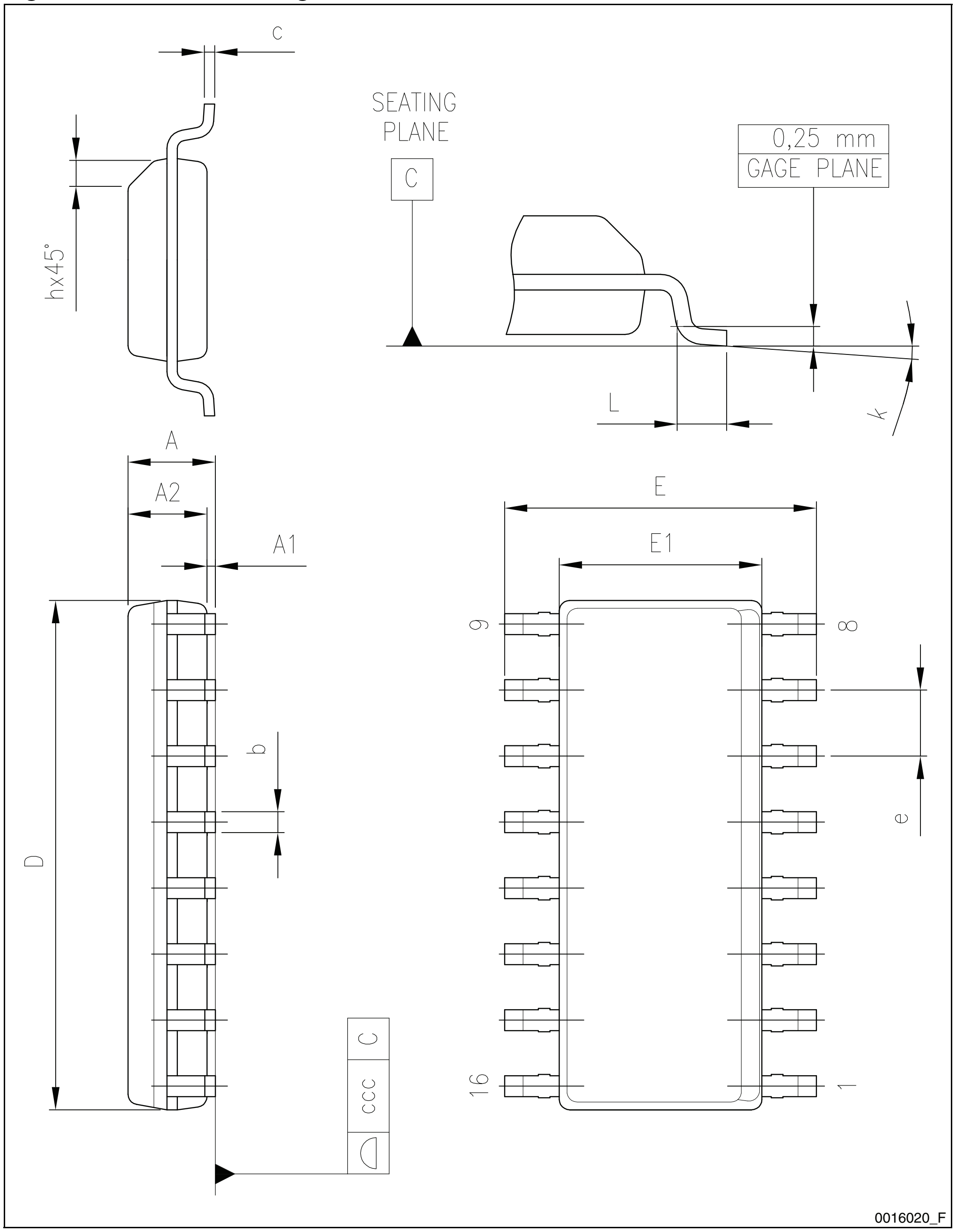
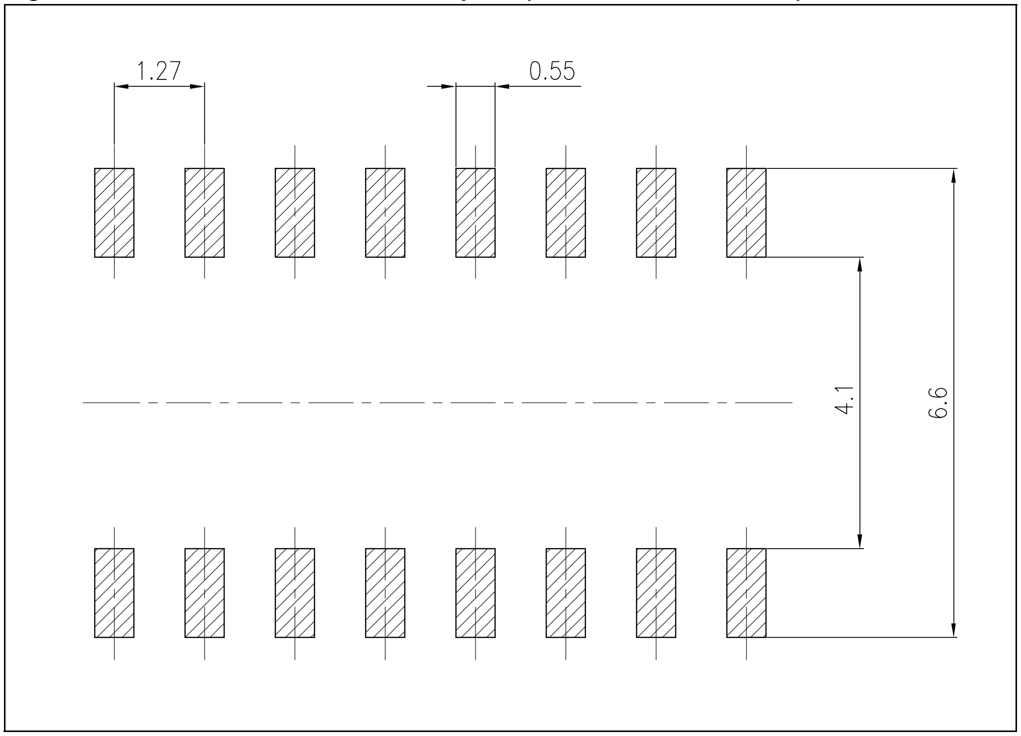


Figure 13. SO16N recommended footprint (dimensions are in mm)



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
26-Jul-2012	1	Initial release.
29-Aug-2012	2	Added *Table 2: Pin description on page 6*.
23-Oct-2012	3	Modified T_J value on *Table 3: Thermal data*. Updated T_J value in note 2 (below *Table 5: Electrical characteristics*). Minor text changes.

Please Read Carefully:

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com