19-6160; Rev 0; 12/11

EVALUATION KIT AVAILABLE

MAX17512

High-Speed, Constant On-Time, Valley Current Regulator for Tracking Applications

General Description

The MAX17512 IC is a fully integrated valley current regulator with a modified constant on-time control scheme that emulates hysteretic-mode behavior for transients. It integrates both the high-side and low-side switches that are designed to deliver load currents up to 6A. The device supports a 6.5V to 18V wide input voltage range. The device accepts an external current-reference signal (ICMD) and regulates the inductor current valley such that it closely follows the reference signal. This allows dynamic voltage scheduling and advanced power management, reducing system power consumption. Example applications include envelope tracking in base stations, dynamic voltage scheduling in industrial control, and lighting.

The device uses a modified constant on-time valley current-mode control scheme to control the inductor current and incorporates a high-performance PWM comparator with very low hysteresis and propagation delay. The constant on-time is programmable using an external resistor, allowing the user to set the desired ripple current in the inductor. This architecture results in a very accurate valley controlled current source whose ripple is tightly controlled, thus making it suitable for high-speed voltage/current-tracking systems.

The architecture of the device allows for simple implementation of multiple parallel modules by driving the respective ICMD pin with the same external reference current signal. An EN/UVLO input functions both as an on/off pin as well as a UVLO monitor. The input supply start voltage is externally programmable with a voltage-divider.

The device incorporates a linear regulator (V_{CC}) for powering the control (AVCC) and driver (PVCC) circuitry. The device incorporates an active-high, open-drain $\overline{FLT}$ pin that goes low when an overcurrent, UVLO, or overtemperature fault occurs.

The device is available in a compact, space-saving, 20-pin (5mm x 5mm) TQFN package with an exposed pad.

Applications

Base-Station Envelope-Tracking Power Supplies

Precision Lighting

Industrial Control

Features

- **6.5V to 18V Wide Input Voltage Range**
- **Delivers Currents Up to 6A**
- **Programmable Constant-On Control**
- **Current-Sense Accuracy > 95% at 5A**
- **High-Speed PWM Comparator**
- **Current-Loop Propagation Delay < 30ns**
- **Peak Efficiency > 88%**
- **$\overline{FLT}$ Power-OK (POK) Signal**
- **Undervoltage Lockout**
- **Overcurrent, Short-Circuit Protection**
- **Overtemperature Protection**
- **Space-Saving, 20-Pin (5mm x 5mm) TQFN Package**

***Ordering Information** appears at end of data sheet.*

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX17512.related**.*

ABSOLUTE MAXIMUM RATINGS

PVIN_ to PGND_ ..... -0.3V to +22V
AVIN to SGND ..... -0.3V to +22V
EN/UVLO to SGND ..... -0.3V to (V_{AVIN} + 0.3V)
V_{CC} to SGND ..... -0.3V to (V_{AVIN} + 0.3V)
AVCC to SGND ..... -0.3V to +6.5V
$\overline{FLT}$ to SGND ..... -0.3V to +6.5V
RTON, ICMD to SGND ..... -0.3V to (V_{AVCC} + 0.3V)
PVCC to PGND_ ..... -0.3V to +6.5V
PGND_ to SGND ..... -0.3V to +0.3V
LX_ to PGND_ ..... -0.3V to ($V_{PVIN\_}$ + 0.3V)
BST to LX_ ..... -0.3V to +6.5V
BST to PGND_ ..... -0.3V to ($V_{PVIN\_}$ + 6.5V)
Continuous Power Dissipation (single-layer board)
TQFN (derate 33mW/°C above +70°C) 2700mW
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Junction Temperature (continuous) ..... +150°C
Soldering Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{PVIN\_}$ = V_{AVIN} = V_{IN} = 12V, $V_{EN/UVLO}$ = 12V, V_{PVCC} = V_{AVCC} = 5V, $V_{PGND\_}$ = V_{SGND} = 0V, V_{BST} = $V_{LX\_}$ + 5V, R_{RTON} = 30.1kΩ, V_{ICMD} = 0V, T_A = T_J = -40°C to +125°C, unless otherwised noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT VOLTAGE (PVIN_ and AVIN)							
Input Voltage Range	V_{IN}			6.5		18	V
Input UVLO	V_{INR}	Rising		5.7	6	6.3	V
	V_{INF}	Falling		5.4	5.7	6	
Input Supply Current	I_{VINQ}	Quiescent current	V_{ICMD} = 0V		0.4	0.85	mA
			V_{ICMD} = 1.4V		0.88	1.25	
	I_{VINSH}	$V_{EN/UVLO}$ = 0V			8	15	µA
PVCC Supply Current	I_{PVCCQ}	Quiescent current			300	600	µA
	I_{PVCCSW}	LX_ frequency = 2MHz			16.7		mA
	I_{PVCCSH}	$V_{EN/UVLO}$ = 0V			54	100	µA
AVCC Supply Current	I_{AVCCQ}	Quiescent current	V_{ICMD} = 0V		0.8	1.5	mA
			V_{ICMD} = 1.4V		1.6	2.5	
	I_{AVCCSH}	$V_{EN/UVLO}$ = 0V			20	35	µA
EN/UVLO							
Rising Threshold	$V_{EN/UVLOR}$			1.186	1.223	1.26	V
Falling Threshold	$V_{EN/UVLOF}$				1.223		V
Input Leakage Current	$I_{EN/UVLO}$	1.1V < $V_{EN/UVLO}$ < 1.3V, T_A = T_J = +25°C		-100		+100	nA

ELECTRICAL CHARACTERISTICS (continued)

($V_{PVIN\_}$ = V_{AVIN} = V_{IN} = 12V, $V_{EN/UVLO}$ = 12V, V_{PVCC} = V_{AVCC} = 5V, $V_{PGND\_}$ = V_{SGND} = 0V, V_{BST} = $V_{LX\_}$ + 5V, R_{RTON} = 30.1kΩ, V_{ICMD} = 0V, T_A = T_J = -40°C to +125°C, unless otherwised noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATOR (V_{CC})							
V_{CC} Output Voltage Range	V_{CC}	1mA < I_{VCC} < 30mA, 6.5V < V_{IN} < 16V		4.75	5.05	5.25	V
V_{CC} Output Voltage In Dropout		V_{IN} = 4.5V, I_{VCC} = 10mA		4.3	4.44		V
V_{CC} Current Limit	I_{VCCLIM}	V_{IN} = 6.5, V_{VCC} = 3V		50	105	160	mA
AVCC UVLO	V_{AVCCR}	Rising		3.9	4.1	4.25	V
	V_{AVCCF}	Falling		3.7	3.9	4.05	
POWER MOSFET							
High Side	R_{DSON-H}	$I_{LX\_}$ = 1A			40	80	mΩ
Low Side	R_{DSON-L}	$I_{LX\_}$ = 1A			40	80	mΩ
BST DRIVER							
BST Capacitor Charging Current (Note 2)		PVIN_ to BST		2.9	5	8.2	mA
		LX_ to PGND_		5.5	10	15.5	
BST to LX_ POK	BSTPOK			1.9	3.1	4	V
LOW-SIDE CURRENT COMPARATOR							
Low-Side Current-Sense Comparator Delay	t_{DELAY}				12		ns
Low-Side Current-Sense Comparator Output to LX_ Rise					8.5		ns
Low-Side Current-Sense Blanking Time	t_{BLANK}			50	95	150	ns
VALLEY CURRENT SETTINGS (ICMD)							
V_{ICMD} to $I_{LX\_}$ Transresistance	R_{TRANS}	0.8A < $I_{LX\_}$ < 1A	T_A = +25°C	0.27	0.28	0.29	V/A
			-40°C ≤ T_A ≤ +125°C	0.258		0.306	
Command Voltage for 1.8A Inductor Valley Current	V_{ICMD}	$I_{LX\_}$ = 1.8A		802	900	988	V
Driver Disable Threshold on Command Voltage (Note 3)	$V_{ICMD-DD}$				0.465		V
ICMD Input Bias Current	I_{ICMD}	V_{ICMD} ≤ 2.2V		-2.5	-0.36		µA
TON CONTROL (RTON)							
RTON Resistance Range	R_{RTON}			10		36	kΩ
High-Side Switch On-Time	t_{ON}	V_{RTON} = 1.5V		114	120	126	ns
RTON Pullup Current	I_{RTON}	V_{RTON} = 1.5V		47.5	50	52.5	µA
Minimum High-Side Switch On-Time	t_{ONMIN}	V_{RTON} = unconnected			95		ns
Maximum High-Side Switch On-Time	t_{ONMAX}	V_{RTON} = 0V			550		ns

ELECTRICAL CHARACTERISTICS (continued)

($V_{PVIN\_}$ = V_{AVIN} = V_{IN} = 12V, $V_{EN/UVLO}$ = 12V, V_{PVCC} = V_{AVCC} = 5V, $V_{PGND\_}$ = V_{SGND} = 0V, V_{BST} = $V_{LX\_}$ + 5V, R_{RTON} = 30.1kΩ, V_{ICMD} = 0V, T_A = T_J = -40°C to +125°C, unless otherwised noted.) (Note 1)

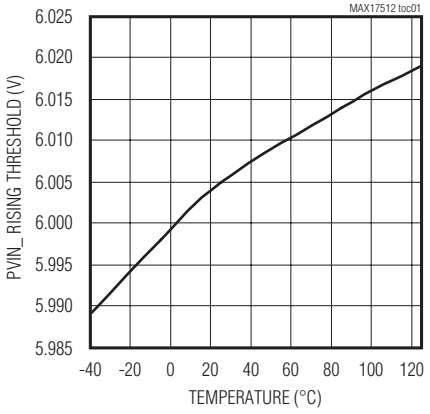
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FLT}$						
Output Leakage Current (Off State)		$V_{\overline{FLT}}$ = 5V, T_A = T_J = +25°C			0.1	µA
$\overline{FLT}$ Output Voltage (On State)		$I_{\overline{FLT}}$ = 10mA	0		0.4	V
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	$t_{SHUTDOWN}$	Temperature rising		165		°C
Thermal-Shutdown Hysteresis				20		°C

Note 1: All devices 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.
Note 2: Currents to charge BST to LX_ capacitor when the voltage across it is < BST POK.
Note 3: This is the minimum input voltage required at ICMD to produce inductor current.

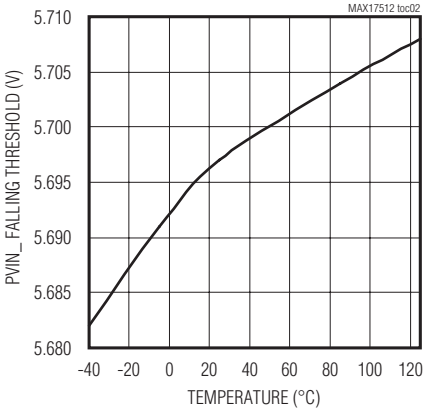
Typical Operating Characteristics

($V_{PVIN\_}$ = V_{AVIN} = V_{IN} = 12V, $V_{EN/UVLO}$ = 12V, V_{PVCC} = V_{AVCC} = 5V, V_{BST} = $V_{LX\_}$ + 5V, R_{RTON} = 30.1kΩ, T_A = T_J = -40°C to +125°C, unless otherwised noted.)

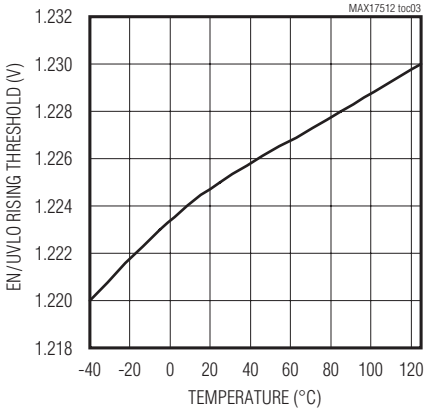
PVIN_ RISING THRESHOLD vs. TEMPERATURE



PVIN_ FALLING THRESHOLD vs. TEMPERATURE



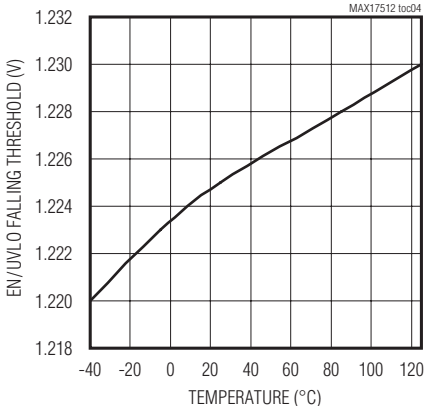
EN/UVLO RISING THRESHOLD vs. TEMPERATURE



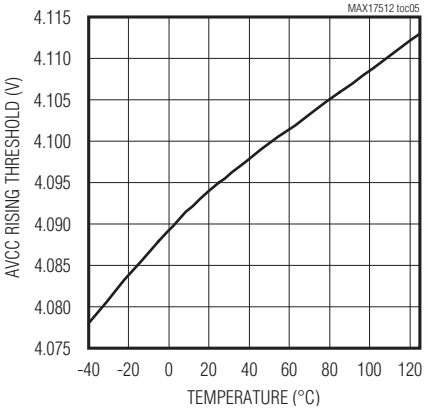
Typical Operating Characteristics (continued)

($V_{PVIN\_}$ = V_{AVIN} = V_{IN} = 12V, $V_{EN/UVLO}$ = 12V, V_{PVCC} = V_{AVCC} = 5V, V_{BST} = $V_{LX\_}$ + 5V, R_{RTON} = 30.1kΩ, T_A = T_J = -40°C to +125°C, unless otherwised noted.)

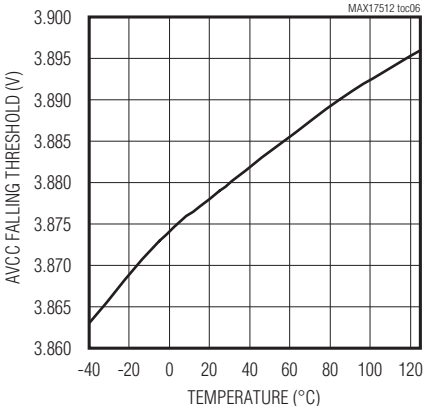
EN/UVLO FALLING THRESHOLD vs. TEMPERATURE



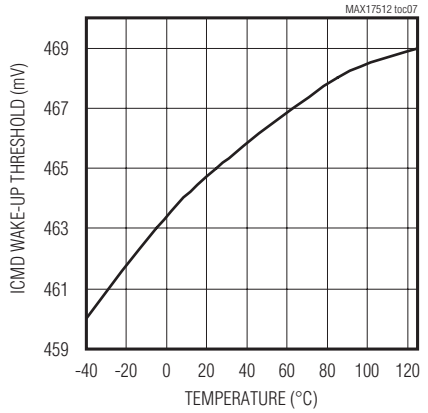
AVCC RISING THRESHOLD vs. TEMPERATURE



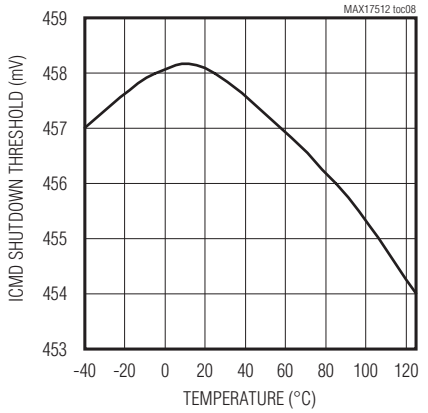
AVCC FALLING THRESHOLD vs. TEMPERATURE



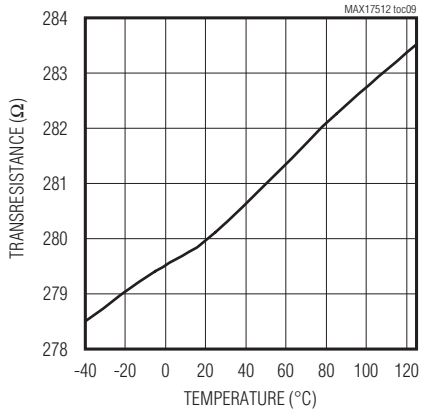
ICMD WAKE-UP THRESHOLD vs. TEMPERATURE



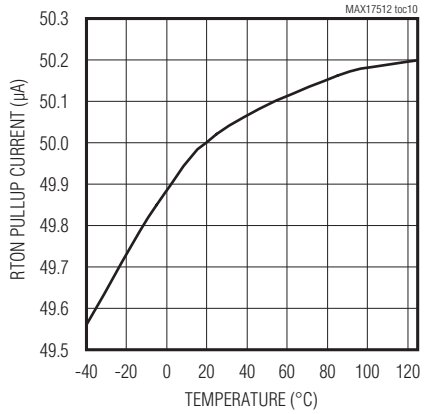
ICMD SHUTDOWN THRESHOLD vs. TEMPERATURE



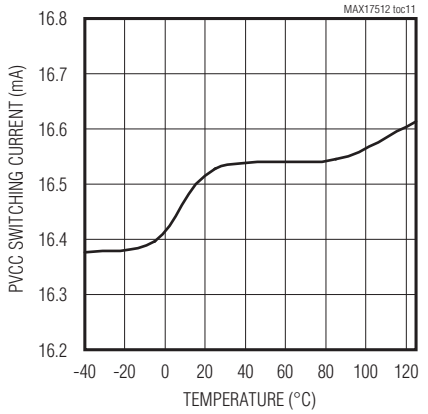
TRANSRESISTANCE vs. TEMPERATURE



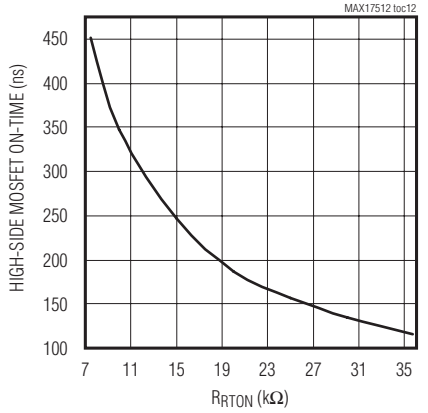
RTON PULLUP CURRENT vs. TEMPERATURE



PVCC SWITCHING CURRENT vs. TEMPERATURE



HIGH-SIDE MOSFET ON-TIME vs. R_{RTON}

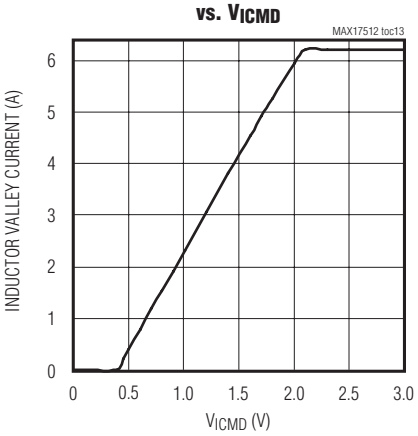


High-Speed, Constant On-Time, Valley Current Regulator for Tracking Applications

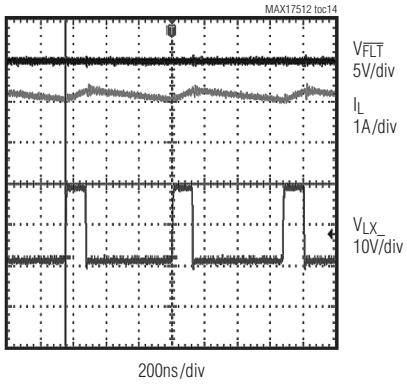
Typical Operating Characteristics (continued)

($V_{PVIN\_}$ = V_{AVIN} = V_{IN} = 12V, $V_{EN/UVLO}$ = 12V, V_{PVCC} = V_{AVCC} = 5V, V_{BST} = $V_{LX\_}$ + 5V, R_{RTON} = 30.1kΩ, T_A = T_J = -40°C to +125°C, unless otherwised noted.)

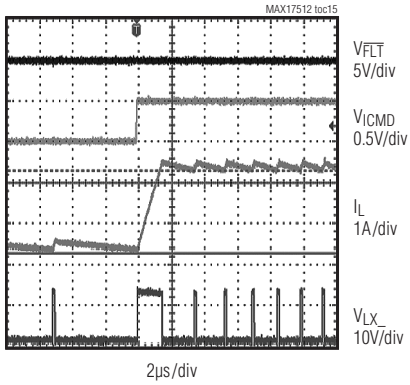
INDUCTOR VALLEY CURRENT vs. V_{ICMD}



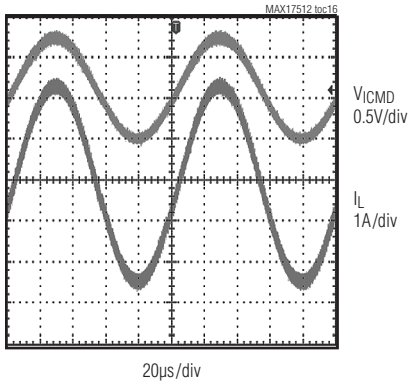
SWITCHING WAVEFORM



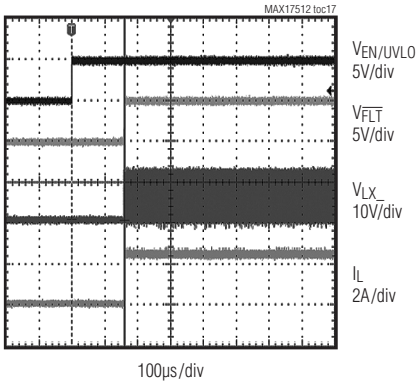
MAX17512 PERFORMANCE FOR STEP COMMAND



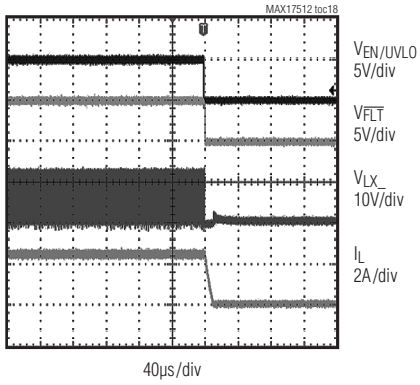
ENVELOPE-TRACKING WAVEFORM



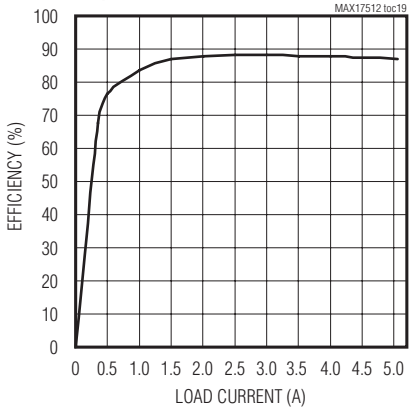
ENABLE STARTUP RESPONSE



ENABLE SHUTDOWN RESPONSE

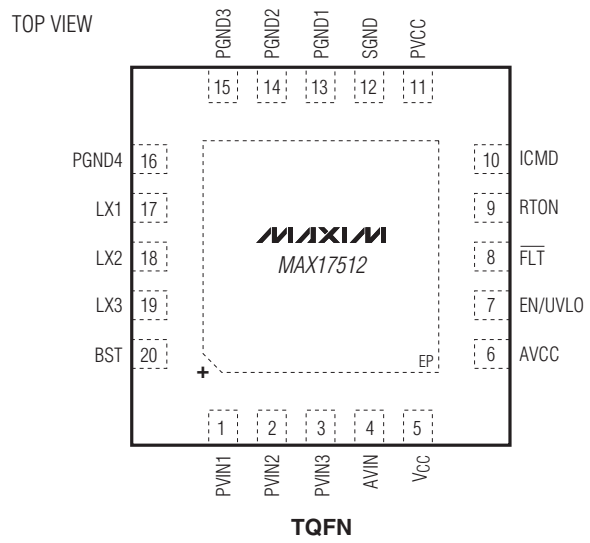


EFFICIENCY GRAPH AT 12V INPUT (TYPICAL APPLICATION CIRCUIT)



High-Speed, Constant On-Time, Valley Current Regulator for Tracking Applications

Pin Configuration



TQFN

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	PVIN1, PVIN2, PVIN3	Buck Regulator Input. Connect PVIN_ to the input-voltage source. Bypass PVIN_ to PGND with a 2x 10µF (min) ceramic capacitor.
4	AVIN	Input to Internal LDO. Externally short AVIN to PVIN_.
5	V_{CC}	Linear Regulator Output. Connect a 2.2µF input bypass capacitor from V_{CC} to SGND as close as possible to the IC. If not used, connect to AVIN.
6	AVCC	Filtered V_{CC} Input. Connect to V_{CC} with a 10Ω resistor. Bypass to SGND with a 0.22µF or larger ceramic capacitor, as close as possible to the IC. Internally connected to PVCC with 1kΩ resistance.
7	EN/UVLO	Enable/Undervoltage Lockout Pin. To externally program the UVLO threshold of the input supply, connect EN/UVLO to the midpoint of a resistive divider between the input supply and SGND.
8	$\overline{FLT}$	Active-Low, Open-Drain Fault Output. $\overline{FLT}$ goes low if overtemperature, AVCC < V_{UVLO}, or V_{EN} < 1.225V conditions occur.
9	RTON	TON-Setting Pin. Connect a resistor to GND for TON setting. Optionally add a resistor from AVIN to the RTON pin current-ripple partial feed-forward compensation to set the LX_ on-time.
10	ICMD	Reference Inductor Valley Current Input. Drive this pin from 0.4V to 1.94V to program the inductor valley current from 0A to 5.5A.
11	PVCC	Internal MOSFET Gate-Driver Power-Supply Input. Connect a 2.2µF input bypass capacitor from PVCC to PGND as close as possible to the IC. Directly connect PVCC to the external power supply when not using the internal linear regulator.

Pin Description (continued)

PIN	NAME	FUNCTION
12	SGND	Signal Ground. Connect SGND to the SGND plane. Connect SGND and PGND at a single point.
13–16	PGND1–PGND4	Power Ground. Connect with a short wide trace to the input decoupling-capacitor ground terminal.
17, 18, 19	LX1, LX2, LX3	External Inductor Connection. Connect LX_ to the switched side of the inductor.
20	BST	Boost Flying Capacitor. Connect a ceramic capacitor with a minimum value of 47nF between BST and LX_.
—	EP	Exposed Pad for Thermal Dissipation. Ensure that the exposed pad connects to a large copper plane that is electrically connected to the SGND pin of the IC.

Detailed Description

The MAX17512 IC is optimized for implementing high efficiency, 6.5V to 18V wide input voltage range, and synchronous, step-down valley current regulators. The device employs a valley constant on-time, current-mode-control architecture with integrated power MOSFETs to deliver load currents up to 6A. The device incorporates a very high-performance PWM comparator that has very low hysteresis and propagation delay. It regulates the inductor current to the valley current-command voltage applied at the ICMD pin. The device also offers selectable on-time that decides the amount of ripple in the inductor current. The architecture of the device allows for simple implementation of multiple parallel modules by driving the respective ICMD pin with the same current-command voltage.

Internal low R_{DSON} integrated switches ensure high efficiency at heavy loads, while minimizing critical inductance, making the layout design a much simpler task than that of discrete solutions. The device improves efficiency by means of an innovative break-before-make scheme that minimizes body diode conduction time, while ensuring that there is no shoot through in the MOSFETs. The device's simple layout and footprint assure first-pass success in new designs.

The device includes an open-drain $\overline{FLT}$ output that goes high when the device is ready to commence operation. See the *Block Diagram* for more information.

Input Voltage Range

The device is designed to operate over a 6.5V to 18V input supply range. The PVIN_ pins are connected to the drain of the internal high-side MOSFET. The AVIN pin connects to the input of an internal linear regulator. The output of the linear regulator is available at the V_{CC} pin.

Linear Regulator (V_{CC})

An internal linear regulator (V_{CC}) provides a 5V nominal supply to power the internal control functions and driver circuitry. The internal linear regulator is powered from the AVIN pin. When using the internal V_{CC} linear regulator, the AVCC and PVCC pins are connected together. To minimize IC power dissipation, the AVCC and PVCC pins can be connected to the external 5V power supply.

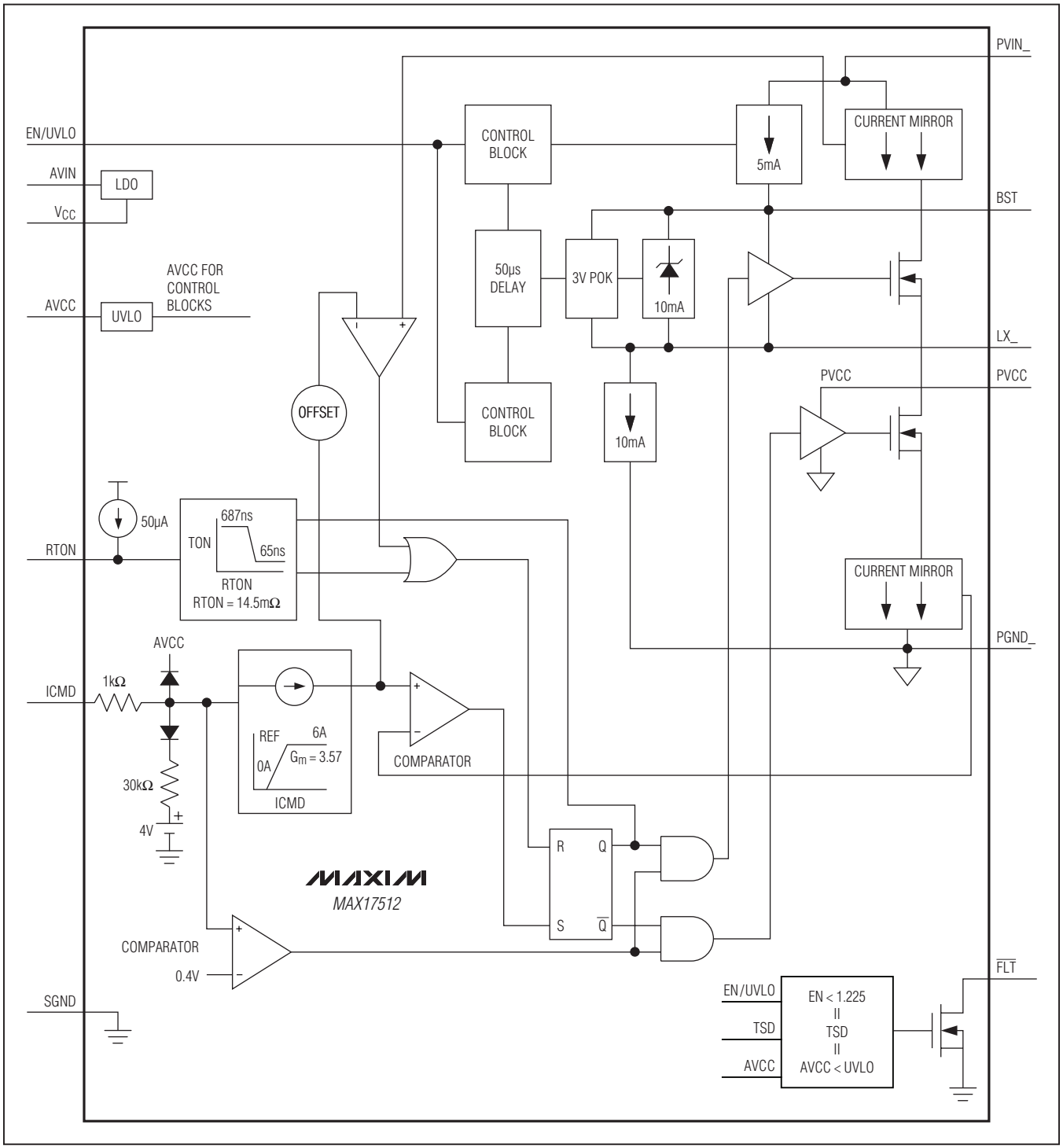
The maximum regulator input voltage (AVIN) is 18V (min). Bypass V_{IN} to PGND with a 10µF ceramic capacitor. Bypass the output of the linear regulator (V_{CC}) with a 2.2µF ceramic capacitor to SGND. When V_{IN} is higher than 6.5V, V_{CC} is typically 5V. The V_{CC} linear regulator can source up to 50mA to supply the device, power the low-side gate driver, and recharge the external boost capacitor when V_{CC} is connected to AVCC and PVCC.

High-Side Gate-Driver Supply (BST)

A flying bootstrap capacitor is connected between LX_ and BST to provide the gate-driver voltage to the internal high-side n-channel MOSFET. Upon startup, an internal low-side switch connects LX_ to ground and charges the BST capacitor to PVCC. Once the BST capacitor is charged, the internal low-side switch is turned off and the BST capacitor voltage provides the necessary enhancement voltage to turn on the high-side switch. A 47nF, 16V ceramic capacitor located as close as possible to the device is used.

High-Speed, Constant On-Time, Valley Current Regulator for Tracking Applications

Block Diagram



High-Speed, Constant On-Time, Valley Current Regulator for Tracking Applications

Control Scheme

The device employs a modified constant on-time valley current-control scheme to generate the programmed inductor current and inductor ripple current. The heart of this control scheme is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to the resistance value connected at the RTON pin. In this time period, the inductor current rises with a slope equal to the ratio of input voltage to the inductance. The control scheme turns off the high-side MOSFET and turns on the low-side MOSFET after the programmed on-time. The low-side MOSFET turns on until the inductor valley current falls below the programmed threshold at the ICMD pin, as determined by the low-side current-sense comparator. A time period that comprises the high-side MOSFET on-time and low-side MOSFET on-time is called a switching time period. The low-side current-sense comparator has very low hysteresis and low propagation delay. The overall current-sense comparator delay is 20ns (typ). This feature is useful in high-performance applications such as envelope tracking in base stations.

The device incorporates a comparator that monitors the change in current-command voltage from the previously programmed command value. If the change in current-command voltage is greater than 70mV (typ), then the comparator ensures that the high-side MOSFET is on until the inductor current is close to the latest current command. This innovative scheme ensures a hysteretic type of behaviour for step changes in the current command, as shown in Figure 1.

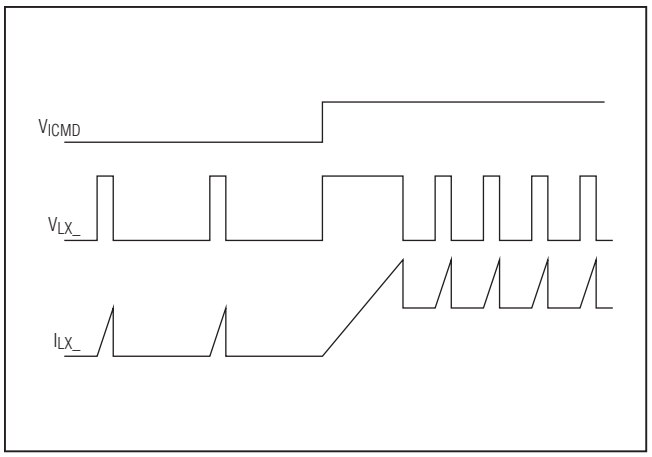


Figure 1. Modified Constant On-Time Valley Current-Control Scheme

$\overline{FLT}$ Power-OK Signal

The device provides a $\overline{FLT}$ signal that serves as a power-OK signal to the system. $\overline{FLT}$ is an open-drain signal and requires a pullup resistor to the preferred supply voltage. The $\overline{FLT}$ signal monitors the input voltage (PVIN), AVCC and die temperature, and pulls high when all these inputs are within their respective operating regions. The $\overline{FLT}$ signal pulls low when either of the inputs fall below its falling threshold.

Thermal Shutdown

The device contains an internal thermal sensor that limits the total power dissipation to protect it in the event of an extended thermal-fault condition. When the die temperature exceeds +160°C, the thermal sensor shuts down the device, turning it off to allow the die to cool. After the die temperature falls by 20°C (typ), the device restarts.

Applications Information

Configuring AVCC and PVCC

AVCC supplies all the control circuitry in the device, and similarly, PVCC supplies the internal MOSFET gate-driver circuitry. Both AVCC and PVCC require a 5V power supply for the internal blocks to operate. For this purpose, the device integrates a linear regulator that generates a 5V supply (V_{CC}). The internal linear regulator can be connected to AVCC through a lowpass filter, as shown in Figure 2. PVCC can be connected directly to V_{CC}.

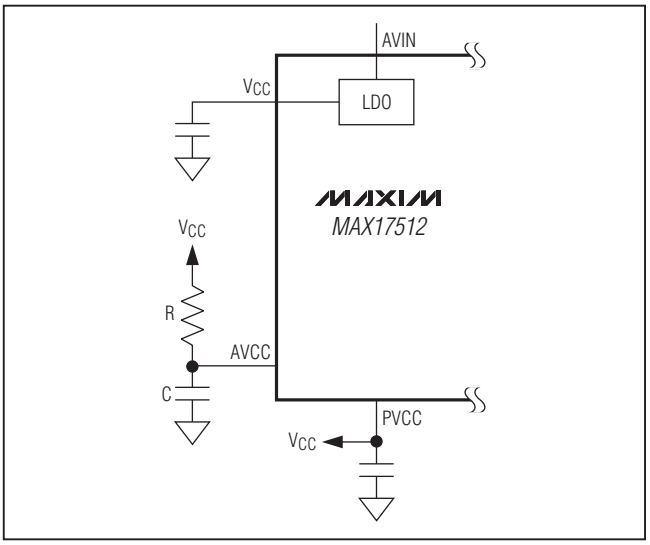


Figure 2. Configuring V_{CC} to Power Control and Drive Circuitry

In applications where it is desired to reduce the internal linear regulator power dissipation to maximize the output current capability of the device, an external 5V rail (V_{REG}) can be used to power AVCC and PVCC, as shown in the Figure 3.

Startup Voltage Setting (EN/UVLO)

The device's EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable undervoltage lockout (UVLO) pin. The device does not commence switching operations unless the EN/UVLO pin voltage exceeds 1.225V (typ). The device turns off if the EN/UVLO pin voltage falls below 1.225V (typ).

A resistor-divider from the input bus to ground can be used to divide-down and apply a fraction of the input voltage to the EN/UVLO pin. The values of the resistor-divider can be selected such that the EN/UVLO pin voltage exceeds the 1.225V (typ) turn-on threshold at the desired input DC bus voltage, as shown in Figure 4. For given values of startup input voltage (V_{START}), the resistor value (R_{TOP}) for the divider can be calculated as follows, assuming a 49.9kΩ resistor for R_{BOTTOM}.

$$R_{TOP} = R_{BOTTOM} \times \left[\frac{V_{START}}{1.225} - 1\right] \text{ in k}\Omega$$

where R_{TOP} and R_{BOTTOM} are in kΩ and V_{START} is in volts.

Programming the Valley Current (ICMD)

The device regulates the valley point of the inductor current depending on the current-command voltage applied at the ICMD pin. For example, the device regulates the valley current to 5A with ±250mA for a 1.842V current-command voltage. The current-command voltage (V_{ICMD}) to be applied at the ICMD pin for a given inductor valley current (I_{VALLEY}) can be calculated as follows:

$$V_{ICMD} = \left[(I_{VALLEY} \times 0.28) + 0.442\right] \text{ in volts}$$

where I_{VALLEY} is in amps.

The device can deliver a maximum current of 6A and hence a clamp on the voltage on the current-command voltage is incorporated. Therefore, the appropriate current-command voltage range is 0.442V to 2.15V, which corresponds to a valley current range of 220mA to 6A.

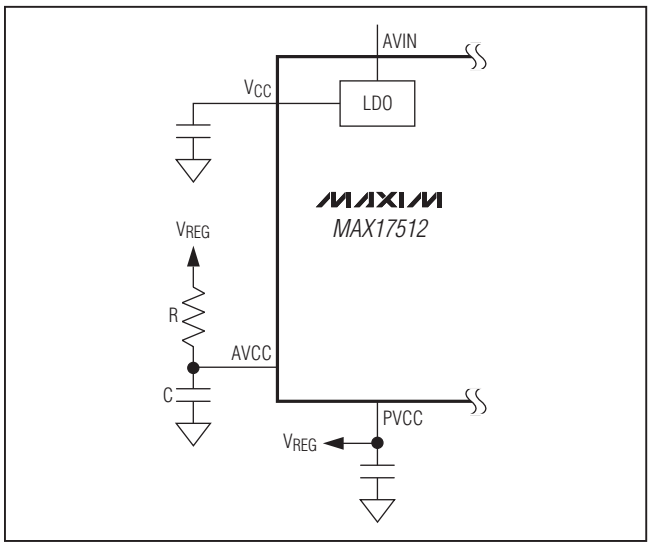


Figure 3. Configuring the MAX17512 to Use an External 5V Regulator (V_{REG})

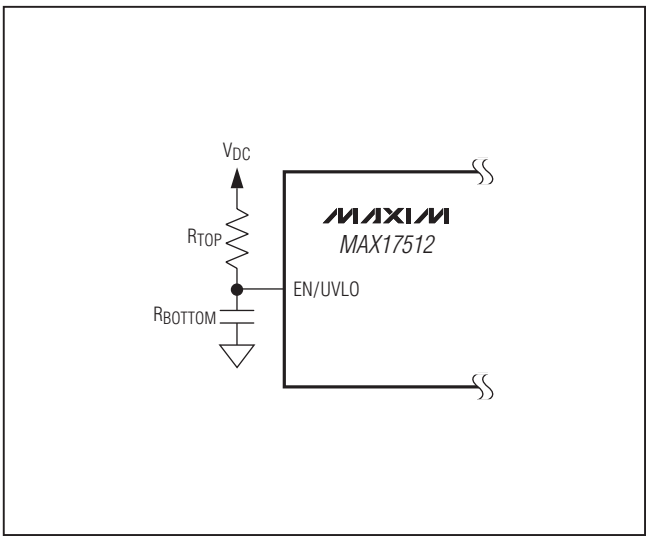


Figure 4. Programming EN/UVLO

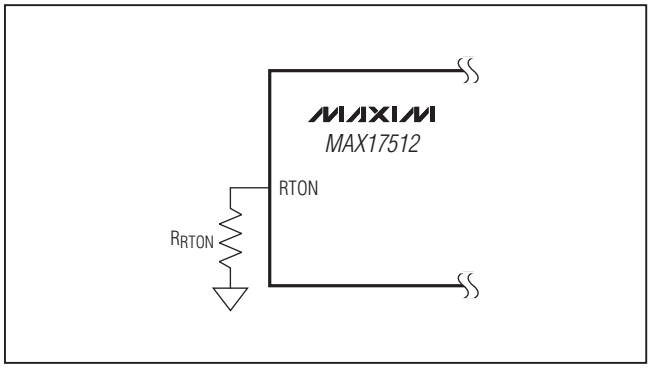


Figure 5. Programming the High-Side Switch On-Time

Programming the Constant On-Time (RTON)

The device employs a modified constant on-time valley current-control scheme (see the *Control Scheme* section) to generate the programmed inductor current and inductor ripple current. The heart of this control scheme is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to the resistance value connected between the RTON pin and SGND terminals. The resistor (R_{RTON}) can be calculated for a given on-time as follows:

$$R_{RTON} = \frac{2520}{t_{ON} - 30} \text{ in k}\Omega$$

where t_{ON} is in ns.

For example, a 36kΩ resistor should be connected between the RTON pin and SGND to program 100ns high-side MOSFET on-time (see Figure 5).

Thermal Considerations

Ensure that the junction temperature of the device does not exceed +125°C under the operating conditions specified for the design. The internal linear regulator power dissipation, which occurs when the device uses its internal linear regulator to power the control and driver circuitry, can be calculated using the following equation:

$$P_{IN} = V_{AVIN} \times I_{AVIN}$$

where V_{AVIN} is the voltage applied at the AVIN pin and I_{AVIN} is the operating supply current. The I_{AVIN} operating supply current can be calculated as follows:

$$I_{AVIN} = I_{VINQ} + I_{PVCCSW} + I_{AVCCQ}$$

where I_{VINQ} is the input supply current, I_{PVCCSW} is the switching current drawn from PVCC for a given frequency of operation, and I_{AVCCQ} is the current drawn from AVCC.

The power required for the device to operate for the design, in which the external V_{REG} regulator is used to power the control and driver circuitry, can be calculated using the following equation:

$$P_{IN} = (V_{IN} \times I_{VINQ}) + [V_{REG} \times (I_{PVCCSW} + I_{AVCCQ})]$$

where V_{IN} is the voltage applied at the PVIN and AVIN pins, V_{REG} is the external regulator voltage, I_{VINQ} is the input supply current, I_{PVCCSW} is the switching current drawn from PVCC for a given frequency of operation, and I_{AVCCQ} is the current drawn from AVCC.

The internal high-side and low-side nMOSFETs experience conduction loss and transition loss when switching between on and off states. The conduction and switching transition losses for a MOSFET can be calculated as follows:

$$P_{CONDUCTION} = I_{RMS}^2 \times R_{DSON}$$

$$P_{TRANSITION} = 0.5 \times V_{INMAX} \times I_{PK} \times (t_R + t_F) \times f_{SW}$$

where I_{RMS} is the RMS current, R_{DSON} is the on-resistance, and t_R and t_F are the rise and fall times of the internal MOSFET.

Additional loss occurs in the system in every switching cycle due to energy stored in the drain-source capacitance of the internal MOSFET being lost when the MOSFET turns on, and discharges the drain-source capacitance voltage to zero. This loss is estimated as follows:

$$P_{CAP} = 0.5 \times C_{DS} \times V_{DSMAX}^2 \times f_{SW}$$

where C_{DS} is the drain-source capacitance of the MOSFET, V_{DSMAX} is the maximum drain-source voltage, and f_{SW} is the frequency of operation.

The total power loss in the device can be calculated from the following equation:

$$P_{LOSS} = P_{IN} + P_{TCONDUCTION} + P_{TTRANSITION} + P_{TCAP}$$

where $P_{TCONDUCTION}$ is the conduction loss in the high-side and low-side MOSFETs, $P_{TTRANSITION}$ is the total transition loss in both the high-side and low-side switches, and P_{TCAP} is the total drain-source capacitance loss.

The maximum power that can be dissipated in the device is 2666mW at +70°C temperature. The power-dissipation capability should be derated, as the temperature goes above +70°C at 33mW/°C. For a multilayer board, the thermal-performance metrics for the package are as follows:

$$\theta_{JA} = 30°C/W$$

$$\theta_{JC} = 2°C/W$$

The junction temperature rise of the device can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the following equation:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature (T_{EP_MAX}), by using proper heatsinks, then the junction temperature rise of the device can be estimated at any given maximum ambient temperature from the following equation:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

Layout, Grounding, and Bypassing

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency switching power converters. This implies that the loop areas for forward and return pulsed currents in various parts of the circuit should be minimized. Additionally, small-current loop areas reduce radiated EMI. Similarly, the heatsink of the main MOSFET presents a dV/dt source; therefore, the surface area of the MOSFET heatsink should be minimized as much as possible.

Ground planes must be kept as intact as possible. The ground plane for the power section of the converter should be kept separate from the analog ground plane, except for a connection at the least noisy section of the power ground plane, typically the return of the PVCC filter capacitor. PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the device for efficient heat dissipation. For a sample layout that ensures first-pass success, refer to the MAX17512 evaluation kit layout available at **www.maxim-ic.com**.

Typical Operating Circuit

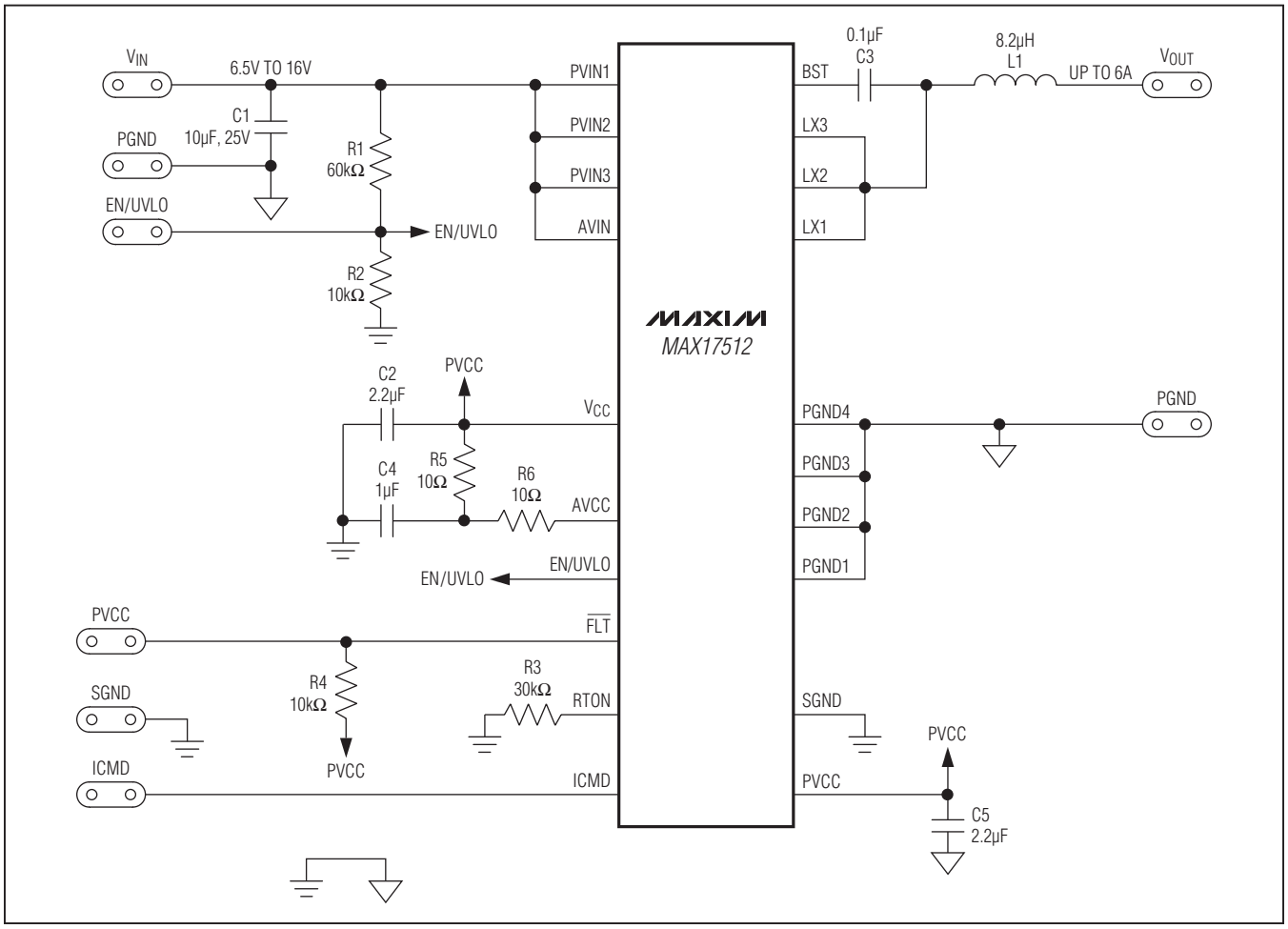


Figure 6. MAX17512 Typical Application Circuit (Envelope Tracking)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17512ATP+	-40°C to +125°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN	T2055+4	21-0140	90-0009

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—