XRT5894

Four-Channel E1
Line Interface (3.3V or 5.0V)

March 2000-3

FEATURES

- Compliant with ITU G.703 Pulse Mask Template for 2.048Mbps (E1) Rates
- Four Independent CEPT Transceivers
- Supports Differential Transformer Coupled Receivers and Transmitters
- On Chip Pulse Shaping for Both 75Ω and 120Ω Line Drivers
- Compliant with ITU G.775 LOS Declaration/Clearing Recommendation
- Optional User Selectable LOS Declaration/Clearing Delay
- Logical Inputs Accept either 3.3V or 5.0V Levels
- Ultra-Low Power Dissipation
- +3.3V or 5.0V Supply Operations
- Individual Transmit Channel Over Temperature Protection

APPLICATIONS

- SDH Multiplexer
- Digital Cross Connects

GENERAL DESCRIPTION

The XRT5894 is an optimized four channel 3.3V line interface unit fabricated using low power CMOS technology. The device contains four independent E1 channels. Each channel performs the driver and receiver functions necessary to convert bipolar signals to logical levels and vice versa. The device requires transformers on both receiver and transmitter sides, and supports both balanced and unbalanced interfaces.

The device offers two distinct modes of LOS detection. The first method, which does not require an external clock, provides an LOS output indication signal with thresholds and delay that comply with the ITU G.775 requirements. In the second mode, the user provides an external clock that increases the delay for LOS declaration and clearing. This feature provides the user with the flexibility to implement LOS specifications that require a delay greater than the G.775 requirements.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRT5894IV	64 Lead TQFP (10 x 10 x 1.4mm)	-40°C to +85°C

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

BLOCK DIAGRAM

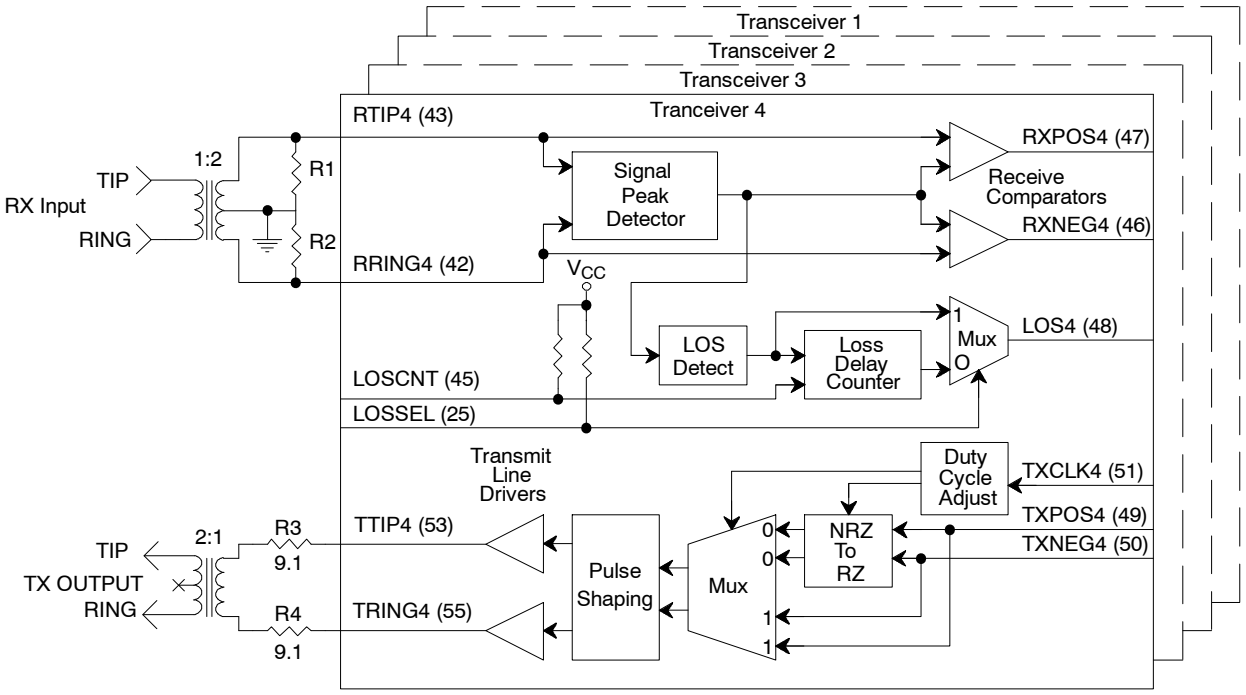


Figure 1. XRT5894 Block Diagram

Receiver Notes

- The same type 1:2CT ratio transformer may be used at the receiver input and transmitter output.
- R1 and R2 are both 150Ω for 75Ω operation, or 240Ω for 120Ω operation.
- Return loss exceeds ITU G.703 specification with these resistors and a 1:2CT ratio input transformer.

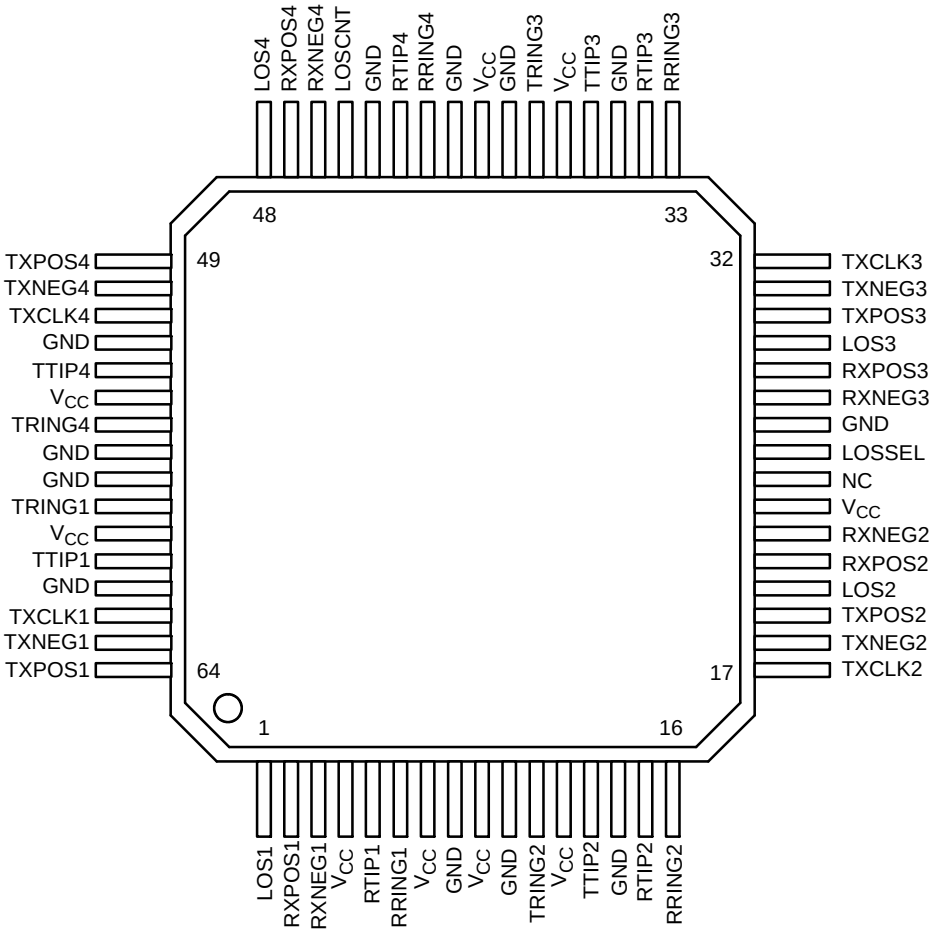
LOS (Loss of Signal) Notes

- LOSSEL (pin 25) is connected to logic 1 for ITU G.775 compliant LOS delay, or to logic 0 for user programmable additional delay.
- LOSCNT (pin 45) is unconnected when LOSSEL is logic 1, or connected to an external clock when LOSSEL is logic 0.

Transmitter Notes

- Return loss exceeds ETSI 300 166 specification with a 1:2 ratio transformer.
- R3 and R4 are always 9.1Ω for both 75Ω and 120Ω applications.

PIN CONFIGURATION



64 LEAD THIN QUAD FLAT PACK
(10 x 10 x 1.4 mm, TQFP)

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	LOS1	O	**Receiver 1 Loss of Signal.** Asserted during LOS condition.
2	RXPOS1	O	**Receiver 1 Positive Data Out.** Positive RZ data output for channel 1.
3	RXNEG1	O	**Receiver 1 Negative Data Out.** Negative RZ data output for channel 1.
4	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Digital circuitry.
5	RTIP1	I	**Receiver 1 Positive Bipolar Input.**
6	RRING1	I	**Receiver 1 Negative Bipolar Input.**
7	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Analog circuitry.
8	GND		**Analog Ground.**
9	V_{CC}		**Positive Supply. (+3.3V or +5.0V ± 5%).** Analog circuitry.
10	GND		**Analog Ground.**
11	TRING2	O	**Transmitter 2 Negative Bipolar Output.**
12	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Transmitter channel 2.
13	TTIP2	O	**Transmitter 2 Positive Bipolar Output.**
14	GND		**Analog Ground.** Transmitter channel 2.
15	RTIP2	I	**Receiver 2 Positive Bipolar Input.**
16	RRING2	I	**Receiver 2 Negative Bipolar Input.**
17	TXCLK2	I	**Transmitter 2 Clock Input.** Use for clocked mode with NRZ data.[1]
18	TXNEG2	I	**Transmitter 2 Negative Data Input.** Negative NRZ or RZ data input.[1]
19	TXPOS2	I	**Transmitter 2 Positive Data Input.** Positive NRZ or RZ data input.[1]
20	LOS2	O	**Receiver 2 Loss of Signal.** Asserted during LOS condition.
21	RXPOS2	O	**Receiver 2 Positive Data Out.** Positive RZ data output for channel 2.
22	RXNEG2	O	**Receiver 2 Negative Data Out.** Negative RZ data output for channel 2.
23	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Digital circuitry.
24	NC		**No Connect.**
25	LOSSEL	I	**Loss of Signal Delay Select.** "Hi" selects G.775, "Lo" selects user programmable.[1]
26	GND		**Digital Ground.**
27	RXNEG3	O	**Receiver 3 Negative Data Out.** Negative RZ data output for channel 3.
28	RXPOS3	O	**Receiver 3 Positive Data Out.** Positive RZ data output for channel 3.
29	LOS3	O	**Receiver 3 Loss of Signal.** Asserted during LOS condition.
30	TXPOS3	I	**Transmitter 3 Positive Data Input.** Positive NRZ or RZ data input.[1]
31	TXNEG3	I	**Transmitter 3 Negative Data Input.** Negative NRZ or RZ data input.[1]
32	TXCLK3	I	**Transmitter 3 Clock Input.** Use for clocked mode with NRZ data.[1]
33	RRING3	I	**Receiver 3 Negative Bipolar Input.**
34	RTIP3	I	**Receiver 3 Positive Bipolar Input.**

Note:
[1] *Has internal pull-up 50KΩ resistor.*

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Type	Description
35	GND		**Analog Ground.**
36	TTIP3	O	**Transmitter 3 Positive Bipolar Output.**
37	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Transmitter channel 3.
38	TRING3	O	**Transmitter 3 Negative Bipolar Output.**
39	GND		**Analog Ground.** Transmitter channel 3.
40	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Analog circuitry.
41	GND		**Analog Ground.**
42	RRING4	I	**Receiver 4 Negative Bipolar Input.**
43	RTIP4	I	**Receiver 4 Positive Bipolar Input.**
44	GND		**Analog Ground.**
45	LOSCNT	I	**Loss of Signal Timing Clock Input.** For user−programmable LOS delay.[1]
46	RXNEG4	O	**Receiver 4 Negative Data Out.** Negative RZ data output for channel 4.
47	RXPOS4	O	**Receiver 4 Positive Data Out.** Positive RZ data output for channel 4.
48	LOS4	O	**Receiver 4 Loss of Signal.** Asserted during LOS condition.
49	TXPOS4	I	**Transmitter 4 Positive Data Input.** Positive NRZ or RZ data input.[1]
50	TXNEG4	I	**Transmitter 4 Negative Data Input.** Negative NRZ or RZ data input.[1]
51	TXCLK4	I	**Transmitter 4 Clock Input.** Use for clocked mode with NRZ data.[1]
52	GND		**Analog Ground.** Transmitter channel 4.
53	TTIP4	O	**Transmitter 4 Positive Bipolar Output.**
54	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Transmitter channel 4.
55	TRING4	O	**Transmitter 4 Negative Bipolar Output.**
56	GND		**Digital Ground.**
57	GND		**Analog Ground.**
58	TRING1	O	**Transmitter 1 Negative Bipolar Output.**
59	V_{CC}		**Positive Supply (+3.3V or +5.0V ± 5%).** Transmitter channel 1.
60	TTIP1	O	**Transmitter 1 Positive Bipolar Output.**
61	GND		**Analog Ground.** Transmitter channel 1.
62	TXCLK1	I	**Transmitter 1 Clock Input.** Use for clocked mode with NRZ data.[1]
63	TXNEG1	I	**Transmitter 1 Negative Data Input.** Negative NRZ or RZ data input.[1]
64	TXPOS1	I	**Transmitter 1 Positive Data Input.** Positive NRZ or RZ data input.[1]

Note:
[1] Has internal pull-up 50KΩ resistor.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 3.3V or 5.0V ± 5%, T_A = -40 to 25 to 85°C, Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DC Electrical Characteristics						
Parameters						
V_{CC}	Voltage Supply	3.135	3.3	3.465	V	3.3V Operation
V_{CC}	Voltage Supply	4.75	5.0	5.25	V	5V Operation
Inputs						
V_{IH}	Input High Level	2.0		5.0	V	
V_{IL}	Input Low Level			0.8	V	
Outputs						
V_{OH}	Output High Level	2.4			V	I_{OH} = -4mA
V_{OL}	Output Low Level			0.4	V	I_{OL} = 4mA
Receiver Specifications						
RX_{CL}	Allowable Cable Loss	0	10	12	dB	Cable loss at 1.024MHz (Relative to 0dB = 2.37Vp measured from RTIP or RRING to ground).
RX_{IM}	Interference Margin	-15	-12		dB	With 6dB cable loss
RX_{XI}	Receiver Slicing Threshold	**45**	50	**55**	%	% of peak input voltage at -3dB cable loss
RX_{LOSSET}	LOS Must Be Set If RX Sig. Atten. ² 32dB (For Any Valid Data Pattern)		15	32	dB	Relative to 0dB = 2.37Vp Measured from RTIP or RRING to ground.
RX_{LOSCLR}	LOS Must Be Cleared If RX Sig. Atten. < 9dB	9	12		dB	Relative to 0dB = 2.37Vp measured from RTIP or RRING to ground.
$RX_{LOSHYST}$	Hysteresis on Input Data	1			dB	For LOS output state change
RX_{IN}	Input Impedance	5			kΩ	Up to 3.072MHz (Measured from RTIP or RRING to ground).
Power Specifications V_{CC} = 3.3V						
P_D	Power Dissipation		460	590	mW	All 1's Transmit and Receive 75Ω
P_D	Power Dissipation		117	155	mW	All Drivers Power Down
P_C	Power Consumption 75Ω		770	900	mW	All 1's Transmit and Receive
P_C	Power Consumption 75Ω		555	675	mW	50% data density, Transmit and Receive
P_C	Power Consumption 120Ω		635	780	mW	All 1's Transmit and Receive
P_C	Power Consumption 120Ω		475	605	mW	50% data density, Transmit and Receive
Power Specifications V_{CC} = 5.0V						
P_D	Power Dissipation		945	1240	mW	All 1's Transmit and Receive 75Ω
P_D	Power Dissipation		235	290	mW	All Drivers Power Down
P_C	Power Consumption 75Ω		1250	1555	mW	All 1's Transmit and Receive

Note:
Bold face parameters are covered by production test and guaranteed over operating temperature range.

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: V_{CC} = 3.3V or 5.0V ± 5%, T_A = -40 to 25 to 85°C, Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Power Specifications V_{CC} =5.0V (Cont'd)						
P_C	Power Consumption 120Ω		1075	1345	mW	All 1's Transmit and Receive
P_C	Power Consumption 75Ω		1025	1300	mW	50% data density, Transmit and Receive
P_C	Power Consumption 120Ω		940	1220	mW	50% data density, Transmit and Receive
AC Electrical Characteristics						
V_{TXOUT}	Output Pulse Amplitude (R_L = 75Ω)	**2.13**	2.37	**2.60**	V	Trans. = 1:2 ratio, 9.1Ω in series with each end of primary
V_{TXOUT}	Output Pulse Amplitude (R_L = 120Ω)	2.70	3.0	3.30	V	Trans. = 1:2 ratio, 9.1Ω in series with each end of primary
T_{XPW}	Output Pulse Width	**224**	244	**264**	ns	
PN_{IMP}	Pos/Neg Pulse Unbalanced		5		%	
T_1	TXCLK Clock Period (E1)		488		ns	
T_2	TXCLK Duty Cycle	**30**	50	**70**	%	
T_{SU}	Data Set-up Time, TDATA to TXCLK	**75**			ns	50% TXCLK Duty Cycle
T_{HO}	Data Hold Time, TDATA to TXCLK	**30**			ns	50% TXCLK Duty Cycle
T_R	TXCLK Rise Time (10% to 90%)		40		ns	
T_F	TXCLK Fall Time (10% to 90%)		40		ns	
$T_{3\text{-noclk}}$	Data Prop. Delay No-Clock Mode		35	50	ns	
$T_{3\text{-clk}}$	Data Prop. Delay Clock Mode		470		ns	50% TXCLK Duty Cycle
T_4	Receive Data High	**219**	244	**269**	ns	0dB Cable Loss
T_5	RX Data Prop. Delay			40	ns	15pF Load
T_6	Receive Rise Time			40	ns	15pF Load
T_7	Receive Rise Time			40	ns	15pF Load

Note:
Bold face parameters are covered by production test and guaranteed over operating temperature range.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -40°C to +85°C
Supply Voltage . . . . . -0.3V to +6.0V
ESD Protection . . . . . >1000V (HBM)

Disabling Output Drivers

Output drivers may be individually disabled (hi-z output) by either of the following methods.

1. Either connect the transmit data inputs TXPOS and TXNEG for the channel to be disabled to a logic 1 source (VCC), or allow them to float (inputs have internal pull–up resistors).
2. Connect TXCLK for the channel to be disabled to logic 0 source (Ground), and also apply data to the TXPOS and TXNEG inputs of that channel.

TRANSFORMER REQUIREMENTS

Turns Ratio	Line Impedance
1:2 CT	75Ω or 120Ω

Table 1. Input Transformer Requirements

Turns Ratio	Line Impedance
1:2	75Ω or 120Ω

Table 2. Output Transformer Requirements

Note:
The same type 1:2 CT ratio device may be used at both receiver input and transmitter output.

The following transformers have been tested with the XRT5894:

HALO type TG26-1205(package contains two 1 CT:2 CT ratio transformers)
Pulse type PE-65535 (1:2 CT ratio)
Transpower Technologies type TTI 7154-R (1:2 CT ratio)

Magnetic Supplier Information:

HALO Electronics, Inc.
P.O. Box 5826
Redwood City, CA 94063
Tel. (415) 568-5800
Fax. (415)568-6161

Pulse
Telecom Product Group
P.O. Box 12235
San Diego, CA 92112
Tel. (619) 674-8100
Fax. (619) 674-8262

Transpower Technologies, Inc.
24 Highway 28, Suite 202
Crystal Bay, NV 89402–0187
Tel. (702) 831–0140
Fax. (702) 831–3521

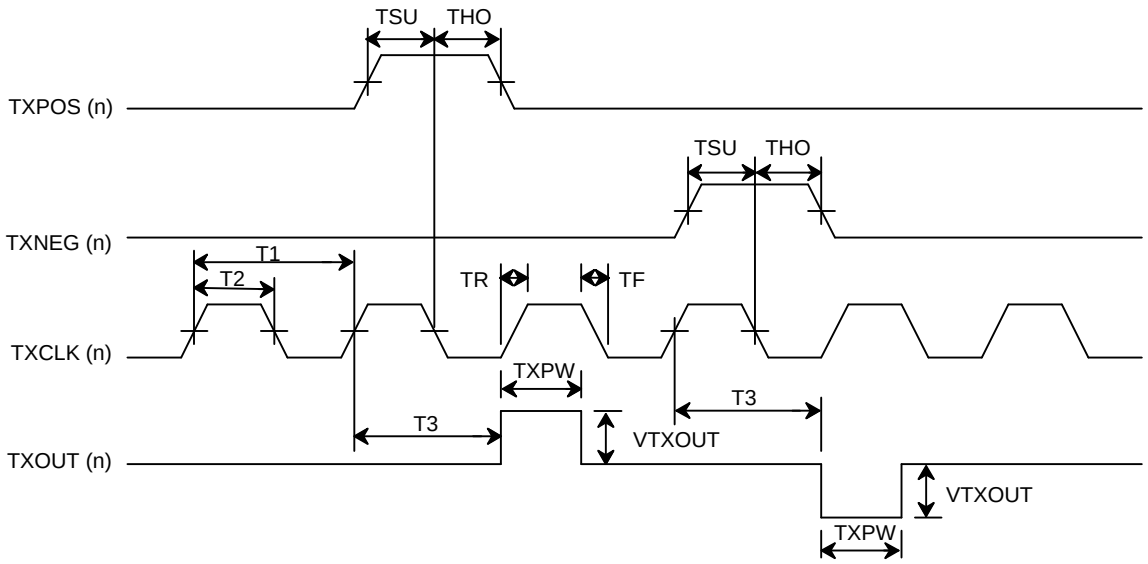


Figure 2. Transmit Timing Diagram

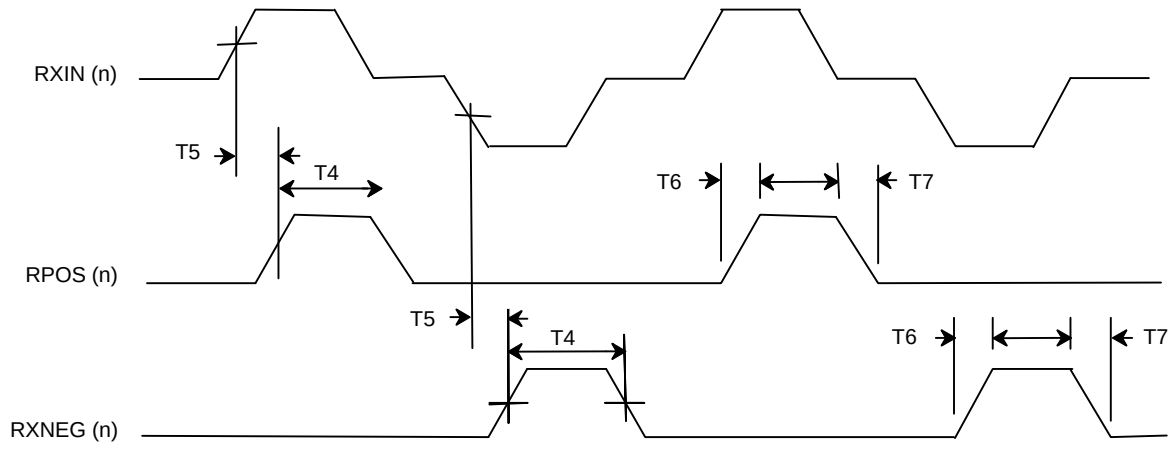


Figure 3. Receive Timing Diagram

RETURN LOSS SPECIFICATIONS

The following transmitter and receiver return loss specifications are based on a typical 1:2CT ratio transformer.

Frequency Range	75Ω		120Ω		Unit
	Min.	Typ.	Min.	Typ.	
51kHz to 102kHz	16	22	10	15	dB
102kHz to 2.048MHz	16	22	10	15	dB
2.048MHz to 3.072MHz	11	18	10	14	dB

Table 3. Transmitter Return Loss Specification

Transmit Return Loss Notes

- Output transformer ratio is 1:2 (return loss exceeds ETSI 300 166 with this transformer).
- For both 75Ω and 120Ω applications, 9.1Ω, 1% resistors are connected between each end of the transformer primary and the XRT5894 TTIP and TRING pins.

Frequency Range	75Ω		120Ω		Unit
	Min.	Typ.	Min.	Typ.	
51kHz to 102kHz	16	28	15	18	dB
102kHz to 2.048MHz	22	34	22	25	dB
2.048MHz to 3.072MHz	18	26	20	30	dB

Table 4. Receiver Return Loss Specification

Receiver Return Loss Notes

- Input transformer ratio is 1:2 CT.
- Transformer center tap is grounded.
- Each half of transformer secondary is terminated with 150Ω for 75Ω operation, or 240Ω for 120Ω operation (resistors are 1% tolerance).

SYSTEM DESCRIPTION

This device is a four channel E1 transceiver that provides an electrical interface for 2.048Mbps applications. Its unique architecture includes four receiver circuits that convert ITU G.703 compliant bipolar signals to TTL compatible logic levels. Each receiver includes a LOS (Loss of Signal) detection circuit that may be configured for either a fixed or a user-programmable LOS response time delay. Similarly, in the transmit direction, four transmitters convert TTL compatible logic levels to G.703 compatible bipolar signals. Each transmitter may be operated either with RZ, or NRZ data types. In NRZ mode a transmit clock is required as well. The following description applies to any of the four receivers or transmitters contained in the XRT5894. Therefore, the suffix numbers for a particular channel are deleted for simplicity. i.e. "RTIP" applies to RTIP1 through RTIP4.

Receiver Operation

A bipolar signal is transformer-coupled to the receiver differential inputs (RTIP and RRING). The receiver is able to tolerate up to 12dB of line loss measured at 1.024MHz. It contains slicing circuitry that automatically samples the incoming data at a fixed percentage (50% nominal) of the peak signal amplitude. A precision peak detector maintains the slicing level accuracy. The TTL compatible receiver output data rails appear at the RXPOS and RXNEG pins. The pulse width of this data; which is in RZ format, is a function of the amount of the cable loss present.

Receiver Loss Of Signal Detection (LOS)

Absence of signal at any receiver input is detected by the loss of signal (LOS) circuit. One LOS detection circuitry is provisioned for each receiver. The LOS signal is asserted (LOS=1) when a LOS condition is detected and is cleared (LOS=0) when a valid input signal is restored.

Two modes of LOS circuit operation are supported. These distinct modes are called "automatic" and "user-programmable". When LOSSEL (pin 25) is set to logic "1", the automatic mode is selected. In this mode the LOS condition will be declared and cleared in full compliance with ITU G.775 specification. When LOSSEL is connected to logic "0", the user-programmable delay mode is enabled. In this mode the user has the option of extending the delay of LOS declaration and clearing specified in the ITU G.775. This is done by providing a user-supplied clock to LOSCNT (pin 45). The "user programmable mode" is provisioned to allow systems designers to comply with older versions of LOS specifications in legacy systems. It needs to be stressed that the delay for declaration and clearing of the LOS condition will never be less than the range specified in the G.775 specification (10-255 pulse intervals).

The LOS detection/clearing circuitry of the XRT5894 in "automatic" mode will detect LOS when the incoming signal has "no transitions" i.e. when the signal level is less than or equal to a signal level A_D dB below nominal signal level, for N consecutive pulse intervals, where $10 \leq N \leq 255$. The value of A_D can vary between 10dB to 32dB depending on the ones density of the incoming signal assuming the received data has minimum permissible ones density. Furthermore LOS detect is cleared when the incoming signal has "transitions," i.e. when the signal level is greater than or equal to a signal level of A_C dB below nominal, for N consecutive pulse intervals, where $10 \leq N \leq 255$. The value of A_C can vary between 9dB to 31dB depending on the ones density of the incoming signal assuming the received data has minimum permissible ones density. Each pulse interval is 488ns at E1 rates. The absolute value of A_C is always smaller than A_D by at least 1dB.

The LOS detection/clearing criteria described above is fully compliant with G.775 LOS specification. In the "user programmable" mode the user has the option of extending the declaration and clearing delay ($10 \leq N \leq 255$) by an amount which is equal to 2048 x T. T is the time period of the clock supplied to LOSCNT (pin 45) by the user.

Nominal signal level is defined as 2.37V peak measured between RTIP or RRING and ground. (This voltage will be present in 75Ω applications using a 1:2 CT ratio input transformer terminated in 300Ω with the center tap grounded with 0dB of cable and a 2.37V peak amplitude transmit pulse at the cable input.)

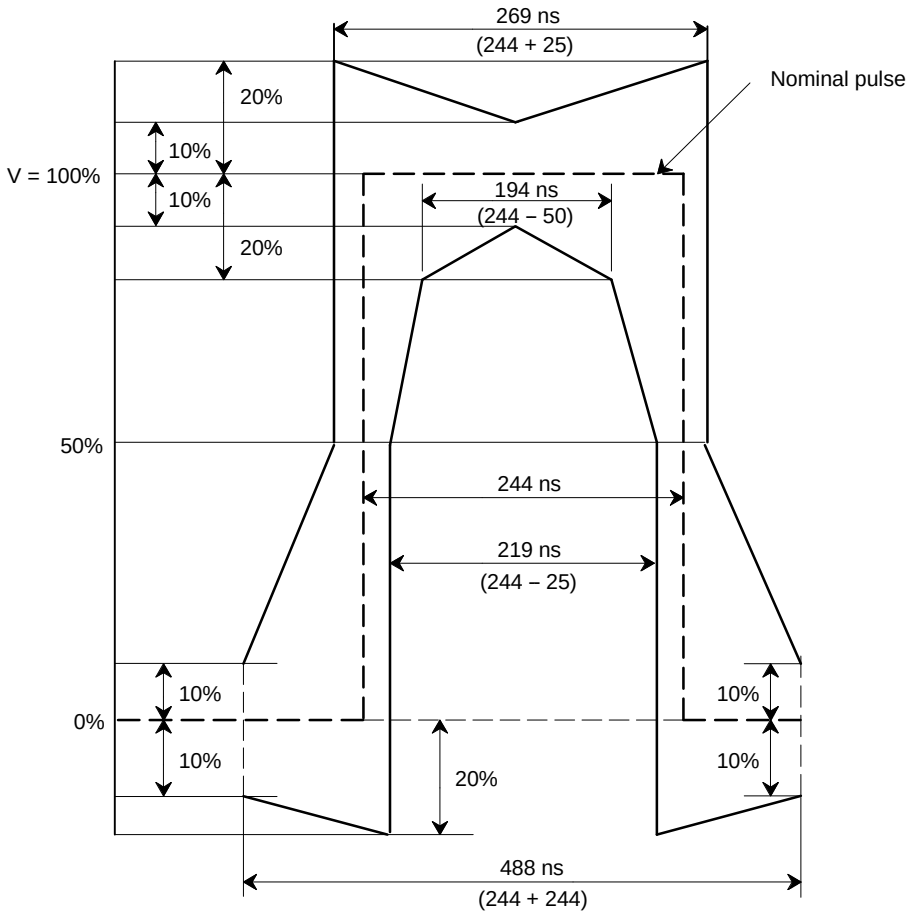
Transmitters

This device contains four identical ITU G.703 compliant transmitters. The output stage of each transmitter is a differential voltage driver. External resistors need to be connected to the primary of output transformer. This is necessary to maintain an accurate source impedance

that ensures compliance to ETSI 300 166 return loss requirement.

TTL compatible dual rail transmit data signals are supplied to TXPOS and TXNEG inputs. The transmitter differential outputs TTIP and TRING are connected to the output transformer primary through series 9.1Ω resistors.

All the four transmitters can be operated in two distinct modes of operation referred to as “clocked” or “clockless” modes. The operational mode is selected automatically based on the signal provided to TXCLK input. If a clock is present at this pin, the transmitter detects its presence and operates in the clocked mode. In this mode, the transmit input should be supplied with full-width NRZ pulses. If a clock is not present at the TXCLK input (pin is left open), the part operates in the clockless mode. In this mode, RZ data should be supplied to the device. Each transmit channel of XRT5894 has a duty cycle correction circuitry. This enables the device to produce output bipolar pulses fully compliant with G.703 despite having TXCLK signal with 30% to 70% duty cycle.



Note: *V corresponds to the nominal peak value*

Figure 4. CCITT G.703 Pulse Template

Transmitter Output Pulse Measurement

Figure 5 shows a typical transmit pulse plotted on the template shown in ITU G.703 Figure 15/G.703. The following conditions apply:

V_{CC}=3.30V

Transmitter output transformer secondary terminated with 120Ω

All ones signal

Receiver output looped backed into transmitter digital input

Operation without transmitter clock (RZ data)

Measurement made with a Tektronix TDS640 digital scope set to full bandwidth

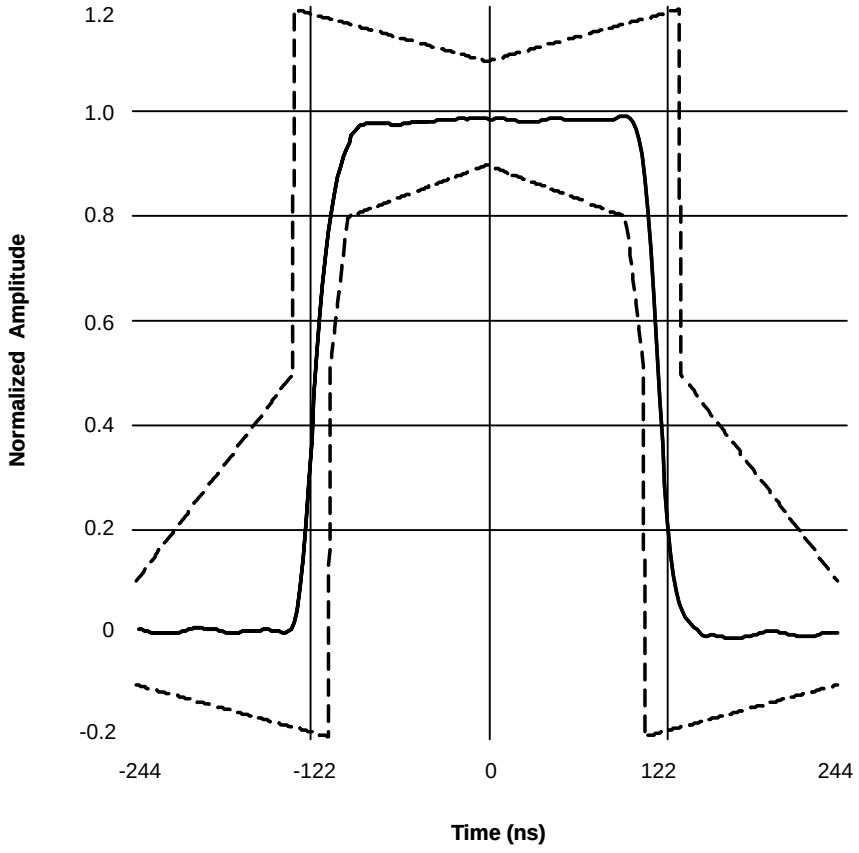


Figure 5. XRT5894 Output Pulse

Transmitter Output Return Loss Measurements

The following measurements were made with a Wandel and Goltermann SNA–2 Network Analyzer equipped with an RFZ–1 75Ω Return Loss Bridge. A 75Ω to 120Ω impedance matching transformer was used to make the 120Ω measurement. A network analyzer calibration run subtracted out the effects of this transformer.

Test Conditions:

- Output transformer ratio was 1:2.
- Transmitter series resistors (R3 and R4 in *Figure 1*) were 9.1Ω .
- Device was powered from a 3.3V source, transmitter was enabled, and no output data was present.

This configuration was used for both 75Ω and 120Ω measurements. The only change was the termination resistance provided by the return loss bridge.

Test Results:

Table 5 compares measured output return loss with requirements in ETSI FINAL DRAFT prETS 300 166, June 1993. These results show that measured return loss is mainly determined by the characteristics of the output transformer. This is particularly evident for the 120Ω load where the measured result is better than the calculated value.

Specified Frequency	Frequency (KHz)	ETSI Spec. (Min. dB)	Meas. Value (dB) 75Ω Load	Meas. Value (dB) 120Ω Load
0.025 fb	51.2	6	22.6	15.4
0.05 fb	102.4	8	22.6	15.7
1.5 fb	3072	8	18.0	14.6

Table 5. Transmitter Output Return Loss Measurements

Notes:

fb = 2048KHz

This data shows that the XRT5894 is fully compliant with the ETSI Output Return Loss Specification for E1 operation with either 75Ω or 120Ω loads.

The following pictures show typical results of measurements that made over a 50 KHz to 3.5MHz frequency range.

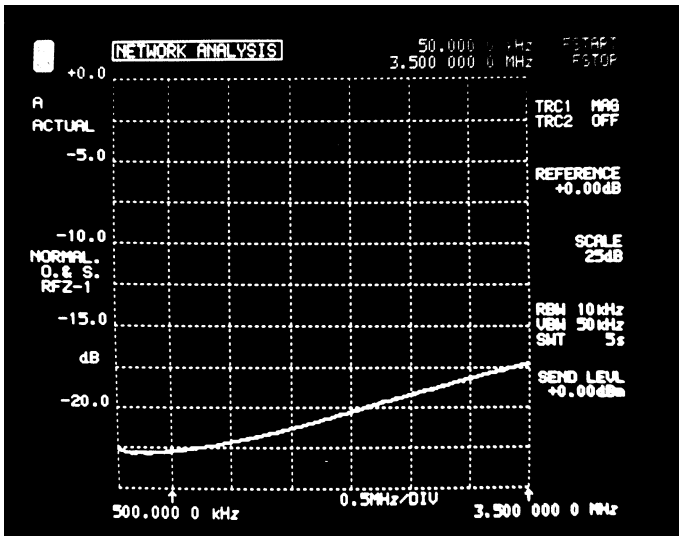


Figure 6. 75Ω Return Loss Measurement

Figure 6 shows a return loss better than 20dB at low frequencies that decreases to about 12dB at 3.5MHz. Since the source and load resistances are well–matched, the return loss degradation is due to the transformer.

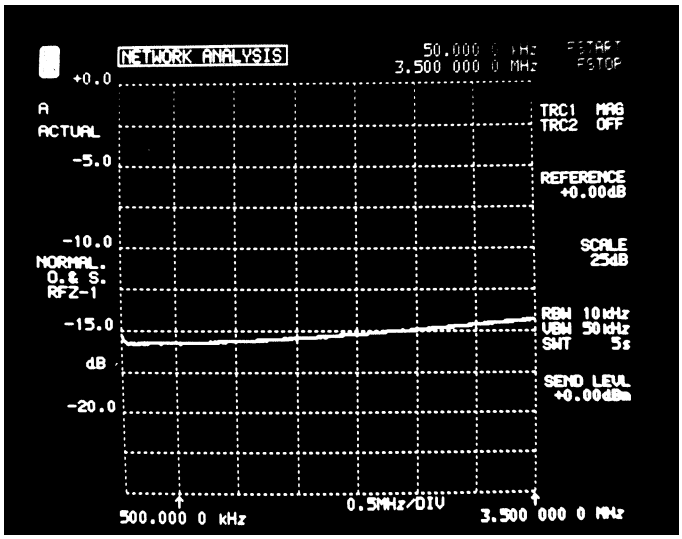


Figure 7. 120Ω Return Loss Measurement

Figure 7 shows that for the 120Ω case, transformer characteristics improve return loss at lower frequencies. At 3.5 MHz, return loss is close to the calculated 13.8dB for a 75Ω source terminated with 120Ω.

Output Transformer Selection

A 1:2 ratio transformer is recommended for both 75Ω and 120Ω operation because the transmitter, when equipped with this device, meets both the ITU G.703 output pulse amplitude requirement and, the ETSI return loss specification. Although a center−tapped output transformer is not required, choosing a part with a center-tapped secondary allows the use of the same type of unit at the receiver input.

A theoretical justification for the 1:2 ratio transformer follows:

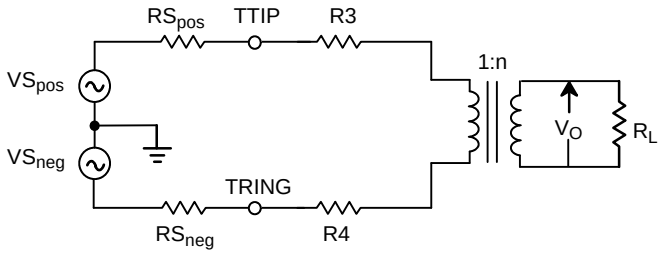


Figure 8. Transmitter Line Driver Model

Where:

$Vs_{pos} = Vs_{neg} = 1.25V$ typical (Differential line driver peak output voltage swing)

$Rs_{pos} = Rs_{neg} = 0.8\Omega$ typical (Differential line driver internal source resistance)

$R3 = R4 = 9.1\Omega$ (Differential line driver external source resistance from *Figure 1*)

$R_L = 75\Omega$ or 120Ω (Transmitter load resistance)

n = 2 (Transformer turns ratio)

Vo = Transmitter peak output voltage (Measured across $R_L = 75\Omega$ or $R_L = 120\Omega$)

Figure 9 may be converted to a single−ended model:

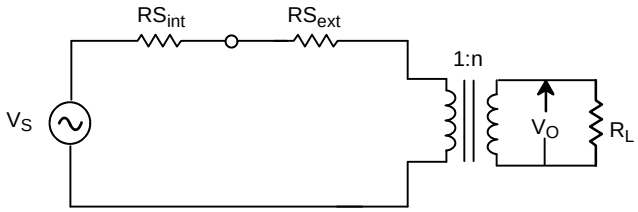


Figure 9. Single-ended Line Driver Model

Where:

$VS = |Vs_{pos}| + |Vs_{neg}|$

$RS_{int} = RS_{pos} + Rs_{neg}$

$RS_{ext} = R3 + R4$

This may be further simplified:

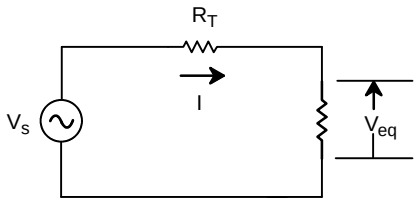


Figure 10. Equivalent Circuit

Where:

$$R_T = RS_{int} + Rs_{ext}$$

$$R_{eq} = \frac{R_L}{n^2}$$

Therefore:

$$I = \frac{Vs}{R_T + Req}$$

$$V_{eq} = I\ R_{eq}$$

$$V_o = n\ V_{eq}$$

And:

$$\text{Return Loss} = 20 \log \left| \frac{R_T + R_{eq}}{R_T - R_{eq}} \right|$$

Table 5 contains the results of calculations made with these equations. The numbers show that output pulse amplitude is within millivolts of the nominal values of 2.37V and 3.00V specified by ITU G.703 for 75Ω and 120Ω operation. Also, the 1:2 ratio transformer provides an almost-perfect match for 75Ω operation, and return loss is well within the ETSI specification for the 120Ω load.

Load Resistance R_L (Ω)	Pulse Amplitude Vo (Volts Peak)	Output Return Loss (dB)
75	2.43	31.3
120	3.01	13.8

Table 5. Calculated Transmitter Pulse Amplitude and Return Loss

64 LEAD THIN QUAD FLAT PACK (10 x 10 x 1.4 mm, TQFP)

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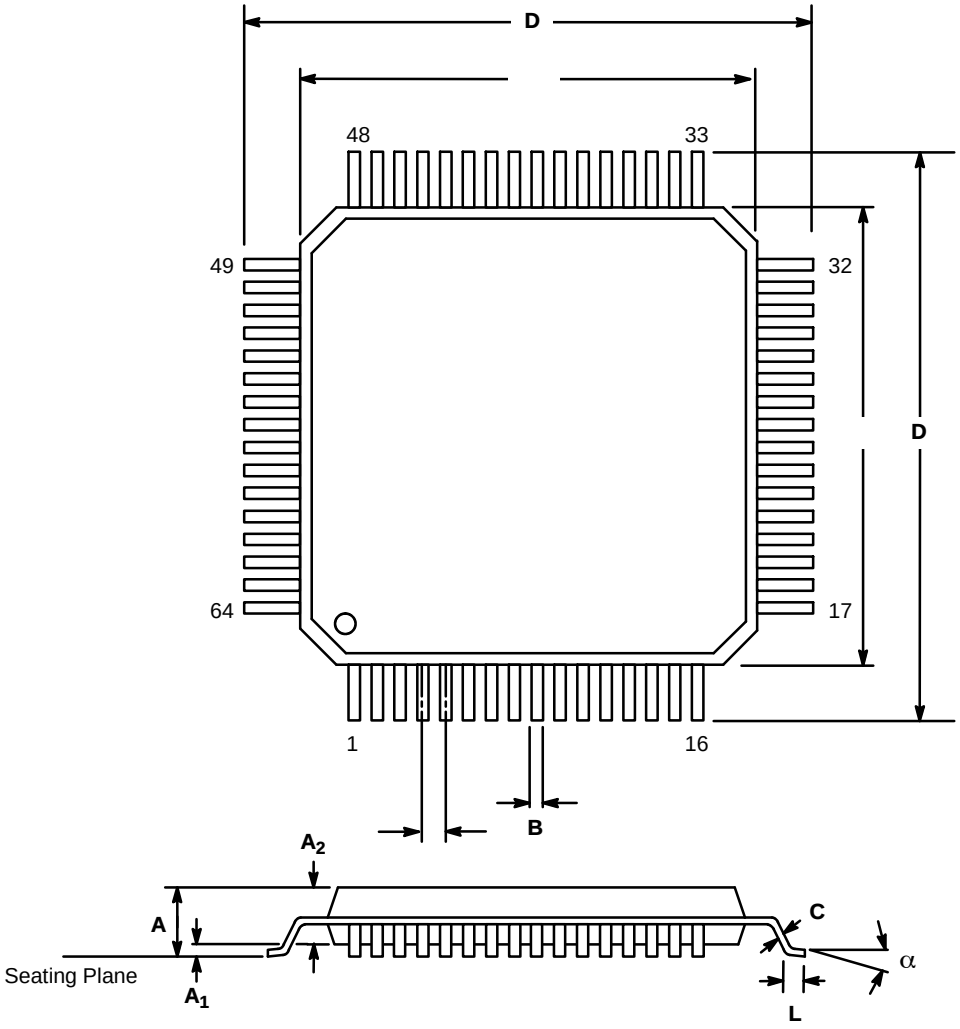

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.005	0.009	0.13	0.23
C	0.004	0.008	0.09	0.20
D	0.465	0.480	11.80	12.20
D_1	0.390	0.398	9.90	10.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

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