FAIRCHILD SEMICONDUCTOR®

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74ABT16374
16-Bit D-Type Flip-Flop with 3-STATE Outputs

General Description

The ABT16374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable ($\overline{OE}$) are common to each byte and can be shorted together for full 16-bit operation.

Features

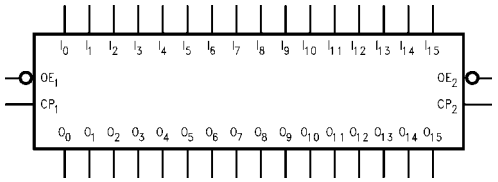
- Separate control logic for each byte
- 16-bit version of the ABT374
- Edge-triggered D-type inputs
- Buffered Positive edge-triggered clock
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Guaranteed latch-up protection

Ordering Code:

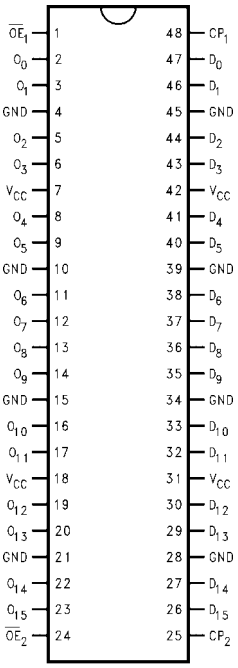
Order Number	Package Number	Package Description
74ABT16374CSSC	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74ABT16374CMTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Name	Description
$\overline{OE}_n$	3-STATE Output Enable Input (Active LOW)
CP_n	Clock Pulse Input (Active Rising Edge)
D_0–D_{15}	Data Inputs
O_0–O_{15}	3-STATE Outputs

Functional Description

The ABT16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable ($\overline{OE}_n$) LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}_n$ is HIGH, the outputs go to the high impedance state. Operation of the OE_n input does not affect the state of the flip-flops.

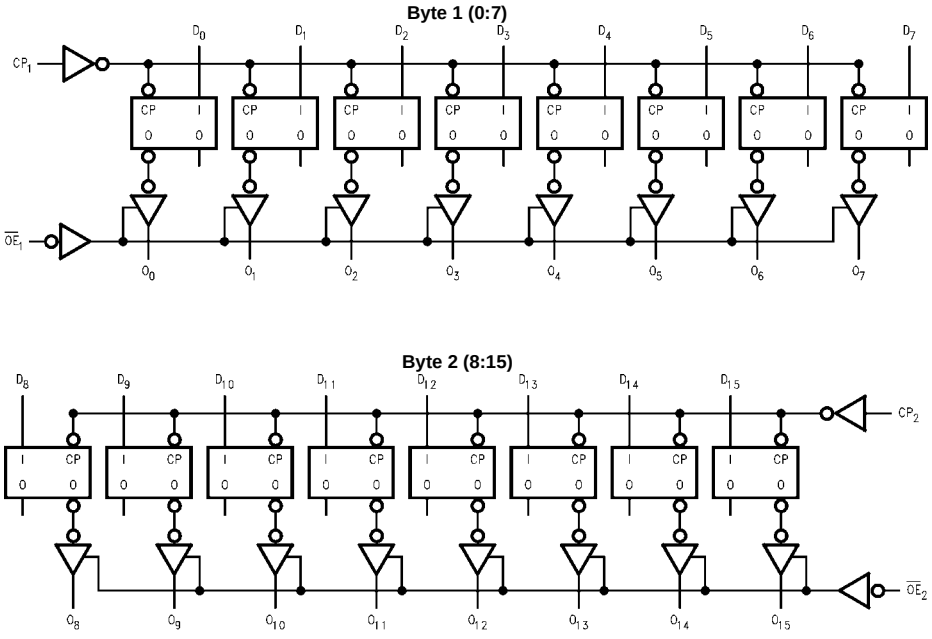
Truth Tables

Inputs			Outputs
CP_1	$\overline{OE}_1$	D_0–D_7	O_0–O_7
⌐	L	H	H
⌐	L	L	L
L	L	X	(Previous)
X	H	X	Z

Inputs			Outputs
CP_2	$\overline{OE}_2$	D_8–D_{15}	O_8–O_{15}
⌐	L	H	H
⌐	L	L	L
L	L	X	(Previous)
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or	
Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current:	
$\overline{OE}$ Pin	−350 mA
(Across Comm Operating Range)	
Other Pins	−500 mA
Over Voltage Latchup (I/O)	10V

Recommended Operating Conditions

Free Air Ambient Temperature	−40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate (ΔV/Δt)	
Data Input	50 mV/ns
Enable Input	20 mV/ns
Clock Input	100mV/ns

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		2.5			V	Min	I_{OH} = −3 mA
			2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage				0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current				1	μA	Max	V_{IN} = 2.7V (Note 3)
					1			V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−1	μA	Max	V_{IN} = 0.5V (Note 3)
					−1			V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA
								All Other Pins Grounded
I_{OZH}	Output Leakage Current				10	μA	0–5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current				−10	μA	0–5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others V_{CC} or GND
I_{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				62	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{OE}$ = V_{CC}; All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			2.5	mA	Max	V_I = V_{CC} − 2.1V
		Outputs 3-STATE			2.5	mA		Enable Input V_I = V_{CC} − 2.1V
		Outputs 3-STATE			2.5	mA		Data Input V_I = V_{CC} − 2.1V
								All Others at V_{CC}or GND
I_{CCD}	Dynamic I_{CC} (Note 3)	No Load			0.30	mA/ MHz	Max	Outputs Open $\overline{OE}$ = GND, (Note 4) One Bit Toggling, 50% Duty Cycle

Note 3: Guaranteed, but not tested.

Note 4: For 8-bit toggling, I_{CCD} < 0.8 mA/MHz.

AC Electrical Characteristics

(SSOP Package)

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	150			150		MHz
t_{PLH}	Propagation Delay	1.8		6.2	1.8	6.2	ns
t_{PHL}	CP to O_n	1.8		5.9	1.8	5.9	
t_{PZH}	Output Enable Time	1.2		5.6	1.2	5.6	ns
t_{PZL}		1.6		5.3	1.6	5.3	
t_{PHZ}	Output Disable Time	2.2		7.1	2.2	7.1	ns
t_{PLZ}		2.2		6.6	2.2	6.6	

AC Operating Requirements

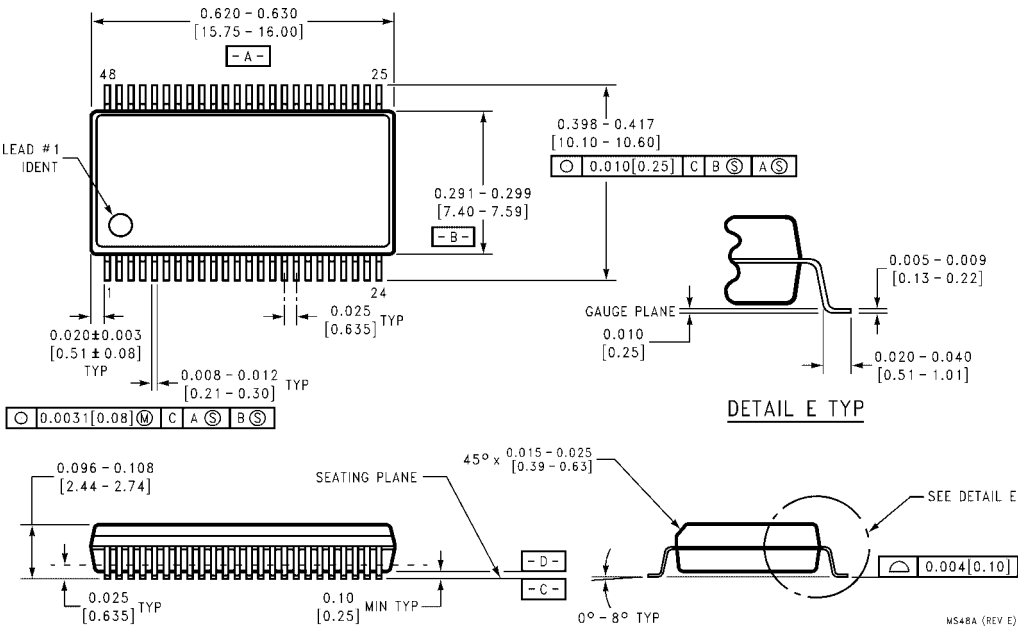
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50$ pF		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH	1.1		1.1		ns
$t_S(L)$	or LOW D_n to CP	1.1		1.1		
$t_H(H)$	Hold Time, HIGH	1.3		1.3		ns
$t_H(L)$	or LOW D_n to CP	1.3		1.3		
$t_W(H)$	Pulse Width, CP	3.0		3.0		ns
$t_W(L)$	HIGH or LOW	3.0		3.0		

Capacitance

Symbol	Parameter	Typ	Units	Conditions ($T_A = 25°C$)
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0V$
C_{OUT} (Note 5)	Output Capacitance	11.0	pF	$V_{CC} = 5.0V$

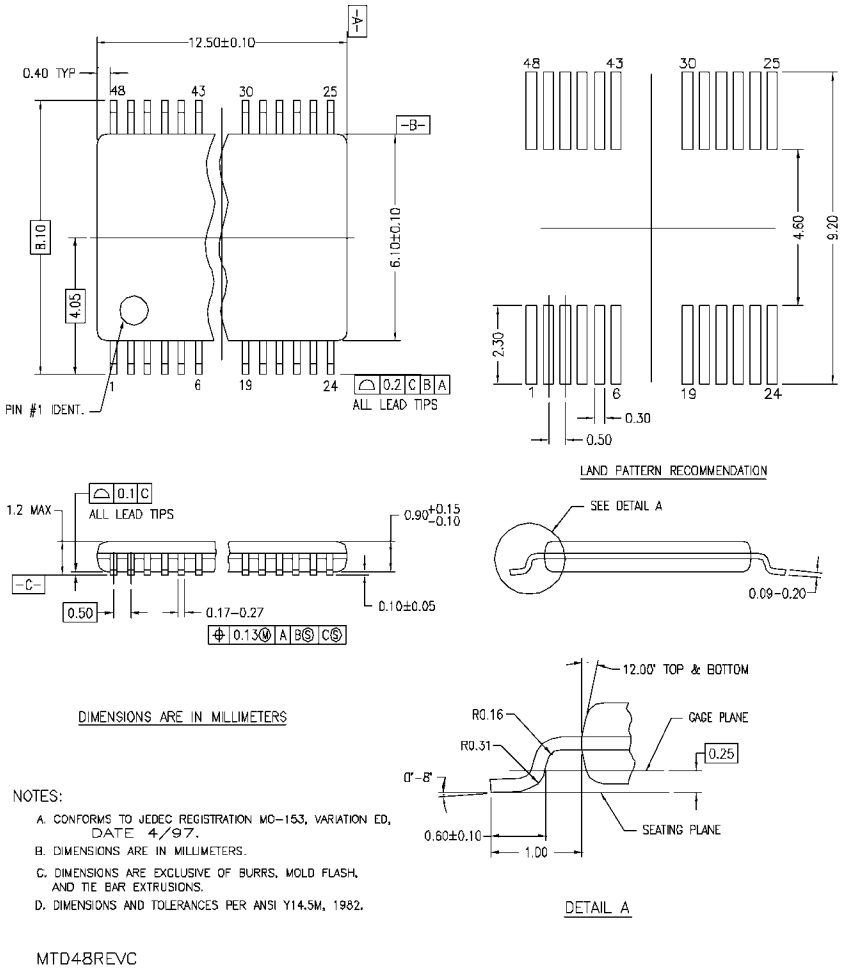
Note 5: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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