

# DATA SHEET

**74F240**

Octal inverting buffer (3-state)

Product data  
Supersedes data of 2002 Mar 18

2004 Feb 25

# Octal inverting buffer

# 74F240

## FEATURES

- Octal bus interface
- 3-state buffer outputs sink 64 mA
- 15 mA source current

## DESCRIPTION

The 74F240 is an octal inverting buffer that is ideal for driving bus lines of buffer memory address registers. The outputs are all capable of sinking 64 mA and sourcing up to 15 mA. The device features two output enables, each controlling four of the 3-state outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F240	4.3 ns	37 mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5 V \pm 10\%$ , $T_{amb} = 0\text{ }^{\circ}C$ to $+70\text{ }^{\circ}C$	
20-pin plastic DIP	N74F240N	SOT146-1
20-pin plastic SOL	N74F240D	SOT163-1
20-pin plastic SSOP II	N74F240DB	SOT339-1

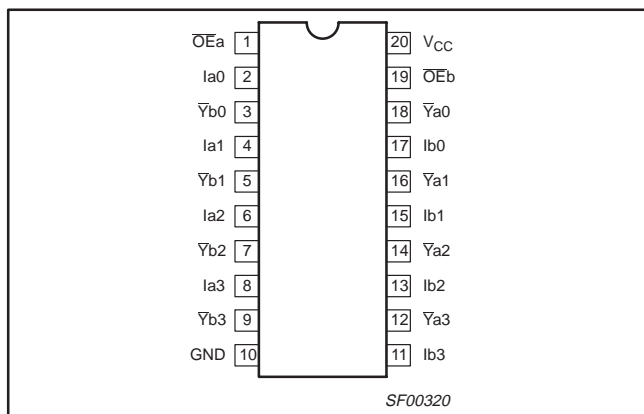
## INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.67	20 $\mu$ A/1.0 mA
$\overline{OE}a$ , $\overline{OE}b$	Output enable inputs (Active-LOW)	1.0/0.33	20 $\mu$ A/0.2 mA
$\overline{Y}an$ , $\overline{Y}bn$	Data outputs	750/106.7	15 mA/64 mA

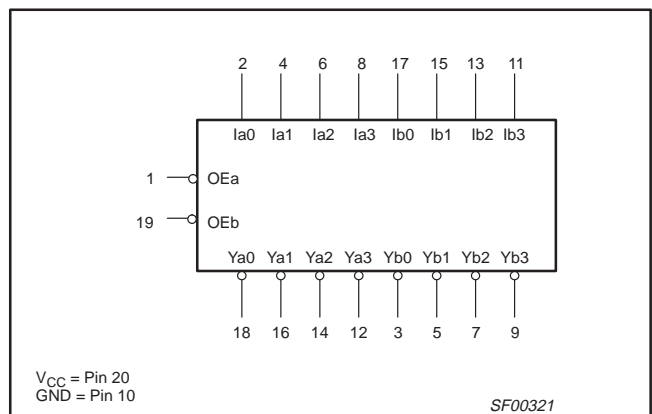
### Note to input and output loading and fan out table

One (1.0) FAST unit load is defined as: 20  $\mu$ A in the HIGH state and 0.6 mA in the LOW state.

## PIN CONFIGURATION



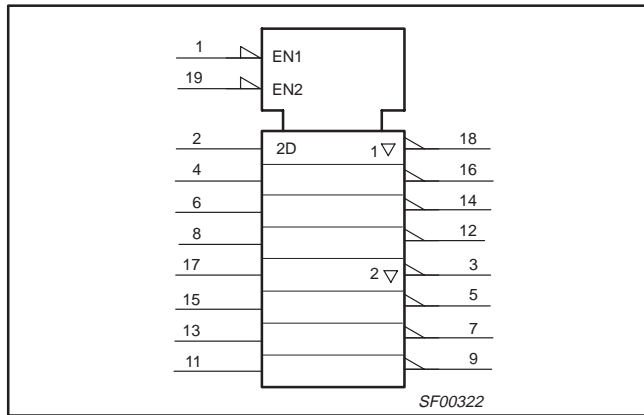
## LOGIC SYMBOL



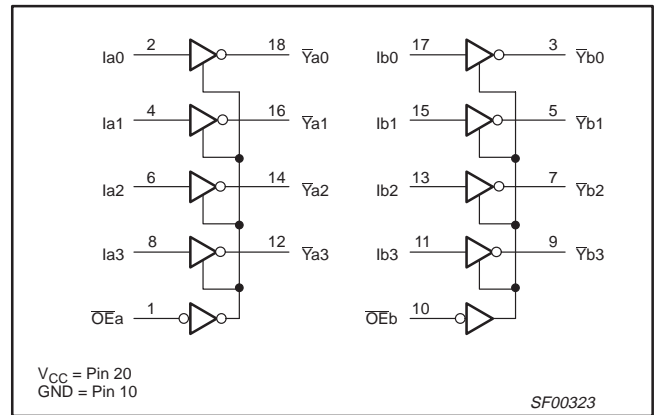
# Octal inverting buffer

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## IEC/IEEE SYMBOL



## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	$\overline{Y}a$	$\overline{Y}b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

### NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in high output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in low output state	128	mA
$T_{amb}$	Operating free air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{Ik}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-15	mA
$I_{OL}$	Low-level output current			64	mA
$T_{amb}$	Operating free air temperature range	0		+70	°C

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN; V <sub>IL</sub> = MAX; V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3 mA	±10%V <sub>CC</sub>	2.4		V
				±5%V <sub>CC</sub>	2.7	3.4	V
			I <sub>OH</sub> = -15 mA	±10%V <sub>CC</sub>	2.0		V
				±5%V <sub>CC</sub>	2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN; V <sub>IL</sub> = MAX; V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.50	V
				±5%V <sub>CC</sub>		0.42	0.50
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN; I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX; V <sub>I</sub> = 7.0 V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX; V <sub>I</sub> = 2.7 V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX; V <sub>I</sub> = 0.5 V			-1.0	mA	
I <sub>OZH</sub>	Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7 V			50	μA	
I <sub>OZL</sub>	Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5 V			-50	μA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX	-100		-225	mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX		12	18	mA
		I <sub>CCL</sub>			50	70	mA
		I <sub>CCZ</sub>			35	45	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω			T <sub>amb</sub> = 0 °C to +70 °C V <sub>CC</sub> = +5.0 V ± 10% C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay I <sub>an</sub> , I <sub>bn</sub> to $\bar{Y}_n$	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 2.0	7.5 5.0	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to high or low level	Waveform 2 & 3	3.0 4.5	5.0 6.5	7.5 8.5	3.0 4.0	9.0 10.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from high or low level	Waveform 2 & 3	3.0 3.0	5.5 5.0	7.0 7.0	3.0 3.0	7.5 7.5	ns

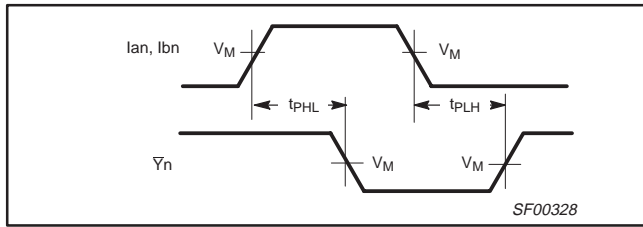
## NOTES:

1. | t<sub>pN</sub> actual – t<sub>pM</sub> actual | for any output compared to any other output where N and M are either LH or HL.

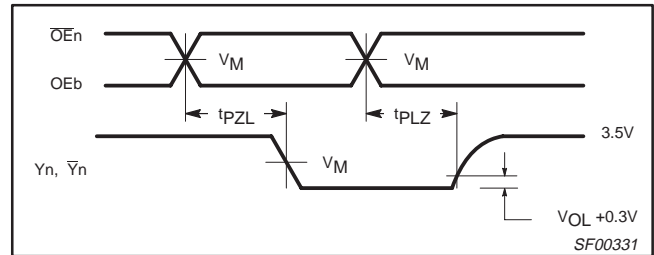
# Octal inverting buffer

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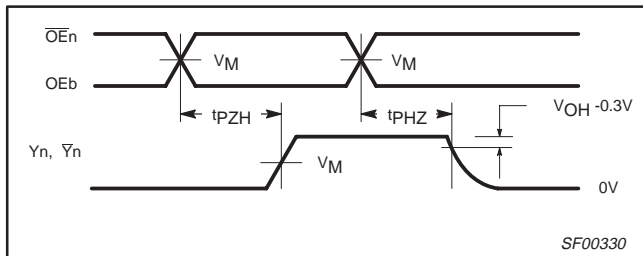
## AC WAVEFORMS



Waveform 1. Propagation delay for inverting outputs



Waveform 3. 3-state output enable time to low level and output disable time from low level



Waveform 2. 3-state output enable time to high level and output disable time from high level

### Notes to AC waveforms

- For all waveforms,  $V_M = 1.5\text{ V}$ .

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Open Collector Outputs**

**Input Pulse Definition**

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS:**

$R_L$  = Load resistor; see AC electrical characteristics for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

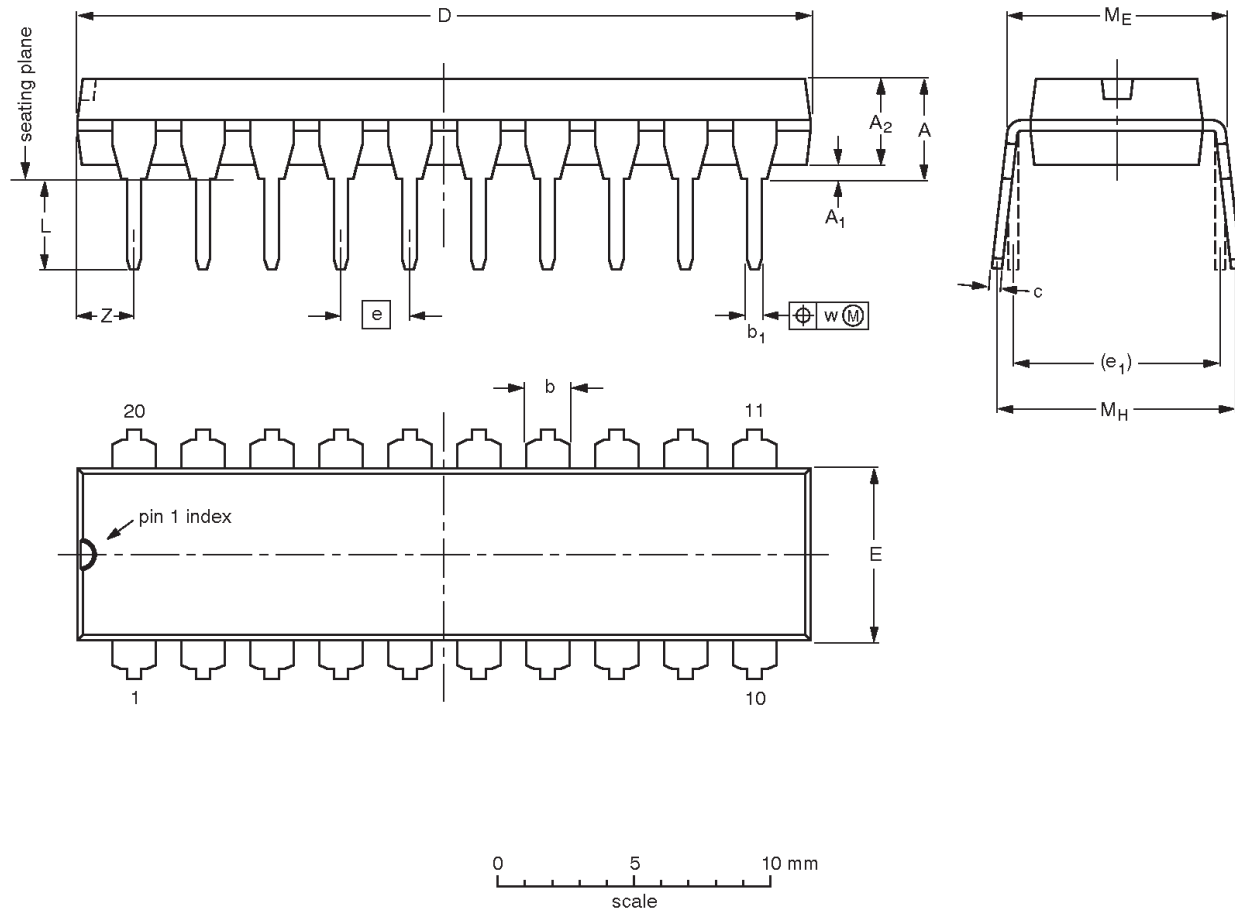
SF00128

# Octal inverting buffer

74F240

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

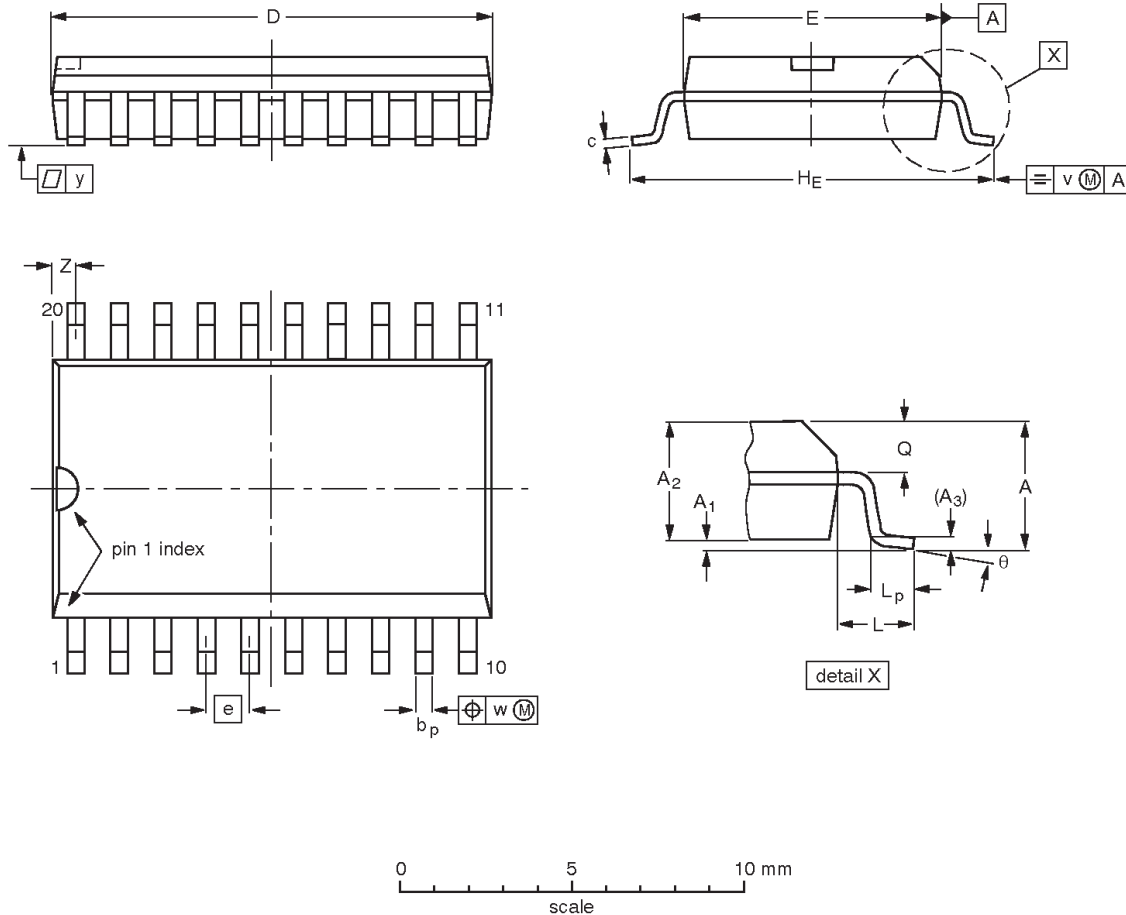
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			99-12-27 03-02-13

# Octal inverting buffer

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				-99-12-27 03-02-19

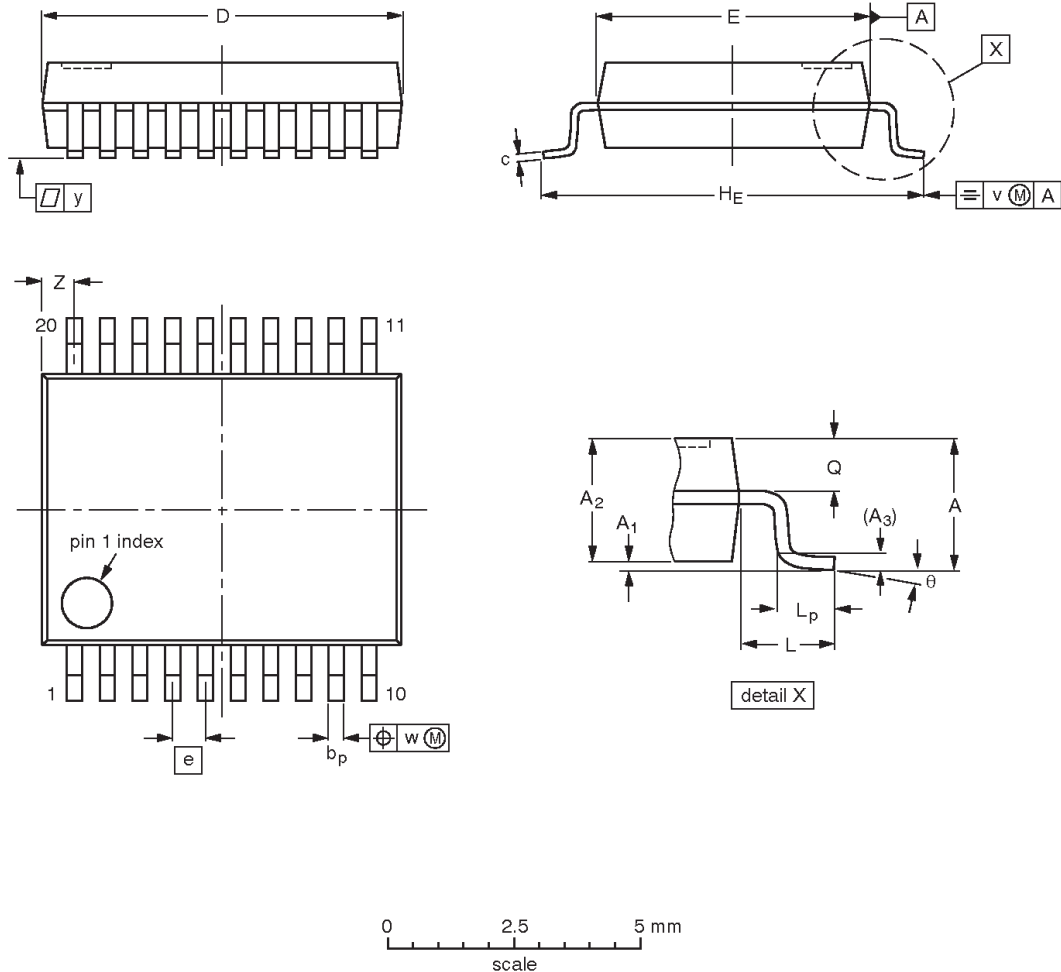


# Octal inverting buffer

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				99-12-27 03-02-19

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**REVISION HISTORY**

Rev	Date	Description
_4	20040225	<b>Product data (9397 750 12941); supersedes data sheet 74F240_241_241A_3 of 2002 Mar 18 (9397 750 09571).</b> Modifications: <ul style="list-style-type: none"><li>• Delete all references to 74F241A (product discontinued).</li><li>• Separate 74F240 and 74F241 into standalone data sheets.</li></ul>
_3	20020318	<b>Product data (9397 750 09571); supersedes previous version.</b>

## Octal inverting buffer

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## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Document order number:

9397 750 12941

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