

## 128 MB to 8 GB 2.5-Inch IDE Flash Drives



## FEATURES

- Capacities from 128MB to 8GB
- Standard IDE Drive Form Factor of 2.5-Inch
- Standard IDE connector and Interface
- Configures to Master or Slave IDE device
- Endurance Guarantee of 2,000,000 Write/Erase Cycles
- Replaces IDE hard drive for applications where tough environments prohibit use of traditional rotating media
- Solid-State (no moving parts)
- High Shock and Vibration Limits
- 512 Byte Sector and ECC Defect Management Compatible to IDE Hard Disk Drives
- No "Spin" Noise Compared to Traditional Rotating Media
- Available in Commercial and Industrial Operating Temperature Ranges
- Standard ECC Engine
- 7 Year Warranty

## GENERAL DESCRIPTION

The SimpleTech SLFLD25-xxxJ(I) are solid-state flash IDE drives with capacities of 128MB to 8GB and in a standard 2.5-inch form factor. The IDE drive consists of an IDE controller and an array of flash memory devices. The IDE drive supports the standard ATA register and command set.

SimpleTech OEM flash drives are the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts to service or maintain, flash drives are reliable alternatives to mechanical hard disk drives for high availability and mission critical applications.

While the inherent ruggedness and reliability of solid state storage relative to rotating hard drives is intuitive, new applications for OEM flash drives are emerging due to the low cost per usable megabyte. Most applications using embedded operating systems such as VxWorks™, Windows XP/embedded™, and Linux™ don't have multi-gigabyte data storage requirements, and therefore a cost savings can be realized when using this robust media.

## ORDERING INFORMATION

## IDE Flash Drives

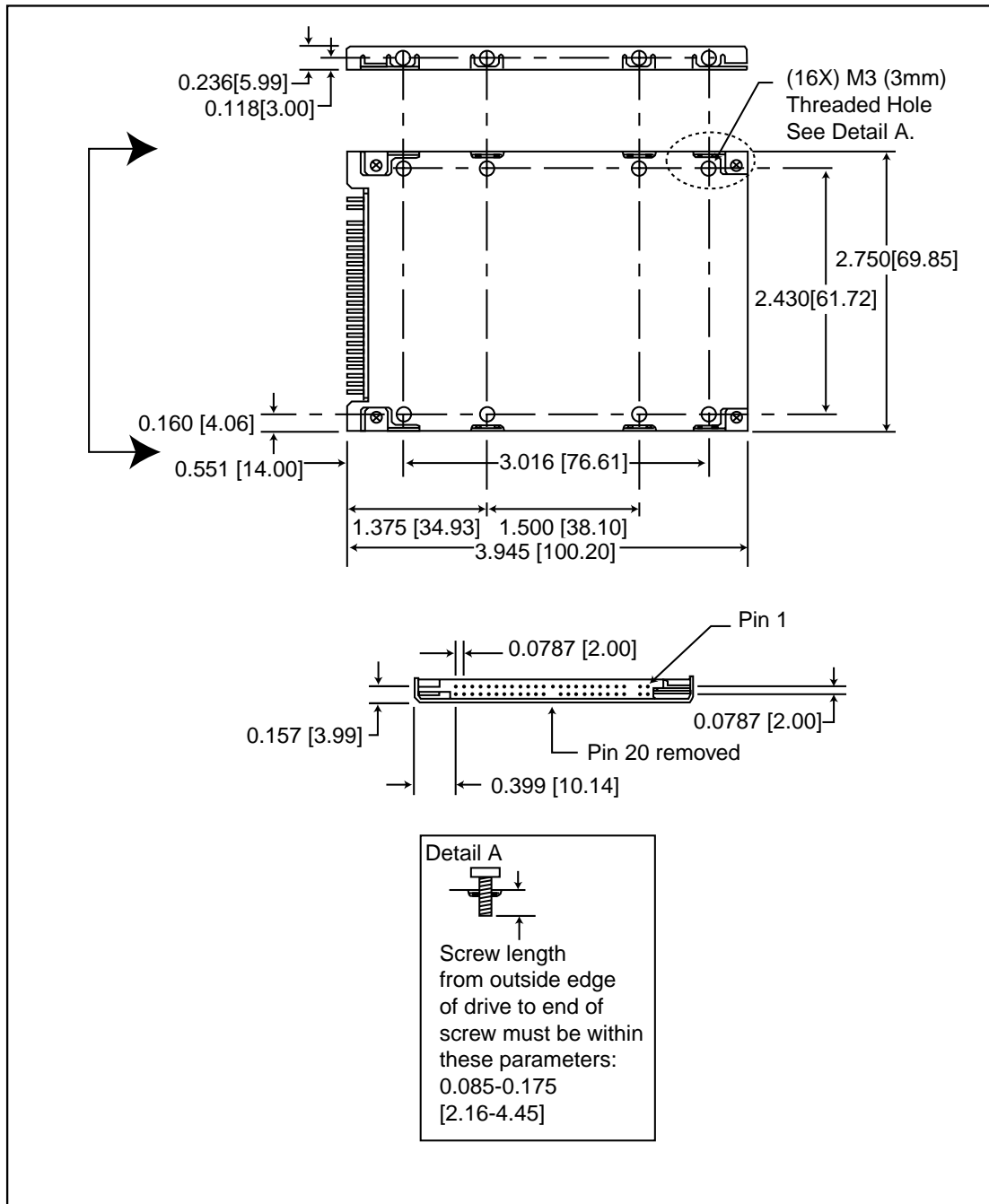
| Part Number*          | Capacity   |
|-----------------------|------------|
| SLFLD25-128J(I) ..... | 128 MBytes |
| SLFLD25-256J(I) ..... | 256 MBytes |
| SLFLD25-512J(I) ..... | 512 MBytes |
| SLFLD25-1GBJ(I) ..... | 1 GBytes   |
| SLFLD25-2GBJ(I) ..... | 2 GBytes   |
| SLFLD25-3GBJ(I) ..... | 3 GBytes   |
| SLFLD25-4GBJ(I) ..... | 4 GBytes   |
| SLFLD25-5GBJ(I) ..... | 5 GBytes   |
| SLFLD25-6GBJ(I) ..... | 6 GBytes   |
| SLFLD25-7GBJ(I) ..... | 7 GBytes   |
| SLFLD25-8GBJ(I) ..... | 8 GBytes   |

\* Custom capacities available.

An "I" suffix added to the part number selects the Industrial Operating Temperature range option. A part number without the "I" suffix selects the Commercial Operating Temperature range option.

**PACKAGE DIMENSIONS**

Refer to the figure below for package dimensions of the 2.5-inch FlashDrive. The units are inches (in parenthesis, millimeters), and the tolerances are  $\pm 0.005$  inches (1.27mm) unless otherwise specified.



**PIN CONFIGURATION**

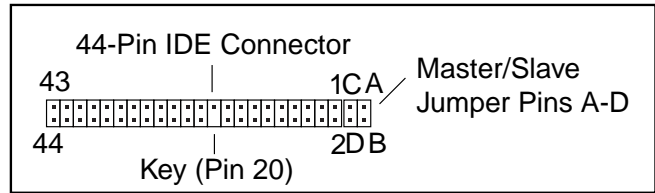
**44-Pin IDE Connector**

**Pin Symbols**

| Pin Num | Pin Symbol | Pin Num | Pin Symbol |
|---------|------------|---------|------------|
| 1       | -RESET     | 23      | -IOWR      |
| 2       | GND        | 24      | GND        |
| 3       | D07        | 25      | -IORD      |
| 4       | D08        | 26      | GND        |
| 5       | D06        | 27      | -IORDY     |
| 6       | D09        | 28      | -CSEL      |
| 7       | D05        | 29      | -DACK      |
| 8       | D10        | 30      | GND        |
| 9       | D04        | 31      | INTRQ      |
| 10      | D11        | 32      | -IOIS16    |
| 11      | D03        | 33      | A1         |
| 12      | D12        | 34      | -PDIAG     |
| 13      | D02        | 35      | A0         |
| 14      | D13        | 36      | A2         |
| 15      | D01        | 37      | -CS1       |
| 16      | D14        | 38      | -CS2       |
| 17      | D00        | 39      | -DASP      |
| 18      | D15        | 40      | GND        |
| 19      | GND        | 41      | VCC        |
| 20      | Key        | 42      | VCC        |
| 21      | DREQ       | 43      | GND        |
| 22      | GND        | 44      | NC         |

"-" indicates signal is active low.

**Pin Locations**



**Jumper Settings**

|   |  |
|---|--|
| <p>43            5 3 1    C A</p> <p>44            6 4 2    D B</p> | <p>If all pins A, B, C, and D are open, the drive is in master mode.</p>                         |
| <p>43            5 3 1    C A</p> <p>44            6 4 2    D B</p> | <p>If pin A is jumpered to pin B, the drive is in slave mode.</p>                                |
| <p>43            5 3 1    C A</p> <p>44            6 4 2    D B</p> | <p>If pin B is jumpered to pin D, the drive mode is determined by the -CSEL signal (Pin 28).</p> |

**NOTE:** In multiple drive configuration, it may become necessary to establish master drive and slave drive. This can be done by booting the PC and using IDE HDD Auto Detection available in CMOS setup.

**Signal Description**

| Signal Name | Dir | Pin   | Description   |
|-------------|-----|---|---|
| -DASP       | I/O | 39  | This input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.   |
| D15-D00     | I/O | 18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 | All Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15.   |
| -IOWR       | I   | 23  | The I/O Write strobe pulse is used to clock I/O data on the drive Data bus into the Drive controller registers when the Drive is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). |
| -IORD       | I   | 25  | This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Drive.   |
| INTRQ       | O   | 31  | Signal is the active high Interrupt Request to the host.  |
| A2-A0       | I   | 35, 33, 36  | A[2:0] are used to select the one of eight registers in the Task File.  |
| -CS1, -CS2  | I   | 37, 38  | -CS1 is the chip select for the task file registers while -CS2 is used to select the Alternate Status Register and the Device Control Register.   |
| -CSEL       | I   | 28  | This internally pulled up signal is used to configure this device as a Master or a Slave. When the pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave   |
| -IOIS16     | O   | 32  | Not used.   |
| -PDIAG      | I/O | 34  | This input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.   |
| -DREQ       | O   | 21  | Not used.   |
| -DACK       | I   | 29  | Not used.   |
| -IORDY      | O   | 27  | Not used, and pulled up to VCC through a 4.7K ohm resistor.   |
| -RESET      | I   | 1   | This input pin is the active low hardware reset from the host.  |
| VCC         | —   | 41, 42  | Power.  |
| GND         | —   | 2, 19, 22, 24, 26, 30, 40, 43                           | Ground.   |
| Key         | —   | 20  | This pin is keyed to ensure cable is connected with the proper orientation.   |

## ABSOLUTE MAXIMUM RATINGS

| Parameter                     | Symbol    | Value           | Unit |
|-------------------------------|-----------|-----------------|------|
| Voltage on any pin w.r.t. Vss | Vin, Vout | -0.5 to VCC+0.5 | V    |
| Storage Temperature range     | Tstg      | -65 to +150     | °C   |

## RECOMMENDED OPERATING CONDITIONS

| Parameter                        | Symbol | Min  | Typ | Max  | Unit |
|----------------------------------|--------|------|-----|------|------|
| Commercial operating temperature | Ta     | 0    | 25  | 70   | °C   |
| Industrial operating temperature | Ta     | -40  | —   | 85   | °C   |
| VCC voltage                      | VCC    | 4.75 | 5.0 | 5.25 | V    |

## PERFORMANCE

| Item                            | Performance           |
|---------------------------------|-----------------------|
| Data Transfer Rate To/From Host | 16.7 MBytes/s (burst) |
| Sustained Read                  | up to 5 MBytes/s      |
| Sustained Write                 | up to 5 MBytes/s      |

## RELIABILITY

| Item                       | Value                            |
|----------------------------|----------------------------------|
| Data Write/Erase Endurance | 2 million cycles min.            |
| Data reliability           | 1 in 10 <sup>14</sup> bits, read |
| Data retention             | 10 years                         |

## ENVIRONMENTAL CHARACTERISTICS

| Item      | Value  |
|-----------|--|
| Shock     | 2K G, half-sine, 0.330 ms to 0.750 ms<br>(per MIL-STD-202G Method 213B, Condition A) |
| Vibration | 30 G 10Hz-2KHz<br>(per MIL-STD-202G Method 204D 20 min/sweep, 12 sweeps/axis)        |
| Humidity  | 85°C 95% RH, 5.5V, 500 hrs   |

## CHS PARAMETERS

| Capacity | C     | H  | S  |
|----------|-------|----|----|
| 128MB    | 980   | 8  | 32 |
| 256MB    | 980   | 16 | 32 |
| 512MB    | 993   | 16 | 63 |
| 1GB      | 1986  | 16 | 63 |
| 2GB      | 3970  | 16 | 63 |
| 3GB      | 6022  | 16 | 63 |
| 4GB      | 7964  | 16 | 63 |
| 5GB      | 10038 | 16 | 63 |
| 6GB      | 12046 | 16 | 63 |
| 7GB      | 14054 | 16 | 63 |
| 8GB      | 16062 | 16 | 63 |

C=cylinders; H=heads; S=sectors/track

**DC CHARACTERISTICS** (Ta=0 to 70°C for commercial temperature parts, -40 to 85°C for industrial temperature parts; VCC=5V±5%)

| Symbol | Parameter  | Min  | Max     | Units | Notes  |
|--------|--|------|---------|-------|--------|
| VIL    | Input LOW Voltage                                      | -0.3 | +0.8    | V     |        |
| VIH    | Input HIGH Voltage                                     | 2.0  | VCC+0.3 | V     |        |
| VOL    | Output LOW Voltage                                     |      | 0.8     | V     | at 4mA |
| VOH    | Output HIGH Voltage                                    | 4.0  |         | V     | at 1mA |
| ICC    | Operating Current, VCC=5.0V<br>Sleep mode<br>Operating |      | 1200    | uA    |        |
|        |  |      | 30      | mA    |        |
| ILI    | Input Leakage Current                                  |      | 10      | μA    |        |
| ILO    | Output Leakage Current                                 |      | 2       | μA    |        |
| CI/O   | Input/output Capacitance                               |      | 25      | pF    |        |

**AC CHARACTERISTICS** (Ta=0 to 70°C for commercial temperature parts, -40 to 85°C for industrial temperature parts; VCC=5V±5%)

### Register Access AC Characteristics for True IDE

| Parameter                              | Symbol          | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Unit |
|--|-----------------|-------|-------|-------|-------|-------|------|
| Cycle time (min)                       | t <sub>0</sub>  | 600   | 383   | 330   | 180   | 120   | ns   |
| Address valid to -IORD/-IOWR setup     | t <sub>1</sub>  | 70    | 50    | 30    | 30    | 25    | ns   |
| -IORD/-IOWR pulse width 8bit (min)     | t <sub>2</sub>  | 290   | 290   | 290   | 80    | 70    | ns   |
| -IORD/-IOWR recovery time (min)        | t <sub>2i</sub> | —     | —     | —     | 70    | 25    | ns   |
| -IOWR data setup (min)                 | t <sub>3</sub>  | 60    | 45    | 30    | 30    | 20    | ns   |
| -IOWR data hold (min)                  | t <sub>4</sub>  | 30    | 20    | 15    | 10    | 10    | ns   |
| -IORD data setup (min)                 | t <sub>5</sub>  | 50    | 35    | 20    | 20    | 20    | ns   |
| -IORD data hold (min)                  | t <sub>6</sub>  | 5     | 5     | 5     | 5     | 5     | ns   |
| -IORD data tristate (max)              | t <sub>6z</sub> | 30    | 30    | 30    | 30    | 30    | ns   |
| Address valid to -IOCS16 assert. (max) | t <sub>7</sub>  | 90    | 50    | 40    | n/a   | n/a   | ns   |
| Address valid to -IOCS16 release (max) | t <sub>8</sub>  | 60    | 45    | 30    | n/a   | n/a   | ns   |
| -IORD/-IOWR to address valid hold      | t <sub>9</sub>  | 20    | 15    | 10    | 10    | 10    | ns   |

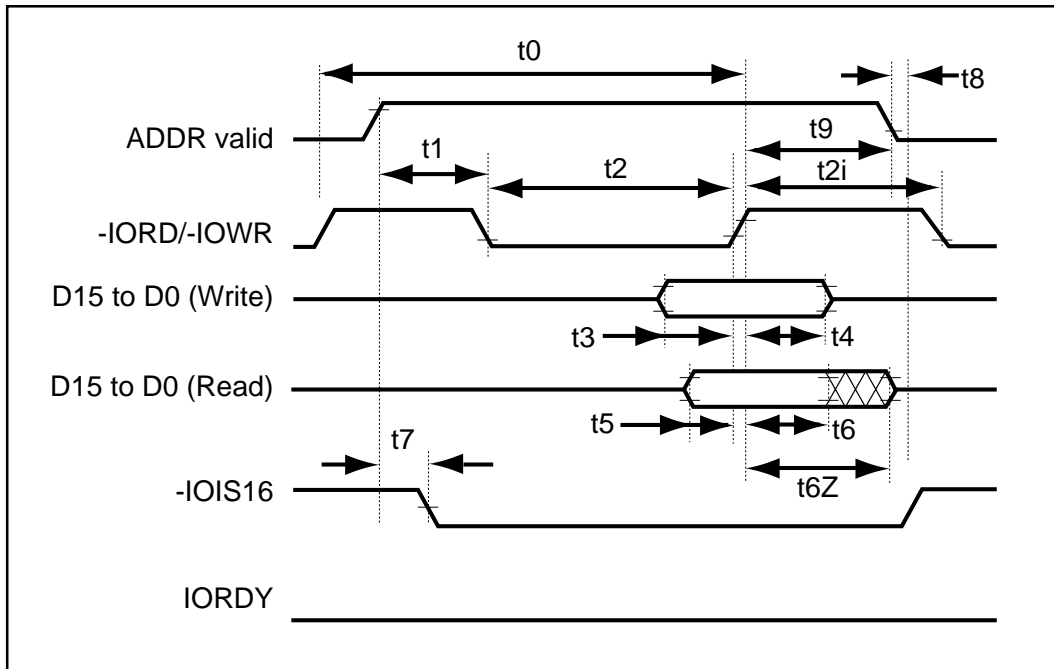
### PIO Mode Access AC Characteristics for True IDE

| Parameter                              | Symbol          | Mode0 | Mode1 | Mode2 | Mode3 | Mode4 | Unit |
|--|-----------------|-------|-------|-------|-------|-------|------|
| Cycle time (min)                       | t <sub>0</sub>  | 600   | 383   | 240   | 180   | 120   | ns   |
| Address valid to -IORD/-IOWR setup     | t <sub>1</sub>  | 70    | 50    | 30    | 30    | 25    | ns   |
| -IORD/-IOWR pulse width 16bit (min)    | t <sub>2</sub>  | 165   | 125   | 100   | 80    | 70    | ns   |
| -IORD/-IOWR recovery time (min)        | t <sub>2i</sub> | -     | -     | -     | 70    | 25    | ns   |
| -IOWR data setup (min)                 | t <sub>3</sub>  | 60    | 45    | 30    | 30    | 20    | ns   |
| IOWR data hold (min)                   | t <sub>4</sub>  | 30    | 20    | 15    | 10    | 10    | ns   |
| -IORD data setup (min)                 | t <sub>5</sub>  | 50    | 35    | 20    | 20    | 20    | ns   |
| -IORD data hold (min)                  | t <sub>6</sub>  | 5     | 5     | 5     | 5     | 5     | ns   |
| -IORD data tristate (max)              | t <sub>6z</sub> | 30    | 30    | 30    | 30    | 30    | ns   |
| Address valid to -IOCS16 assert. (max) | t <sub>7</sub>  | 90    | 50    | 40    | n/a   | n/a   | ns   |
| Address valid to -IOCS16 release (max) | t <sub>8</sub>  | 60    | 45    | 30    | n/a   | n/a   | ns   |
| -IORD/-IOWR to address valid hold      | t <sub>9</sub>  | 20    | 15    | 10    | 10    | 10    | ns   |

(continued)

AC CHARACTERISTICS *(continued)*

True IDE Mode Access Read/Write Timings





**TRUE IDE MODE**

The drive is configured in a True IDE mode at power up. The data register is accessed in word (16-bit) mode at power up. The drive permits 8-bit accesses if the host issues a Set Feature Command to put the device in 8-bit mode.

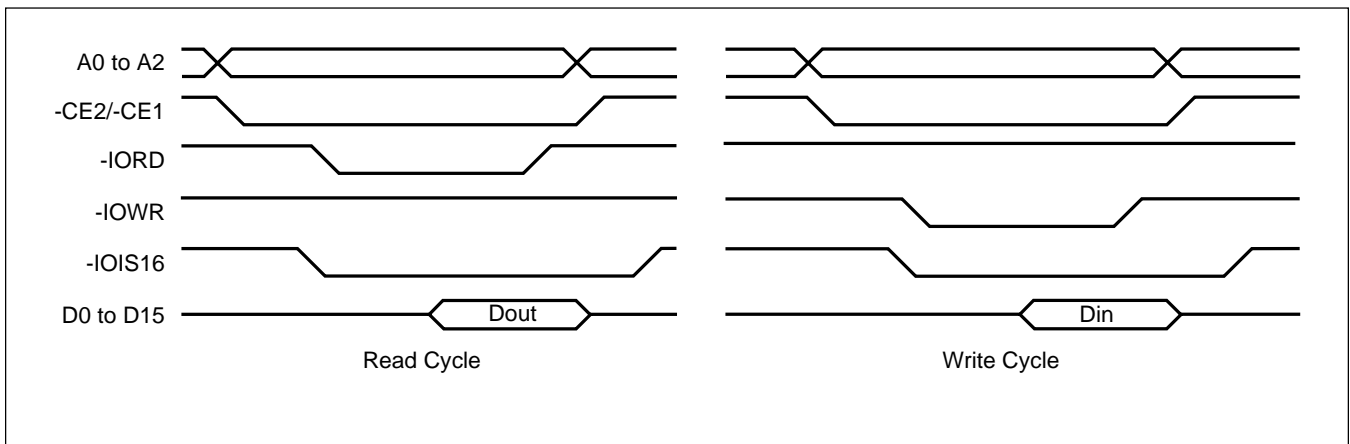
**True IDE Mode Read I/O Function**

| Mode                    | -CE2 | -CE1 | A0 to A2 | -IOR $\bar{D}$ | -IOW $\bar{R}$ | D15-D8   | D7-D0      |
|-------------------------|------|------|----------|----------------|----------------|----------|------------|
| Invalid Mode            | L    | L    | x        | x              | x              | High Z   | High Z     |
| Standby Mode            | H    | H    | x        | x              | x              | High Z   | High Z     |
| Data Register Access    | H    | L    | 0        | L              | H              | Odd-Byte | Even-Byte  |
| Alternate Status Access | L    | H    | 6h       | L              | H              | High Z   | Status Out |
| Other Task File Access  | H    | L    | 1-7h     | L              | H              | High Z   | Data       |
| x: L or H               |      |      |          |                |                |          |            |

**True IDE Mode Write I/O Function**

| Mode                    | -CE2 | -CE1 | A0 to A2 | -IOR $\bar{D}$ | -IOW $\bar{R}$ | D15-D8     | D7-D0      |
|-------------------------|------|------|----------|----------------|----------------|------------|------------|
| Invalid Mode            | L    | L    | x        | x              | x              | Don't Care | Don't Care |
| Standby Mode            | H    | H    | x        | x              | x              | Don't Care | Don't Care |
| Data Register Access    | H    | L    | 0        | H              | L              | Odd-Byte   | Even-Byte  |
| Control Register Access | L    | H    | 6h       | H              | L              | Don't Care | Control In |
| Other Task File Access  | H    | L    | 1-7h     | H              | L              | Don't Care | Data       |
| x: L or H               |      |      |          |                |                |            |            |

**True IDE Mode I/O Access Timing Example**



## TASK FILE REGISTER SPECIFICATION

These registers are used for reading and writing data to the drive.

### True IDE Mode I/O Map

| -CE2 | -CE1 | A2 | A1 | A0 | -IORD=0                | -IOWR=0                 |
|------|------|----|----|----|------------------------|-------------------------|
| 1    | 0    | 0  | 0  | 0  | Data register          | Data register           |
| 1    | 0    | 0  | 0  | 1  | Error register         | Feature register        |
| 1    | 0    | 0  | 1  | 0  | Sector Count register  | Sector Count register   |
| 1    | 0    | 0  | 1  | 1  | Sector No. register    | Sector No. register     |
| 1    | 0    | 1  | 0  | 0  | Cylinder Low register  | Cylinder Low register   |
| 1    | 0    | 1  | 0  | 1  | Cylinder High register | Cylinder High register  |
| 1    | 0    | 1  | 1  | 0  | Drive Head register    | Drive Head register     |
| 1    | 0    | 1  | 1  | 1  | Status register        | Command register        |
| 0    | 1    | 1  | 1  | 0  | Alt Status register    | Device Control register |
| 0    | 1    | 1  | 1  | 1  | Drive Address register | Reserved                |

**Data Register**

The Data Register is a 16 bit read/write register used for transferring data between the drive and the host. This register can be accessed in word mode and byte mode.

|           |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|-----------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| bit15     | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| D0 to D15 |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |

**Error Register**

This read only register is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to "0" (Ready).

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| BBK  | UNC  | 0    | IDNF | 0    | ABRT | 0    | AMNF |

| bit | Name                          | Function   |
|-----|-------------------------------|--|
| 7   | BBK (Bad Block Detected)      | This bit is set when a Bad Block is detected in requested ID field—not supported |
| 6   | UNC (Data ECC Error)          | This bit is set when an Uncorrectable error has occurred when reading the drive. |
| 4   | IDNF (ID Not Found)           | The requested sector ID is in error or cannot be found.                          |
| 2   | ABRT (ABoRTed Command)        | Drive status error or Aborted invalid command                                    |
| 0   | AMNF (Address Mark Not Found) | This bit is set in case of a general error.                                      |

| Diagnostic Code | Description               |
|-----------------|---------------------------|
| 01h             | No error detected         |
| 02h             | Formatting error          |
| 03h             | Sector buffer error       |
| 04h             | ECC error                 |
| 05h             | Microprocessor error      |
| 8xh             | Drive 1 failed (not used) |

**Feature Register**

This write only register provides information regarding the features of the drive which the host wishes to utilize. See details under the SET FEATURE command.

|              |      |      |      |      |      |      |      |
|--------------|------|------|------|------|------|------|------|
| bit7         | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Feature Byte |      |      |      |      |      |      |      |

**Sector Count Register**

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the drive. If the value in the register is 0, a count of 256 sectors is indicated.

|                   |      |      |      |      |      |      |      |
|-------------------|------|------|------|------|------|------|------|
| bit7              | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Sector Count Byte |      |      |      |      |      |      |      |

**Sector Number Register**

When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.

|   |      |      |      |      |      |      |      |
|---|------|------|------|------|------|------|------|
| bit7                                      | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Sector Number Byte or bits 7:0 of the LBA |      |      |      |      |      |      |      |

**Cylinder Low Register**

In CHS mode (LBA=0), this register contains the low order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.

|   |      |      |      |      |      |      |      |
|---|------|------|------|------|------|------|------|
| bit7                                      | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Cylinder Low Byte or bits 15:8 of the LBA |      |      |      |      |      |      |      |

**Cylinder High Register**

In CHS mode (LBA=0), this register contains the high order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.

|   |      |      |      |      |      |      |      |
|---|------|------|------|------|------|------|------|
| bit7  | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| Cylinder High Byte or bits 23:16 of the LBA |      |      |      |      |      |      |      |

**Drive/Head Register**

This register select the device address translation (CHS or LBA) and provides head address (CHS) or high order address bits 27:24 for LBA.

|      |      |      |      |                            |      |      |      |
|------|------|------|------|----------------------------|------|------|------|
| bit7 | bit6 | bit5 | bit4 | bit3                       | bit2 | bit1 | bit0 |
| 1    | LBA  | 1    | DRV  | Head No. or LBA bits 27:24 |      |      |      |

| bit | Name                  | Function  |
|-----|-----------------------|---|
| 7   | 1                     | This bit is set to "1".   |
| 6   | LBA                   | LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected. When LBA=1, LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows:<br>LBA07-LBA00: Sector Number Register D7-D0<br>LBA15-LBA08: Cylinder Low Register D7-D0<br>LBA23-LBA16: Cylinder High Register D7-D0<br>LBA27-LBA24: Drive/Head Register bits HS3-HS0 |
| 5   | 1                     | This bit is set to "1".   |
| 4   | DRV (DRiVe select)    | This bit is used for selecting the Master (drive 0) and Slave (drive 1) in Master/Slave organization. The drive is set to be drive 0 or 1 by using DRV# of the Socket and Copy register.  |
| 3-0 | Head Number (HS3-HS0) | These bits are used for selecting the Head number. Bit 3 is MSB. In LBA mode, these bits represent the LBA address 27:24.   |

### Status Register

This read only register indicates status of a command execution. When the BSY bit is “0”, the other bits are valid; when the BSY bit is “1”, the other bits are not valid. When the register is read, the interrupt (-IREQ pin) is cleared.

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| BSY  | DRDY | DWF  | DSC  | DRQ  | CORR | IDX  | ERR  |

| bit | Name                      | Function  |
|-----|---------------------------|---|
| 7   | BSY (BuSY)                | This bit is set when the drive internal operation is executing. When this bit is set to “1”, other bits in this register are invalid.   |
| 6   | DRDY (Drive ReaDY)        | If this bit and DSC bit are set to “1”, the drive is capable of receiving the read and write or seek requests. If this bit is set to “0”, the drive prohibits these requests. On error, DRDY changes only after the host reads the Status Register. |
| 5   | DWF (Drive Write Fault)   | This bit is set if a fault occurs during the write process.   |
| 4   | DSC (Drive Seek Complete) | This bit is set when the requested sector was found.  |
| 3   | DRQ (Data ReQuest)        | This bit is set when information can be transferred between the host and data register.   |
| 2   | CORR (CORReCted data)     | This bit is set when a correctable data error has occurred and the data has been corrected.   |
| 1   | IDX (InDeX)               | This bit is always set to “0”.  |
| 0   | ERR (ERRor)               | This bit is set when the previous command has ended in some type of error. The error information is set in the Error register.  |

### Alternate Status Register

This register is the same as the Status register except that -IREQ is not negated when data is read.

### Command Register

This write only register is used for writing the command that executes the drive’s operation. The command code is written in the command register after its parameters are written in the Task File during the drive ready state. See details under the ATA COMMAND SPECIFICATIONS.

**Device Control Register**

This write only register is used for controlling the interrupt request and issuing an ATA soft reset to the drive.

| bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|------|------|------|------|------|------|------|------|
| x    | x    | x    | x    | 1    | SRST | nIEN | 0    |

| bit | Name                    | Function   |
|-----|-------------------------|--|
| 7-4 | x                       | Don't care.  |
| 3   | 1                       | This bit is set to "1".  |
| 2   | SRST (Software ReSeT)   | This bit is set to "1" in order to force the drive to perform an AT disk control soft reset operation.   |
| 1   | nIEN (Interrupt ENable) | When set to "0", it enables interrupts to the host (using the -IREQ tri-state pin). When inactive (set to "1") or drive is not selected, it disables all pending interrupts (-IREQ in high-Z). This bit is ignored in memory mode. |
| 0   | 0                       | This bit is set to "0".  |

**Drive Address Register**

This read only register is used for confirming the drive's status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host's I/O space because of potential conflicts on bit 7.

| bit7   | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|--------|------|------|------|------|------|------|------|
| High-Z | nWTG | nHS3 | nHS2 | nHS1 | nHS0 | nDS1 | nDS0 |

| bit | Name                     | Function  |
|-----|--------------------------|---|
| 7   | x                        | This bit is unused.   |
| 6   | nWTG (WriTing Gate)      | This bit is unused.   |
| 5-2 | nHS3-0 (Head Select 3-0) | These bits are the negative value of the Head Select bits (bit 3 to 0) in the Drive/Head register |
| 1   | nDS1 (Drive Select 1)    | When set to "0", drive 1 is active and selected.  |
| 0   | nDS0 (Drive Select 0)    | When set to "0", drive 0 is active and selected.  |

## ATA COMMAND SPECIFICATIONS

This table with the following paragraphs summarizes the ATA command set.

| No. | Command set                 | Code        | FR | SC | SN | CY | DR  | HD | LBA |
|-----|-----------------------------|-------------|----|----|----|----|-----|----|-----|
| 1   | Check Power Mode            | E5h or 98h  | —  | Y  | —  | —  | Y   | —  | —   |
| 2   | Execute Drive Diagnostic    | 90h         | —  | —  | —  | —  | Y** | —  | —   |
| 3   | Erase Sector(s)             | C0h         | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 4   | Format Track                | 50h         | —  | Y  | —  | Y  | Y   | Y  | Y   |
| 5   | Identify Drive              | ECh         | Y  | —  | —  | —  | Y   | —  | —   |
| 6   | Idle                        | E3h or 97h  | —  | Y  | —  | —  | Y   | —  | —   |
| 7   | Idle Immediate              | E1h or 95h  | —  | —  | —  | —  | Y   | —  | —   |
| 8   | Initialize Drive Parameters | 91h         | —  | Y  | —  | —  | Y   | Y  | —   |
| 9   | Read Buffer                 | E4h         | —  | —  | —  | —  | Y   | —  | —   |
| 10  | Read Multiple               | C4h         | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 11  | Read Long Sector            | 22h or 23h* | —  | —  | Y  | Y  | Y   | Y  | Y   |
| 12  | Read Sector(s)              | 20h or 21h* | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 13  | Read Verify Sector(s)       | 40h or 41h* | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 14  | Recalibrate                 | 1Xh         | —  | —  | —  | —  | Y   | —  | —   |
| 15  | Request Sense               | 03h         | —  | —  | —  | —  | Y   | —  | —   |
| 16  | Seek                        | 7Xh         | —  | —  | Y  | Y  | Y   | Y  | Y   |
| 17  | Set Features                | EFh         | —  | Y  | Y  | Y  | Y   | Y  | —   |
| 18  | Set Multiple Mode           | C6h         | —  | Y  | —  | —  | Y   | —  | —   |
| 19  | Set Sleep Mode              | E6h or 99h  | —  | —  | —  | —  | Y   | —  | —   |
| 20  | Stand By                    | E2h or 96h  | —  | Y  | —  | —  | Y   | —  | —   |
| 21  | Stand By Immediate          | E0h or 94h  | —  | —  | —  | —  | Y   | —  | —   |
| 22  | Translate Sector            | 87h         | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 23  | Wear Level                  | F5h         | —  | —  | —  | —  | Y   | Y  | —   |
| 24  | Write Buffer                | E8h         | —  | —  | —  | —  | Y   | —  | —   |
| 25  | Write Long Sector           | 32h or 33h* | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 26  | Write Multiple              | C5h         | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 27  | Write Multiple w/o Erase    | CDh         | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 28  | Write Sector(s)             | 30h or 31h* | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 29  | Write Sector(s) w/o Erase   | 38h         | —  | Y  | Y  | Y  | Y   | Y  | Y   |
| 30  | Write Verify                | 3Ch         | —  | Y  | Y  | Y  | Y   | Y  | Y   |

FR=Features Register, Register, HD=Head no. (0 to 3) of Drive/Head Register, \* First command code=with retry, Second command code=without retry.  
 SC=Sector Count Register (00h to FFh), SN=Sector Number Register (01h to 20h), CY=Cylinder Registers, DR=Drive bit of Drive/Head Register, HD=Head no. (0 to 3) of Drive/Head Register, LBA=Logical Block Address Mode Supported.  
 Y—Set up. \*\* Address to drive 0. Both drives execute command  
 “—” —Not set up.



### Check Power Mode (code: E5h or 98h)

This command checks the power mode.

### Execute Drive Diagnostic (code: 90h)

This command performs the internal diagnostic tests implemented by the drive. See ERROR register for diagnostic codes.

### Erase Sector(s) (code: C0h)

This command is used to pre-erase and condition data sectors in advance.

### Format Track (code: 50h)

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically 00h or FFh). This drive accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.

### Identify Drive (code: ECh)

This command enables the host to receive parameter information from the drive. (See table below.)

Identify Drive Information (Typical)

| Word Address | Data  | Total Bytes | Description   |
|--------------|-------|-------------|---|
| 0            | 044AH | 2           | General configuration bit-significant information—value fixed by CFA                |
| 1            | XXXXH | 2           | Default number of cylinders   |
| 2            | 0000H | 2           | Reserved  |
| 3            | 00XXH | 2           | Default number of heads   |
| 4            | XXXXH | 2           | Do not use this word. Before retirement, was number of unformatted bytes per track  |
| 5            | XXXXH | 2           | Do not use this word. Before retirement, was number of unformatted bytes per sector |
| 6            | XXXXH | 2           | Default number of sectors per track   |
| 7-8          | XXXXH | 4           | Number of sectors per card (word7=MSW, word 8 = LSW)                                |
| 9            | 0000H | 2           | Reserved  |
| 10-19        | XXXXH | 20          | Serial Number (see table next page for definition)                                  |
| 20           | XXXXH | 2           | Do not use this word. Before retirement, was buffer type                            |
| 21           | XXXXH | 2           | Do not use this word. Before retirement, was buffer size in 512 byte increments     |
| 22           | 0004H | 2           | # of ECC bytes passed on Read/Write Long commands                                   |
| 23-46        | XXXXH | 48          | Firmware revision and model number in ASCII (see table next page for definition)    |
| 47           | 0001H | 2           | Maximum of 1 sector on Read/Write Multiple command                                  |
| 48           | 0000H | 2           | Double Word not supported   |
| 49           | 0200H | 2           | DMA not supported, LBA supported  |
| 50           | 0000H | 2           | Reserved  |
| 51           | 0200H | 2           | PIO data transfer cycle timing mode   |
| 52           | 0000H | 2           | Single word DMA data transfer cycle timing mode (not supported)                     |
| 53           | 0003h | 2           | Words 54 - 58 and 64 - 70 are valid   |
| 54           | XXXXH | 2           | Number of Current Cylinders   |
| 55           | XXXXH | 2           | Number of Current Heads   |
| 56           | XXXXH | 2           | Number of Current Sectors Per Track   |
| 57           | XXXXH | 2           | LSW of the Current Capacity in Sectors  |
| 58           | XXXXH | 2           | MSW of the Current Capacity in Sectors  |
| 59           | 010XH | 2           | Current Setting for Block Count=1 for R/W Multiple commands                         |
| 60-61        | XXXXH | 4           | Total number of sectors addressable in LBA Mode                                     |
| 62           | 0000H | 2           | Single word DMA transfer not supported  |
| 63           | 0000H | 2           | Multiword DMA modes not supported   |
| 64           | 0003H | 2           | Advanced PIO modes supported (modes 3 and 4)  |
| 65           | 0000H | 2           | Minimum multiword DMA transfer cycle time per word (ns)                             |
| 66           | 0000H | 2           | Recommended multiword DMA transfer cycle time per word (ns)                         |
| 67           | 0078H | 2           | Minimum PIO transfer without flow control   |
| 68           | 0078H | 2           | Minimum PIO transfer with IORDY flow control  |
| 69-255       | 0000H | 388         | Reserved  |

XXXXH: These values are dependent upon the the specific card.

**Identify Drive Information (continued)**  
(Serial Number, Firmware Revision, and Model Number)

|   |           |            |           |           |           |
|---|-----------|------------|-----------|-----------|-----------|
| Serial Number Format (typical): Words 10-19 |           |            |           |           |           |
| SimpleTech Proprietary                      | Yr        | Day        | Hr        | Min       | Sec       |
| <i>STI_J13C0</i>                            | <i>04</i> | <i>224</i> | <i>09</i> | <i>27</i> | <i>50</i> |
| Firmware Revision: Words 23-26              |           |            |           |           |           |
| <i>mm/dd/yy</i>                             |           |            |           |           |           |
| Model Number: Words 27-46                   |           |            |           |           |           |
| <i>STI Flash X.Y.Z</i>                      |           |            |           |           |           |

**Idle**  
(code: E3h or 97h)

This command causes the drive to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

**Idle Immediate**  
(code: E1h or 95h)

This command causes the drive to set BSY, enter the Idle (Read) mode, clear BSY, and generate an interrupt.

**Initialize Drive Parameters**  
(code: 91h)

This command enables the host to set the number of sectors per track and the number of heads per cylinder.

**Read Buffer**  
(code: E4h)

This command enables the host to read the current contents of the drive's sector buffer.

**Read Multiple**  
(code: C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

**Read Long Sector**  
(code: 22h or 23h)

This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

**Read Sector(s)**  
(code: 20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

**Read Verify Sector(s)**  
(code: 40h or 41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. This

**Recalibrate**  
(code: 1Xh)

The CompactFlash performs only the interface timing and register operations. When this command is issued, the CompactFlash sets BSY and waits for an appropriate length of time after which it clears BSY and issues an interrupt. When this command ends normally, the CompactFlash is initialized

**Request Sense**  
(code: 03h)

This command requests an extended error code after a command ends with an error. Refer to table below.

| Code                    | Description  |
|-------------------------|--|
| 00H                     | No error detected                                  |
| 01H                     | Self test OK (No error)                            |
| 09H                     | Miscellaneous Error - N/A                          |
| 20H                     | Invalid Command                                    |
| 21H                     | Invalid Address (requested Head or Sector invalid) |
| 2FH                     | Address Overflow (address too large)               |
| 35H, 36H                | Supply or generate Voltage Out of Tolerance        |
| 11H                     | Uncorrectable ECC Error                            |
| 18H                     | Correctable ECC Error - N/A                        |
| 05H, 30H-34H, 37H, 3EH  | Self Test Diagnostic Failed                        |
| 10H, 14H                | ID Not Found - N/A                                 |
| 3AH                     | Spare Sectors Exhausted                            |
| 1FH                     | Data Transfer Error / Aborted Command              |
| 0CH, 38H, 3BH, 3CH, 3FH | Corrupted Media Format - N/A                       |
| 03H                     | Write / Erase Failed - N/A                         |
| 22H                     | Power Level 1 Disabled                             |

### Seek (code: 7Xh)

This command is effectively a NOP command to the drive although it does perform a range check.

### Set Features (code: EFh)

This command is used by the host to establish or select certain features.

| Feature | Description  |
|---------|--|
| 01H     | Enable 8-bit data transfers  |
| 55H     | Disable Read Look Ahead  |
| 66H     | Disable Power on Reset (POR) establishment of defaults at Soft Reset |
| 81H     | Disable 8-bit data transfers   |
| BBH     | 4bytes of data apply on Read/Write Long commands                     |
| CCH     | Enable Power on Reset (POR) establishment of default at Soft Reset   |

### Set Multiple Mode (code: C6h)

This command enables the drive to perform Read and Write Multiple operations and establishes the block count for these commands.

### Set Sleep Mode (code: E6h or 99h)

This is the only command that allows the host to set the CompactFlash into Sleep mode. When the drive is set to sleep mode, the CompactFlash clears the BSY line and issues an interrupt. The drive enters sleep mode and the only method to make the drive active again (back to normal operation) is by performing a hardware reset or a software reset.

### Stand By (code: E2h or 96h)

This command sets the drive in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the drive returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.

### Stand By Immediate (code: E0h or 94h)

This command causes the drive to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

### Translate Sector (code: 87h)

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.

### Wear Level (code: F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.

### Write Buffer (code: E8h)

This command enables the host to overwrite the contents of the drive's sector buffer with any data pattern desired.

### Write Long Sector (code: 32h or 33h)

This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

### Write Multiple (code: C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

### Write Multiple without Erase (code: CDh)

This command is similar to the Write Multiple command with the exception that an implied erase before the write operation is not performed. Note that before using this command, it is required to erase the respective sectors using the Erase Sectors command.

**Write Sector(s)  
(code: 30h or 31h)**

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

**Write Sector(s) without Erase  
(code: 38h)**

This command is similar to the Write Sector(s) command with the exception that an implied erase before the write operation is not performed. Note that before using this command, it is required to erase the respective sectors using the Erase Sectors command.

**Write Verify  
(code: 3Ch)**

This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

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## REVISION HISTORY

### Rev. Change Description from Previous Revision

- 101 2/1/04. Initial Release.
- 102 5/26/04. IOL/IOH condition at 5.0V is removed. General Description updated with new marketing copy. 64MB removed. R/W speeds changed from 5.4/4.5MB/s to 5/5MB/s. CHS Parameter table added. VCC 5V tolerance changed to 5% from 10%. Disclaimer notice added.
- 103 7/2/04. Pin Description changes: -IOIS16 not used in IDE mode; -IORDY description corrected to not used by card and pulled up by 4.7K ohm resistor. Performance rates for read and write described as sustained read and sustained write. Error register bit 0 Function "not supported" phrase removed. DMA commands removed (paper only error indicated that DMA was supported). Identify Drive Information table updated to reflect DMA not supported. DC Characterists Sleep Mode value changed from 120uA to 1200uA for 5V power supply.
- 104 7/9/04. Endurance increased from 300,000 cycles min to 2 million cycles min.
- 105 7/22/04. "up to" added to sustained read and write data rate performance.
- 106 8/23/04. Environmental Characteristics updated to testing parameters. Definition for Serial #, Firmware Rev., and Model # in the Identify Drive Information table added in callout. Words 4-5, 20-21, 49, and 63 of Drive ID table corrected.
- 107 10/14/04. Standard ECC, Endurance, and Warranty bullets added to Features on page 1.
- 108 2/14/05. Shock parameter changed to 0.330ms to 0.750ms from 11ms. 3/14/05. Humidity parameter updated to 95% from 85%. CHS values updated.

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