GLS85LD1001T / GLS85LD512
Industrial Grade PATA NANDrive™

Data Sheet 06.000
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Features

- **Industry Standard ATA / IDE Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6 [1)]
  - Supports up to Multi-Word DMA Mode-4 [2)]
  - Supports up to Ultra DMA Mode-4
- **Performance**
  - Sustained sequential data read - Up to 30 MByte/sec*
  - Sustained sequential data write - Up to 10 MByte/sec*
    * measured using 128 KByte block size
- **Power Management**
  - 3.3V Power Supply
  - 5.0V or 3.3V Host Interface Through VDDQ pins
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Power Specification**
  - Active mode
    85mA typical (GLS85LD0512)
    100mA typical (GLS85LD1001T)
  - Sleep mode
    160µA typical (GLS85LD0512)
    170µA typical (GLS85LD1001T)
- **Expanded Data Protection**
  - WP#/PD# pin configurable by firmware for prevention of data overwrites
- **Integrated Voltage Detector**
  - Detects supply voltage fluctuations and generates reset during power-up and power-down to prevent inadvertent writes
- **20-Byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-Byte Unique ID
  - User-Programmable 10-Byte ID
- **Integrated Voltage Detector**
  - Prevents inadvertent Write operations due to unexpected power-down or brownout.
- **Pre-programmed Embedded Firmware**
  - Executes industry standard ATA/IDE commands
  - Implements dynamic wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Robust Built-in ECC**
- **Industrial Temperature Range**
  - -40°C to 85°C for industrial operation
- **Package**
  - 12mm x 24mm x 1.40mm (maximum height), 91-ball, 1.0mm ball pitch, LBGA (LBTE)
- **All Devices are RoHS Compliant**

Product Description

The GLS85LD0512 and GLS85LD1001T Industrial Grade PATA NANDrive™ devices (referred to as "PATA NANDrive" in this datasheet) are high-performance, fully-integrated, embedded flash solid-state drives. They combine an integrated ATA Controller and 512 MByte or 1 GByte of NAND flash memory in a multi-chip package. These products are ideal for solid-state mass storage in embedded and portable applications that require smaller form-factor and more reliable data storage.

ATA-based solid-state mass storage technology is widely used in GPS and telematics, in-vehicle infotainment, portable and industrial computers, handheld data collection scanners, point-of-sale terminals, networking and telecommunications equipment, robotics, audio and video recorders, monitoring devices and set-top boxes.

The PATA NANDrive is a single device, solid-state drive designed for embedded ATA/IDE protocol systems and supports standard ATA/IDE protocol with up to PIO Mode-6[1)], Multi-Word DMA Mode-4[2)] and Ultra DMA Mode-4 interface. The PATA NANDrive device provides complete IDE hard disk drive functionality and compatibility in a 12 mm x 24 mm LBGA package for easy, space-saving mounting to a system motherboard. These products surpass traditional storage in their small size, security, reliability, ruggedness and low power consumption.

The integrated NAND flash controller with built-in advanced NAND management firmware communicates with the Host through the standard ATA protocol. It does not require any additional or proprietary software such as the Flash File System (FFS) and Memory Technology Driver (MTD).

The PATA NANDrive provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites. The PATA NANDrive is pre-programmed with a 10-Byte unique serial ID and has the option of programming an additional 10-Byte serial ID for even greater system security.

The PATA NANDrive's advanced NAND management technology enhances data security, improves endurance and accurately predicts the remaining lifespan of the NAND flash devices. This innovative technology combines robust NAND controller hardware error correction capabilities with advanced wear-leveling algorithms and bad block management to significantly extend the life of the product.

1) PATA NANDrive is capable of supporting PIO Mode-6, but Identify-Drive information report will show PIO Mode-4
2) PATA NANDrive is capable of supporting Multi-Word DMA Mode-4, but Identify-Drive information report will show MWDMA Mode-2

Contents

1.0 GENERAL DESCRIPTION

Each PATA NANDrive contains an integrated PATA NAND flash memory controller and discrete NAND flash die(s) in a LBGA package. Refer to Figure 2-1 for the PATA NANDrive block diagram.

1.1 Optimized PATA NANDrive

The heart of the PATA NANDrive is the PATA NAND flash memory controller, which translates standard PATA signals into flash media data and control signals. The following components contribute to the PATA NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU transfers the ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The PATA NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The PMU controls the power consumption of the PATA NANDrive. The PMU dramatically reduces the power consumption of the PATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the PATA NANDrive performance is an SRAM buffer. The buffer optimizes the Host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the PATA NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes to increase the longevity of flash media
3. Keeps track of data file structures

1.1.6 Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. During the design process, always provide access to the SCI port in the PCB design to aid in design validation.

1.1.8 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program and Erase operations to multiple flash media devices.

1.2 Advanced NAND Management

Advanced NAND management technology balances the wear on erased blocks with an advanced wear-leveling scheme. Advanced NAND management technology tracks the number of program/erase cycles within a group. When the Host updates data, higher priority is given to the less frequently written erase blocks; thereby, evenly distributing host writes within a wear-leveling group.

Advanced NAND management technology enhances the PATA NANDrive security with password protection and four independent protection zones, which can be set to Read-only or Hidden.

2.0 FUNCTION BLOCKS

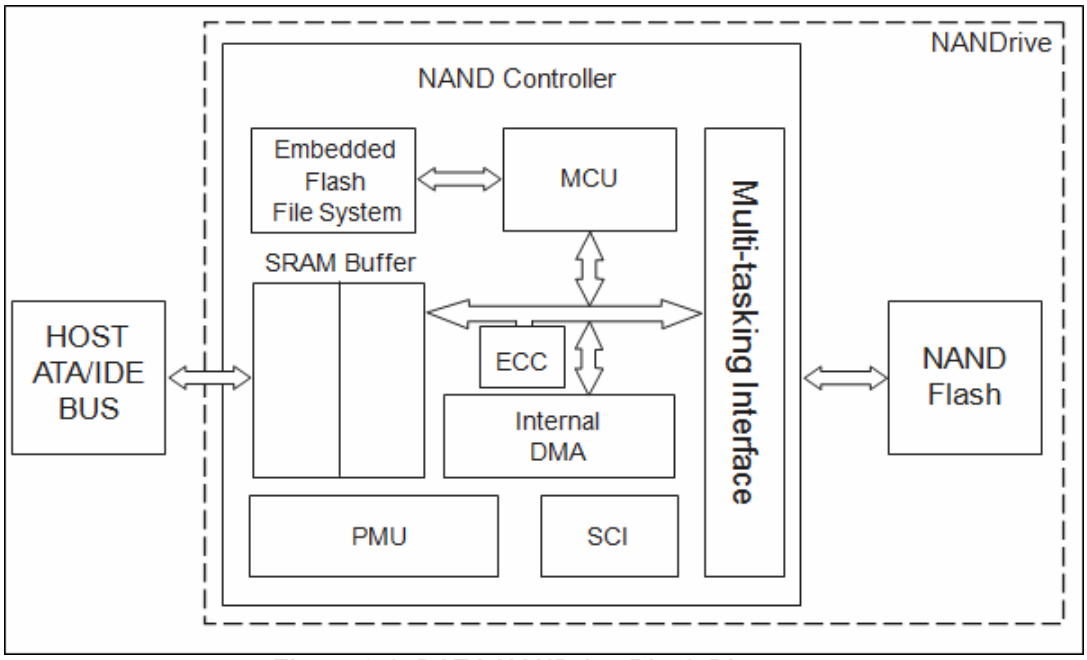


Figure 2-1: PATA NANDrive Block Diagram

3.0 PIN ASSIGNMENT

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output. Signals that the Host sources are designated as inputs, while signals that the PATA NANDrive sources are outputs.

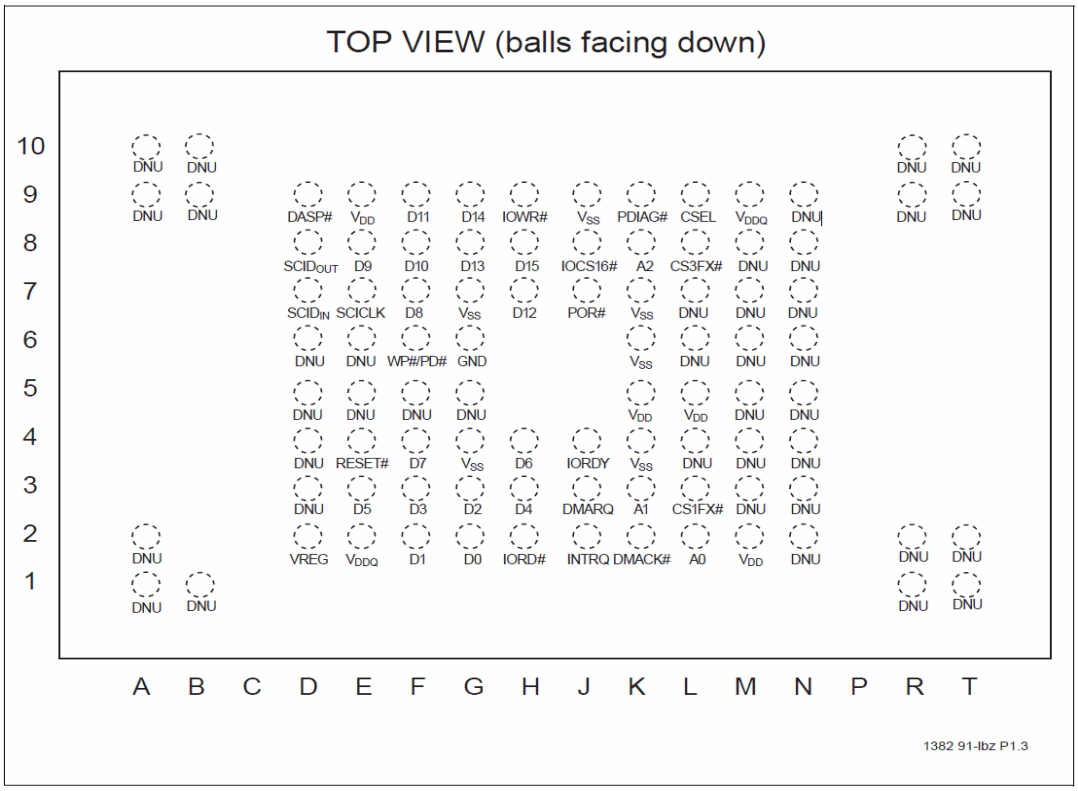


Figure 3-1: Pin Assignments for 91-Ball LBGA

Table 3-1: Pin Assignments (1 of 2)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	K3			
A0	L2			
D15	H8	I/O	I1Z/O2	D[15:0] Data bus
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7			
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK#	K2	I	I2U	DMA Acknowledge - input from Host
DMARQ	J3	O	O1	DMA Request to Host
CS1FX#	L3	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	L8			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	IORD#: This is an I/O Read Strobe generated by the Host. When Ultra DMA mode is not active, this signal gates I/O data from the device. (This pin supports three functions)
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the Host to indicate that the Host is ready to receive Ultra DMA data-in bursts. The Host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the Host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The Host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	H9	I	I2Z	IOWR#: This is an I/O Write Strobe generated by the Host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device. (This pin supports two functions)
				STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst

Table 3-1: Pin Assignments (2 of 2)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
IORDY	J4	O	O1	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions)
				DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
				DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the Host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
IOCS16#	J8	O	O2	This output signal is asserted low when the device is indicating a Word data transfer cycle.
INTRQ	J2	O	O1	This signal is the active high Interrupt Request to the Host.
PDIAG#	K9	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O6	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the Host.
WP#/PD#	F6	I	I3U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
Serial Communication Interface (SCI)				
$SCID_{OUT}$	D8	O	O4	SCI data output. No external pull-up or pull-down resistor should connect to this signal.
$SCID_{IN}$	D7	I	I3U	SCI data input
SCICLK	E7	I	I3U	SCI clock
Miscellaneous				
V_{SS}	G4, G6, G7, K4, K6, K7, J9	PWR		Ground
V_{DD}	E9, K5, L5, M2	PWR		V_{DD} (3.3V)
V_{DDQ}	E2, M9	PWR		V_{DDQ} (5V/3.3V) for Host interface
POR#	J7	I	Analog Input	Power-on Reset (POR). Active low. Analog input for supply voltage detection
V_{REG}	D2	O		External capacitor pin
DNU	A1, A2, A9, A10, B1, B9, B10, D3, D4, D5, D6, E5, E6, F5, G5, L4, L6, L7, M3, M4, M5, M6, M7, M8, N2, N3, N4, N5, N6, N7, N8, N9, R1, R2, R9, R10, T1, T2, T9, T10			Do not use. All these pins should not be connected.

4.0 KEY PARAMETERS

Table 4-1 shows the PATA NANDrive default capacity and specific settings for heads, sectors and cylinders. Users can change the default settings in the drive ID table using the Identify-Drive command. If the total number of Bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. It should also be noted that if the total flash drive capacity exceeds the total default number of Bytes, the flash drive endurance will be reduced.

Table 4-1: Default PATA NANDrive Settings

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA (Logical Block Addressing)
512 MByte	512,483,328	993	16	63	1,000,944
1 GByte	1,024,966,656	1,986	16	63	2,001,888

Table 4-2: Sustained Performance

Product	Write Performance	Read Performance
GLS85LD0512-60-RI-LBTE	Up to 5 MByte/sec	Up to 17 MByte/sec
GLS85LD1001T-60-RI-LBTE	Up to 10 MByte/sec	Up to 30 MByte/sec

Table 4-3: Supported ATA Modes

Products	PIO	MWDMA	Ultra DMA
GLS85LD0512-60-RI-LBTE	Up to Mode-6 [1)]	Up to Mode-4 [2)]	Up to Mode-4
GLS85LD1001T-60-RI-LBTE	Up to Mode-6 [1)]	Up to Mode-4 [2)]	Up to Mode-4

Table 4-4: Advanced NAND Management Technology Write Cycles

Products	Write Cycles per Group	Number of Groups per Product	Wear-leveling Group Size	Cluster Size
GLS85LD0512-60-RI-LBTE	100M	4	128 MBytes	2 KBytes
GLS85LD1001T-60-RI-LBTE	100M	4	256 MBytes	4 KBytes

5.0 CONFIGURABLE WRITE PROTECT / POWER-DOWN MODES

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

5.1 Write Protect Mode

When the device is configured in the Write Protect mode, the WP#/PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP#/PD# pin should be asserted prior to issuing the destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Multiple, Write-Multiple-without-Erase, Write-Sector(s) Write-Sector-without-Track or Write-Verify. This will force the PATA NANDrive to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

5.2 Power-down Mode

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, the PATA NANDrive completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

6.0 POWER-ON INITIALIZATION

The PATA NANDrive is self-initialized during the first power-up. As soon as the power is applied to the PATA NANDrive it reports busy for typically up to five seconds while performing bad blocks search and low-level format. This initialization is a one-time event.

During the first self-initialization, the PATA NANDrive firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, the PATA NANDrive performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support and performing the low-level format.

If the drive initialization fails and a visual inspection is unable to determine the problem, Greenliant provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

7.0 ATA/IDE HOST INTERFACE

The ATA/IDE host interface can be used for PATA NANDrive manufacturing support. Greenliant provides an example of a DOS- and Windows™-based solution (an executable routine) for manufacturing debug and rework.

7.1 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting and for accessing the status of the controller's internal activities. The SCI consists of three active signals: $SCID_{OUT}$, $SCID_{IN}$ and SCICLK. Always provide access to the SCI port in the PCB design to aid in design validation.

8.0 LIFETIME EXPECTANCY

The PATA NANDrive with advanced NAND management technology significantly extends the life of a product with its extensive ECC and advanced wear-leveling algorithms.

For applications where data security is essential, the PATA NANDrive with advanced NAND management technology offers two additional protection features - protection zones and password protections.

Protection Zones - Up to four independent protection zones can be enabled as either Read-only or Hidden (Read/Write protected). If the zones are not enabled, the data is unprotected (default configuration).

Password Protection - Requires a customer-unique password to access information within the protected zones.

9.0 POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Please contact Greenliant to obtain the PATA NANDrive reference design schematics including the POR# circuit for the industrial PATA NANDrive offerings.

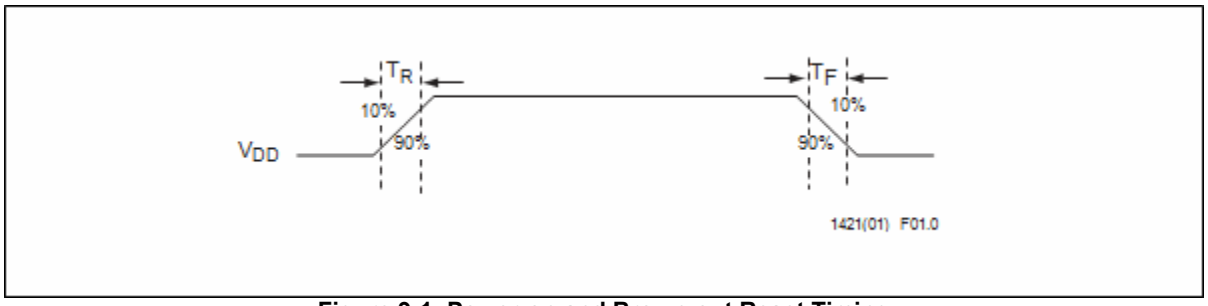


Figure 9-1: Power-on and Brown-out Reset Timing

Table 9-1: Power-on and Brown-out Reset Timing

Item	Symbol	Min	Max	Units
V_{DD}/POR# Rise Time	T_R		250	ms
V_{DD}/POR# Fall Time	T_F		250	ms

10.0 SOFTWARE INTERFACE

10.1 I/O Transfer Function

The default operation for the PATA NANDrive is 16-bit. However, if the Host issues a SET-FEATURE command to enable 8-bit mode, the PATA NANDrive permits 8-bit data access. The following table defines the function of various operations.

Table 10-1: I/O Function

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	VIL	VIL	X	X	X	Undefined	Undefined
Standby Mode	VIH	VIH	X	X	X	High Z	High Z
Task File Write	VIH	VIL	1-7H	VIH	VIL	X	Data In
Task File Read	VIH	VIL	1-7H	VIL	VIH	High Z	Data Out
Data Register Write	VIH	VIL	0	VIH	VIL	In [3)]	In
Data Register Read	VIH	VIL	0	VIL	VIH	Out [3)]	Out
Control Register Write	VIL	VIH	6H	VIH	VIL	X	Control In
Alt Status Read	VIL	VIH	6H	VIL	VIH	High Z	Status Out

3) If 8-bit data transfer mode is enabled.
In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be VIH or VIL, but no other value.

10.2 Command Description

This section defines the software requirements and the format of the commands the Host sends to the PATA NANDrive. Commands are issued to the PATA NANDrive by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. With the exception of commands listed in Sections “Idle – 97h or E3h”, “Set-Sleep-Mode – 99h or E6h”, “Set-WP#/PD#-Mode - 8Bh”, the PATA NANDrive complies with ATA-6 Specifications.

Table 10-2: NANDrive Command Set

Command	Code	FR [4),5)]	SC [5), 6)]	SN [5), 7)]	CY [5), 8)]	DH [9), 10)]	LBA [5), 11)]
Check-Power-Mode	E5h or 98h	-	-	-	-	D	-
Execute-Drive-Diagnostic	90h	-	-	-	-	D	-
Erase-Sector(s)	C0h	-	Y	Y	Y	Y	Y
Flush-Cache	E7h	-	-	-	-	D	-
Format-Track	50h	-	Y	-	Y	Y	Y
Identify-Drive	ECh	-	-	-	-	D	-
Idle	E3h or 97h	-	Y	-	-	D	-
Idle-Immediate	E1h or 95h	-	-	-	-	D	-
Initialize-Drive-Parameters	91h	-	Y	-	-	Y	-
NOP	00h	-	-	-	-	D	-
Read-Buffer	E4h	-	-	-	-	D	-
Read-DMA	C8h or C9h	-	Y	Y	Y	Y	Y
Read-Multiple	C4h	-	Y	Y	Y	Y	Y
Read-Sector(s)	20h or 21h	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40h or 41h	-	Y	Y	Y	Y	Y
Recalibrate	1Xh	-	-	-	-	D	-
Request-Sense	03h	-	-	-	-	D	-
Security-Disable-Password	F6h	-	-	-	-	D	-
Security-Erase-Prepare	F3h	-	-	-	-	D	-
Security-Erase-Unit	F4h	-	-	-	-	D	-
Security-Freeze-Lock	F5h	-	-	-	-	D	-
Security-Set-Password	F1h	-	-	-	-	D	-
Security-Unlock	F2h	-	-	-	-	D	-
Seek	7Xh	-	-	Y	Y	Y	Y
Set-Features	EFh	Y	-	-	-	D	-
SMART [12)]	B0h	Y	Y	Y	Y	D	-
Set-Multiple-Mode	C6h	-	Y	-	-	D	-
Set-Sleep-Mode	E6h or 99h	-	-	-	-	D	-
Set-WP#/PD#-Mode	8Bh	Y	-	-	-	D	-
Standby	E2h or 96h	-	-	-	-	D	-
Standby-Immediate	E0h or 94h	-	-	-	-	D	-
Translate-Sector	87h	-	Y	Y	Y	Y	Y
Write-Buffer	E8h	-	-	-	-	D	-
Write-DMA	CAh or CBh	-	Y	Y	Y	Y	Y
Write-Multiple	C5h	-	Y	Y	Y	Y	Y
Write-Multiple-Without-Erase	CDh	-	Y	Y	Y	Y	Y
Write-Sector(s)	30h or 31h	-	Y	Y	Y	Y	Y
Write-Sector(s)-Without-Erase	38h	-	Y	Y	Y	Y	Y
Write-Verify	3Ch	-	Y	Y	Y	Y	Y

4) FR - Features register
5) Y - The register contains a valid parameter for this command
6) SC - Sector Count register
7) SN - Sector Number register
8) CY - Cylinder registers
9) For the Drive/Head register: Y means both the Drive and Head parameters are used; D means only the Drive parameter is valid and not the Head parameter
10) DH - Drive/Head register
11) LBA - Logical Block Address mode supported (see command descriptions for use)
12) Please ask your Greenliant contact about SMART command support

10.2.1 Identify-Drive – ECh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the Host to receive parameter information from the PATA NANDrive. This command has the same protocol as the Read-Sector(s) command. The parameter Words in the buffer have the arrangement and meanings defined in Table 10-3. All reserved bits or Words are zero. The following table gives the definition for each field in the Identify-Drive information.

Table 10-3: Identify-Drive Information (1 of 2)

Word Address	Total Bytes	Default Value	Data Field Type Information
0	2	044Ah	General configuration bit
1	2	bbbbh [14)]	Default number of cylinders
2	2	0000h	Reserved
3	2	bbbbh [14)]	Default number of heads
4	2	0000h	Reserved
5	2	xxxxh	Vendor Unique
6	2	bbbbh [14)]	Default number of sectors per track
7-8	4	bbbbh [14)]	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	2	xxxxh [13)]	Vendor Unique
10-14	10	eeeeH [16)]	User-programmable serial number in ASCII
15-19	10	ddddH [17)]	Greenliant preset, unique ID in ASCII
20	2	0002h	Buffer type
21	2	xxxxh [13)]	Vendor Unique
22	2	xxxxh [13)]	Vendor Unique
23-26	8	aaaah [18)]	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	40	cccch [19)]	User Definable Model number
47	2	8001h	Maximum number of sectors on Read/Write-Multiple command
48	2	0000h	Reserved
49	2	0B00h	Capabilities
50	2	0000h	Reserved
51	2	0200h	PIO Data Transfer Cycle Timing Mode
52	2	0000h	Reserved
53	2	0007h	Translation parameters are valid
54	2	nnnnh [15)]	Current numbers of cylinders
55	2	nnnnh [15)]	Current numbers of heads
56	2	nnnnh [15)]	Current sectors per track
57-58	4	nnnnh [15)]	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	2	010xh	Multiple sector setting
60-61	4	nnnnh [15)]	Total number of sectors addressable in LBA mode
62	2	0000h	Reserved
63	2	0x07h	DMA data transfer is supported in NAND Controller
64	2	0003h	Advanced PIO Transfer mode supported
65	2	0078h	120 ns cycle time support for Multi-Word DMA Mode-2
66	2	0078h	120 ns cycle time support for Multi-Word DMA Mode-2
67	2	0078h	PIO Mode-4 supported
68	2	0078h	PIO Mode-4 supported

Table 10-3: Identify-Drive Information (2 of 2)

Word Address	Total Bytes	Default Value	Data Field Type Information
69-79	22	0000h	Reserved
80	2	007Eh	ATA major version number
81	2	0019h	ATA minor version number
82	2	706Bh	Features/command sets supported
83	2	400Ch	Features/command sets supported
84	2	4000h	Features/command sets supported
85-87	6	xxxxh [13)]	Features/command sets enabled
88	2	xx1Fh	UDMA modes
89	2	xxxxh [13)]	Time required for security erase unit completion
90	2	xxxxh [13)]	Time required for enhanced security erase unit completion
91-127	74	0000h	Reserved
128	2	xxxxh [13)]	Security Status
129-159	62	0000h	Vendor unique bytes
160-162	6	0000h	Reserved
163	2	xxx2h	CF Advanced True IDE Timing Mode capabilities and settings
164-255	184	0000h	Reserved

13) xxxx - This field is subject to change by the Host or the device.
14) bbbb - default value set by the controller. The selections could be user programmable.
15) n - calculated data based on product configuration
16) eeee - the default value is '0000000000'
17) dddd - unique number of each device
18) aaaa - any unique Greenliant firmware revision
19) cccc – the default value is "xxxMB NANDrive" or "xxxGB NANDrive" where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

Word 0: General Configuration

This field informs the Host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Word 7-8: Number of Sectors

This field contains the number of sectors per the PATA NANDrive. This Double Word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

Word 10-19: Serial Number

The contents of this field are right justified and padded with spaces (20h). The right-most ten bytes are Greenliant preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of spaces.

Word 20: Buffer Type

This field defines the buffer capability:

0002h: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the PATA NANDrive.

Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Word 27-46: Model Number

This field is reserved for the model number for this product.

Word 47: Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

Word 49: Capabilities

Bit	Function
13	Standby Timer 0: Forces sleep mode when Host is inactive
11	IORDY Support 1: PATA NANDrive supports PIO Mode-4
9	LBA support 1: PATA NANDrive supports LBA mode addressing
8	DMA Support 1: DMA mode is supported

Word 51: PIO Data Transfer Cycle Timing Mode

This field contains the mode for PIO data transfer. The PATA NANDrive supports PIO Mode-4.

Word 53: Translation Parameters Valid

Bit	Function
0	1: Words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: Words 64-70 are valid to support PIO Mode-3 and -4.
2	1: Word 88 is valid to support Ultra DMA data transfer.

Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contain the current number of user addressable Cylinders, Heads and Sectors/Track in the current translation mode.

Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01h which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this Word by default contains a 00h which indicates that Read/Write Multiple commands are not valid.

Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the PATA NANDrive in LBA mode only.

Word 63: Multi-Word DMA Transfer Mode

This field identifies the Multi-Word DMA transfer modes supported by the PATA NANDrive and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function
15-11	Reserved
10	Multi-Word DMA mode 2 selected 1: Multi-Word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-Word DMA mode 2 is not selected
9	Multi-Word DMA mode 1 selected 1: Multi-Word DMA mode 1 is selected and 8 and 10 should be cleared to 0 0: Multi-Word DMA mode 1 is not selected
8	Multi-Word DMA mode 0 selected 1: Multi-Word DMA mode 0 is selected and bits 9 and 10 are cleared to 0 0: Multi-Word DMA mode 0 is not selected
7-3	Reserved
2	Multi-Word DMA mode 2 supported

1: Multi-Word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1

1 Multi-Word DMA mode 1 supported
1: Multi-Word DMA mode 1 and below are supported

0 Multi-Word DMA mode 0 supported
1: Multi-Word DMA mode 0 is supported

Word 64: Advanced PIO Data Transfer Mode [3)]

Bits [7:0] are defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of Word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits [7:2] are reserved for future PIO modes.

Bit	Function
0	1: PATA NANDrive supports PIO Mode-3
1	1: PATA NANDrive supports PIO Mode-4

Word 65: Minimum Multi-Word DMA Transfer Cycle Time Per Word [20)]

This field defines the minimum Multi-Word DMA transfer cycle time per Word. This field defines, in nanoseconds, the minimum cycle time that the PATA NANDrive supports when performing Multi-Word DMA transfers on a per Word basis. The PATA NANDrive supports up to Multi-Word DMA Mode-2, so this field is set to 120ns.

20) The PATA NANDrive is capable of supporting Multi-Word DMA Mode-4 cycle time of 80ns (0050H). Contact Greenliant sales/ FAE for more details.

Word 66: Device Recommended Multi-Word DMA Cycle Time [20)]

This field defines the PATA NANDrive recommended Multi-Word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per Word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a Host runs at a faster cycle rate by operating at a cycle time of less than this value, the PATA NANDrive may negate DMARQ for flow control. The rate at which DMARQ is negated could result in Advance Information reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. The PATA NANDrive supports Multi-Word DMA Mode-2, so this field is set to 120ns.

Word 67: Minimum PIO Transfer Cycle Time Without Flow Control [21)]

This field defines, in nanoseconds, the minimum cycle time that, if used by the Host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of Word 53 shall be set to one. The PATA NANDrive supports PIO Mode-4, so this field is set to 120ns.

21) The PATA NANDrive is capable of supporting PIO Mode-6 cycle time of 80ns (0050H). Contact Greenliant sales/ FAE for more details.

Word 68: Minimum PIO Transfer Cycle Time With IORDY [21)]

This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of Word 53 shall be set to one. The PATA NANDrive supports PIO Mode-4, so this field is set to 120ns.

Word 80: Major Version Number

If not 0000h or FFFFh, the device claims compliance with the major version(s) as indicated by bits [6:1] being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. The PATA NANDrive supports ATA-1 to ATA-6.

Word 81: Minor Version Number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, Word 81 should be 0000h or FFFFh.

A value of 0019h reported in Word 81 indicates ATA-6 T13/1410D revision 3a guided the implementation.

Words 82-84: Features/command sets supported

Words 82, 83 and 84 indicate the features and command sets supported. A value of 706Bh is reported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	1: SMART feature set is supported

Word 83

The values in this Word should not be depended on by host implementers.

Bit	Function
15	0: Provides an indication whether the features/command sets supported Words are not valid
14	1: Provides an indication whether the features/command sets supported Words are valid
13-9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is supported
2	1: CFA feature set is supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this Word should not be depended on by host implementers.

Bit	Function
15	0: Provides an indication whether the features/command sets supported Words are not valid
14	1: Provides an indication whether the features/command sets supported Words are valid
13-0	0: Reserved

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled. The Host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled
	1: NOP command is enabled
13	0: Read Buffer command is not enabled
	1: Read Buffer command is enabled
12	0: Write Buffer command is not enabled
	1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled
	1: Look-ahead is enabled
5	0: Write cache is not enabled
	1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled
	1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command
	1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

Word 86

Bit	Function
15-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled
2	0: CFA feature set is disabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this Word should not be depended on by host implementers.

Bit	Function
15	0: Provides an indication whether the features/command sets supported Words are not valid
14	1: Provides an indication whether the features/command sets supported Words are valid
13-0	0: Reserved

Word 88

Bit	Function
15-13	Reserved
12	1: Ultra DMA mode 4 is selected
	0: Ultra DMA mode 4 is not selected
11	1: Ultra DMA mode 3 is selected
	0: Ultra DMA mode 3 is not selected
10	1: Ultra DMA mode 2 is selected
	0: Ultra DMA mode 2 is not selected
9	1: Ultra DMA mode 1 is selected
	0: Ultra DMA mode 1 is not selected
8	1: Ultra DMA mode 0 is selected
	0: Ultra DMA mode 0 is not selected
7-5	Reserved
4	1: Ultra DMA mode 4 and below are supported
3	1: Ultra DMA mode 3 and below are supported
2	1: Ultra DMA mode 2 and below are supported
1	1: Ultra DMA mode 1 and below are supported
0	1: Ultra DMA mode 0 is supported

Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 128: Security Status

Bit	Function
8	Security Level
	1: Security mode is enabled and the security level is maximum
	0: and security mode is enabled, indicates that the security level is high
5	Enhanced security erase unit feature supported
	1: Enhanced security erase unit feature set is supported
4	Expire
	1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset
3	Freeze
	1: Security is frozen
2	Lock
	1: Security is locked
1	Enable/Disable
	1: Security is enabled
	0: Security is disabled
0	Capability
	1: PATA NANDrive supports security mode feature set
	0: PATA NANDrive does not support security mode feature set

Word 163: CF Advanced True IDE Timing Mode Capability and Settings

This Word describes the capabilities and current settings for CF modes utilizing the True IDE interface.

Four separate fields determine support and selection options in the Advanced PIO and Advanced Multiword DMA timing modes. For information on the older modes, see "Word 63: Multi-Word DMA Transfer Mode" and "Word 64: Advanced PIO Data Transfer Mode". When the Identity-Drive command executes, the device returns 0492h.

Bit Function

2-0 Advanced True IDE PIO Mode Support. Indicates the maximum True IDE PIO Mode supported by the card

Value	Time
0	Specified in Word64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

5-3 Advanced True IDE Multi-Word DMA Mode Support. Indicates the maximum True IDE Multi-Word DMA Mode supported by the card

Value	Time
0	Specified in Word63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

8-6 Advanced True IDE PIO Mode Support. Indicates the current True IDE PIO Mode selected on the card

Value	Time
0	Specified in Word64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

11-9 Advanced True IDE Multi-Word DMA Mode Support. Indicates the current True IDE Multi-Word DMA Mode selected on the card

Value	Time
0	Specified in Word63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

15-12 Reserved

10.2.2 Set-Features – EFh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the Host to establish or select certain features. Table 10-4 defines all features that are supported.

Table 10-4: Features Supported

Feature	Operation
01h	Enable 8-bit data transfers.
02h	Enable Write cache
03h	Set transfer mode based on value in Sector Count register. Table 10-5 defines the values.
09h	Enable Extended Power Operations
55h	Disable Read Look Ahead.
66h	Disable Power-on Reset (POR) establishment of defaults at software reset.
69h	NOP - Accepted for backward compatibility.
81h	Disable 8-bit data transfer.
82h	Disable Write Cache
89h	Disable Extended Power operations
96h	NOP - Accepted for backward compatibility.
97h	Accepted for backward compatibility. Use of this Feature is not recommended.
AAh	Enable Read-Look-Ahead
CCh	Enable Power-on Reset (POR) establishment of defaults at software reset.

Features 01h and 81h are used to enable and clear 8-bit data transfer mode. If the 01h feature command is issued all data transfers will occur on the low order D[7:0] data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02h and 82h allow the Host to enable or disable write cache in the PATA NANDrive that implements write cache. When the subcommand Disable-Write-Cache is issued, the PATA NANDrive should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the Host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The Host may change the selected modes by the Set-Features command.

Feature 55h is the default feature for the PATA NANDrive. Therefore, the Host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66h and CCh can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

Table 10-5: Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	Mode [22]
Multi-Word DMA mode	00100b	Mode [22]
Ultra-DMA mode	01000b	Mode [22]
Reserved	Other	N/A

22) Mode = transfer mode number, all other values are not valid

10.2.3 Idle – 97h or E3h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97h or E3h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the PATA NANDrive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms [23].

23) The time base equals to 5 ms is different from the ATA specification.

10.2.4 Set-Sleep-Mode – 99h or E6h

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99h or E6h							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the PATA NANDrive to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted, but not required). Sleep mode is also entered when internal timers expire so the Host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

10.2.5 Set-WP#/PD#-Mode - 8Bh

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8Bh							
C/D/H (6)	X			Drive	X			
Cyl High (5)	6Eh							
Cyl Low (4)	44h							
Sec Num (3)	72h							
Sec Cnt (2)	50h							
Feature (1)	55h or AAh							

This command configures the WP#/PD# pin for either the Write Protect mode or the Power-down mode. When the Host sends this command to the device with the value AAH in the feature register, the WP#/PD# pin is configured for the Write Protect mode. The Write Protect mode is the factory default setting. When the Host sends this command to the device with the value 55h in the feature register, WP#/PD# is configured for the Power-down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

10.2.6 Error Posting

The following table summarizes the valid status and error values for the PATA NANDrive command set.

Table 10-6: Error and Status Register [24), 25)]

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic						V		V		V
Erase-Sector(s)	V		V	V	V	V	V	V		V
Flush-Cache				V		V	V	V		V
Format-Track				V		V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request-Sense				V		V		V		V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP#/PD#-Mode				V		V		V		V
SMART				V		V	V	V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Translate-Sector	V		V	V	V	V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Multiple-Without-Erase	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-Without-Erase	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

24) The Host is required to reissue any media access command (such as Read-Sector and Write Sector) that ends with an error condition.

25) V = valid on this command.

11.0 ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Absolute Maximum Stress Ratings - Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Storage Temperature ..... -55°C to +125°C
D.C. Voltage on Pin types [26] I3, I4, O4, and O5 to Ground Potential ..... -0.5V to V_{DD} +0.5V
Transient Voltage (<20 ns) on Pin types [26] I3, I4, O4, and O5 to Ground Potential ..... -2.0V to V_{DD} +2.0V
D.C. Voltage on Pin types [26] I1, I2, O1, O2, and O6 to Ground Potential ..... -0.5V to V_{DDQ} +0.5V
Transient Voltage (<20 ns) on Pin types [26] I1, I2, O1, O2, and O6 to Ground Potential ..... -2.0V to V_{DDQ} +2.0V
Package Power Dissipation Capability (TA = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) ..... 300°C
Surface Mount Solder Reflow Temperature [28] ..... 260°C for 10 seconds
Output Short Circuit Current [27] 50mA

26) Refer to Table 3-1 "Pin Assignment"
27) Outputs shorted for no more than one second. No more than one output shorted at a time.
28) Refer to Figure 12-1

11.1.1 Absolute Maximum Power Pin Stress Ratings

Table 11-1: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	V_{DDQ} V_{DD}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to VDD + 0.5V max

11.2 Operating Ratings

Table 11-2: Operating Range

Range	Ambient Temperature	V_{DDQ}				V_{DD}	
		3.3V		5V		3.3V	
		Min	Max	Min	Max	Min	Max
Industrial	-40°C to +85°C	3.135V	3.465V	4.5V	5.5V	3.135V	3.465V

11.3 AC Characteristics

11.3.1 AC Conditions of Test

Table 11-3: AC Conditions of Test

Input Rise/Fall Time	Output Load
10 ns	CL = 100 pF

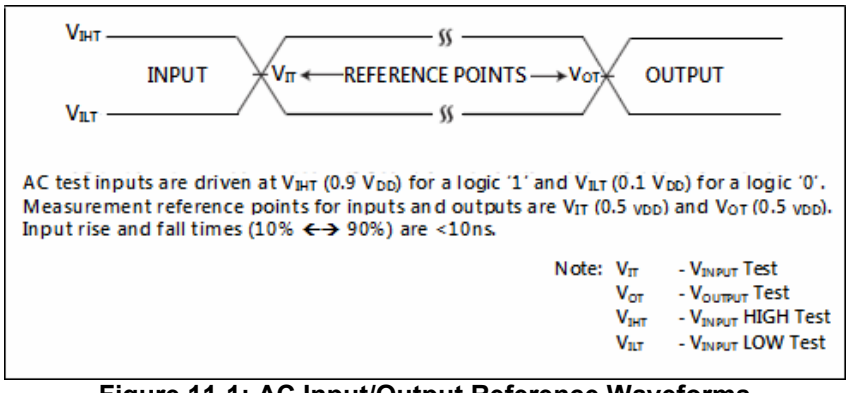


Figure 11-1: AC Input/Output Reference Waveforms

11.4 Recommended System Power-on Timing

Table 11-4: Recommended System Power-on Timing [29)]

Symbol	Parameter	Typical	Maximum	Units
TPU-INITIAL	Drive Initialization to Ready	3sec + (0.5 sec/GByte)	100	sec
TPU-READY1	Host Power-on/Reset to Ready Operation	200	1,000	ms
TPU-WRITE1	Host Power-on/Reset to Write Operation	200	1,000	ms

29) This parameter is measured only for initial qualification and after a design or process change that could affect.

11.5 Reliability Characteristics [29)]

Table 11-5: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
ILTH	Latch Up	100 + IDD	mA	JEDEC Standard 78

11.6 Capacitance [29)]

Table 11-6: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
CI/O	I/O Pin Capacitance	VI/O = 0V	10 pF
CIN	Input Capacitance	VIN = 0V	10 pF

11.7 DC Characteristics

Table 11-8: DC Characteristics for Host Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
VIH1	I1	Input Voltage	2		V	V_{DDQ}=V_{DDQ} Max
VIL1				0.8	V	V_{DDQ}=V_{DDQ} Min
IIL1	I1Z	Input Leakage Current	-10	10	µA	V_{IN} = GND to V_{DDQ}, V_{DDQ}=V_{DDQ} Max
IU1	I1U	Input Pull-Up Current	-150	-6	µA	V_{OUT}=GND, V_{DDQ}=V_{DDQ} Max
VT+2	I2	Input Voltage Schmitt Trigger		2.0	V	V_{DDQ}=V_{DDQ} Max
VT-2			0.8		V	V_{DDQ}=V_{DDQ} Min
IIL2	I2Z	Input Leakage Current	-10	10	µA	V_{IN} = GND to V_{DDQ}, V_{DDQ}=V_{DDQ} Max
IU2	I2U	Input Pull-Up Current	-150	-6	µA	V_{OUT}=GND, V_{DDQ}=V_{DDQ} Max
VOH1	O1	Output Voltage	2.4		V	IOH1=IOH1 Min
VOL1				0.4	V	IOL1=IOL1 Max
IOH1		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
IOL1				4	mA	V_{DDQ}=V_{DDQ} Min
VOH2	O2	Output Voltage	2.4		V	IOH2=IOH2 Min
VOL2				0.4	V	IOL2=IOL2 Max
IOH2		Output Current	-8		mA	V_{DDQ}=2.7V
IOL2				8	mA	V_{DDQ}=V_{DDQ} Min
VOH6	O6	Output Voltage	2.4		V	IOH6=IOH6 Min
VOL6				0.4	V	IOL6=IOL6 Max
IOH6		Output Current	-4		mA	V_{DDQ}=2.7-3.465V
IOL6				12	mA	V_{DDQ}=2.7-3.465V
IOH6		Output Current	-4		mA	V_{DDQ}=4.5-5.5V
IOL6				12	mA	V_{DDQ}=4.5-5.5V

Table 11-9: Power Consumption

Symbol	Type	Device	Parameter	Min	Max	Units	Conditions
IDD [30), 31)]	PWR	GLS85LD0512 -60-RI-LBTE	Power supply current (TA = -40°C to +85°C)		130	mA	V_{DD}=V_{DD} Max, V_{DDQ}=V_{DDQ} Max
ISP	PWR		Sleep/Standby/Idle current (TA = -40°C to +85°C)		1000	µA	V_{DD}=V_{DD} Max, V_{DDQ}=V_{DDQ} Max
IDD [30), 31)]	PWR	GLS85LD1001T -60-RI-LBTE	Power supply current (TA = -40°C to +85°C)		160	mA	V_{DD}=V_{DD} Max, V_{DDQ}=V_{DDQ} Max
ISP	PWR		Sleep/Standby/Idle current (TA = -40°C to +85°C)		1050	µA	V_{DD}=V_{DD} Max, V_{DDQ}=V_{DDQ} Max

30) Sequential data transfer from host interface and write data to media.
31) This parameter is measured only for initial qualification and after a design or process change that could affect.

12.0 APPENDIX

12.1 Differences between the PATA NANDrive and the ATA Specifications

12.1.1 Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in the ATA specifications.

12.1.2 Recovery from Sleep Mode

For the PATA NANDrive devices, recovery from sleep mode is accomplished by simply issuing another command to the device. Hardware or Software reset is not required.

12.2 Reflow Profile

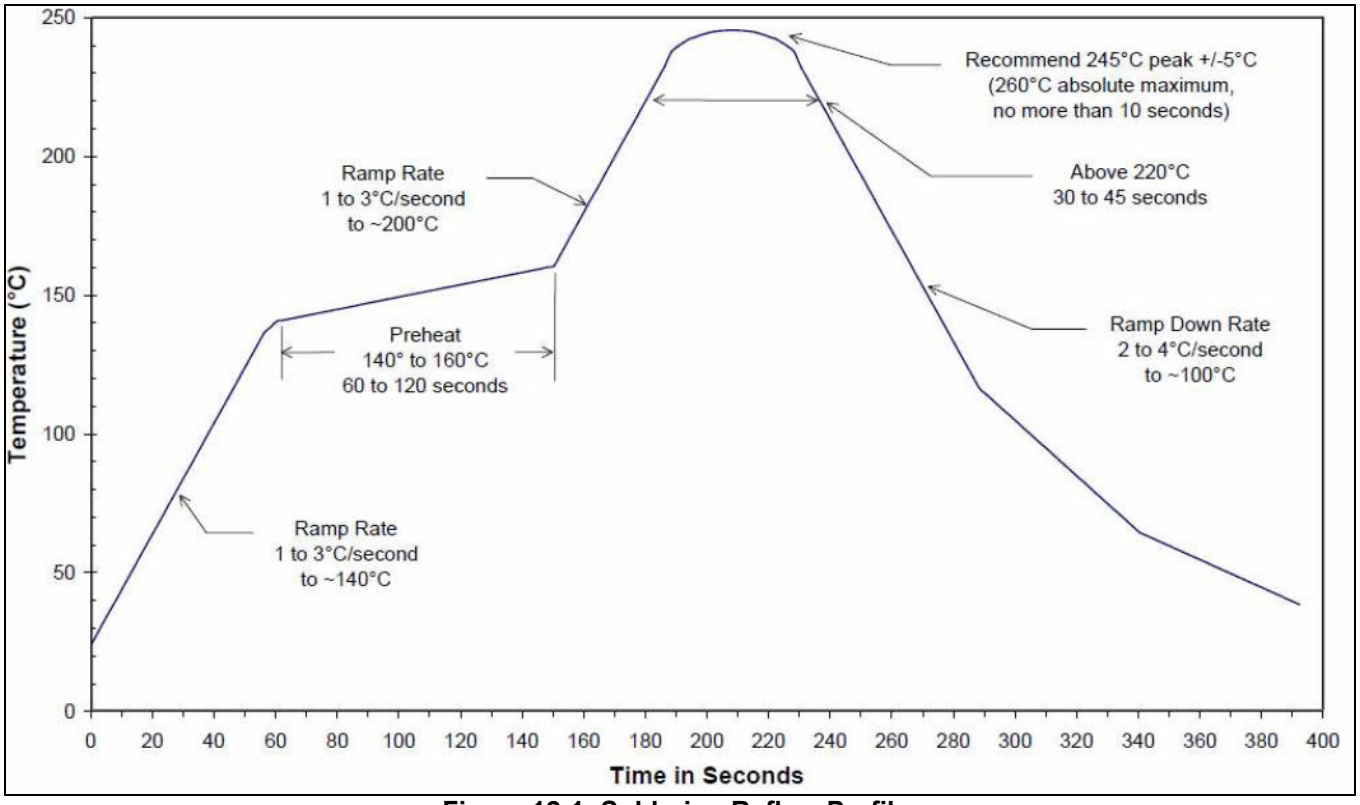
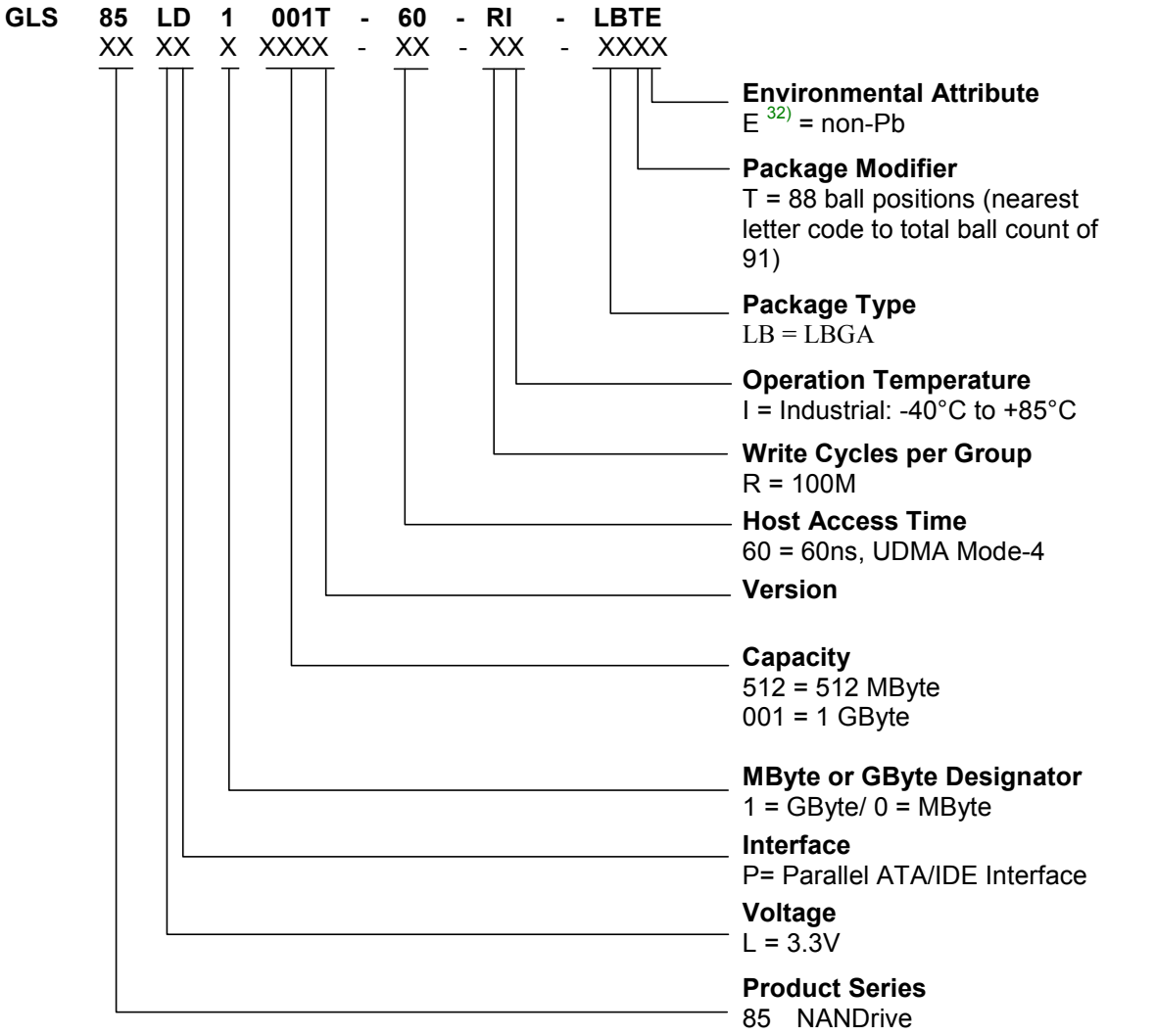


Figure 12-1: Soldering Reflow Profile

12.3 Product Ordering Information



32) Environmental suffix "E" denotes non-Pb solder. Greenliant non-Pb solder devices are "RoHS Compliant."

Valid Combinations 33)

PATA NANDrive Product

GLS85LD0512-60-RI-LBTE/ GLS85LD1001T-60-RI-LBTE

PATA NANDrive Evaluation Board (xxCN: xx-pin ATA Interface EVB, K: Kit)

GLS85LD0512-60-RI-40CN-K, GLS85LD1001T-60-RI-40CN-K,
GLS85LD0512-60-RI-44CN-K, GLS85LD1001T-60-RI-44CN-K

33) Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

12.4 Packaging Diagram

12.4.1 LBTE Package

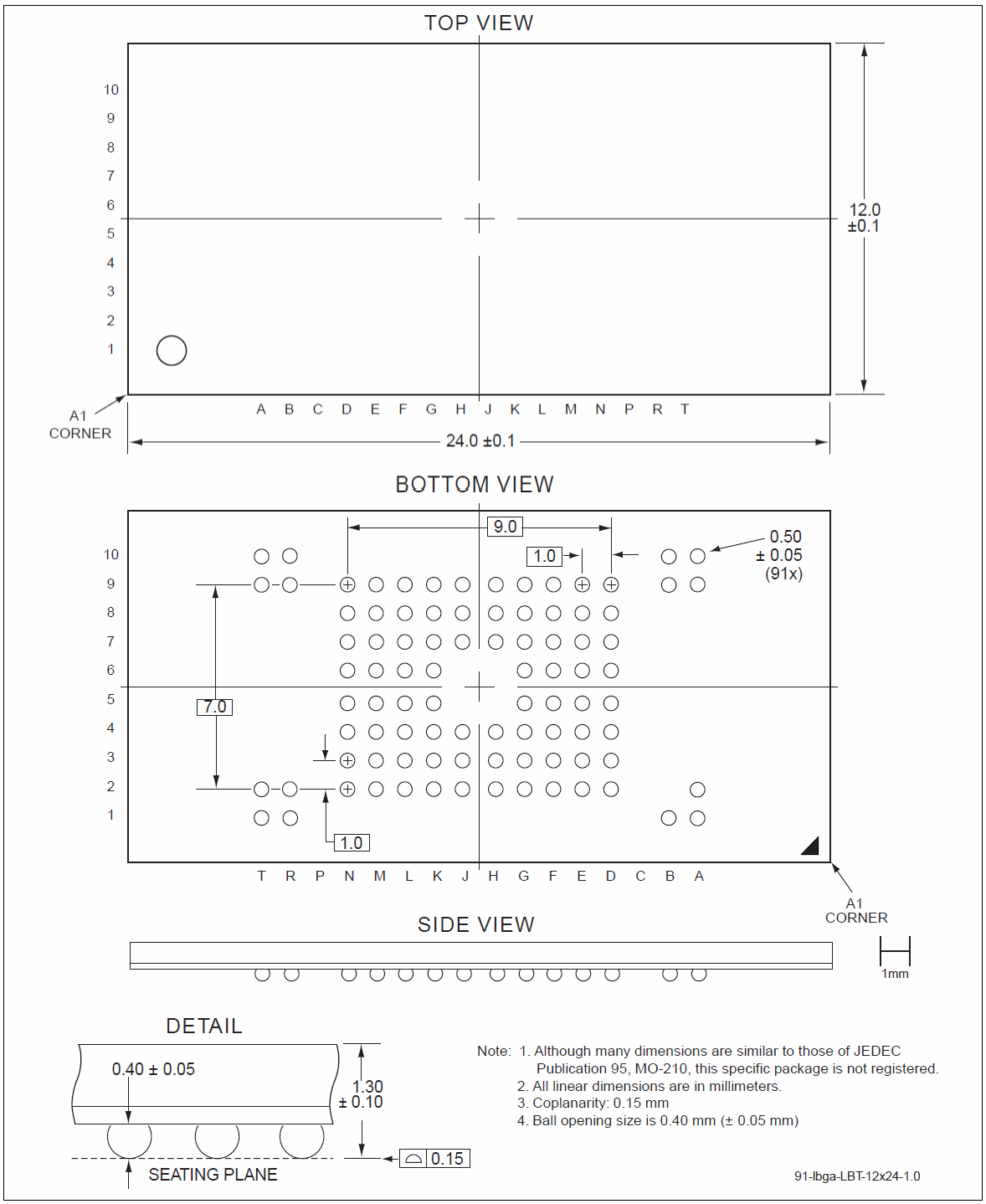


Figure 12-2: PATA NANDrive 91-Ball, Ball Grid Array (BGA) Greenliant Package Code: LBTE

Note: All linear dimensions are in millimeters.
Un-tolerance dimensions are nominal target values.
Co-planarity: 0.15 mm.
Ball opening size is 0.40 mm (± 0.05 mm).

12.5 Reference Documents

Table 12-1: Reference Document

Title	Revision	Date
NANDrive SMART Specification	02.000	Feb 10, 2011
WindowsPT2 User Guide	02.000	March 1, 2011

12.6 Revision History

Table 12-2: Revision History

Number	Description	Date
00.000	- Initial release for SST85LD0512/SST85LD1001T/SSTLD1002U Data Sheet	April, 2008
01.000	- Added 5I (100M cycle endurance) information including updates in "Features" , "General Description" , "Capacity Specification" , "Lifetime Expectancy" , "Software Interface" "Electrical Specifications" , and "Product Ordering Information". - Changed pin K2 from DMACK to DMACK# in Figure 2 and Table 1.	September, 2008
02.000	- Preliminary Specifications-to-Data Sheet phase change	November, 2008
03.000	- End-of-Life valid combinations SST85LD0512-60-5I-LBTE, SST85LD1001T-60-5ILBTE, and SST85LD1002U-60-5I-LBTE. See S71382 (02). - Removed all references to 100M cycle endurance in Features, page 1 and Standard NANDrive on page 2 and page 12. - Removed SST85LD0512-60-5I-LBTE, SST85LD1001T-60-5I-LBTE, and - SST85LD1002U-60-5I-LBTE from Table 3 on page 7, Table 4 on page 7, and Table 20 on page 30.	September, 2008
04.000	- Applied the new document format - Updated Figure 1.	October, 2009
05.000	- Transferred from SST to Greenliant	May, 2010
06.000	- Updated the typical of power consumption for GLS85LD1001T-60-RI-LBTE and the performance value for Sustained Sequential Write, on Page1. - Removed the descriptions of Endurance and Data retention on Page1. - Corrected the description and I/O type of IORDY on pin assignment table, on Table3-1 on Page6. - Added Solder Reflow Profile, Figure12-1 on Page25. - Changed the definition of "R" in the ordering information from Endurance to Write Cycles per Group on Page26. - Added Reference Document table, Table12-1 on Page28.	July, 2011