Industrial / Commercial Temp **SATA NANDrive**™



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Features

Industry Standard Serial ATA (SATA) Host Interface

- SATA 1.5 Gb/s or SATA 3.0 Gb/s 1)
- ATA/ATAPI-8 compliant
- Supports 48-bit address feature set

Performance

- Sequential data read -Up to 110 MByte/sec*
- Sequential data write Up to 60 MByte/sec*
 * measured using 128 KByte transfer size

Power Management

- 3.3V and 1.2Vpower supply
- Host SATA interface power management
- Immediate disabling of unused circuitry without host intervention

Power Specifications ²⁾

Active mode:

820mW typical (GLS85LS1064B) 565mW typical (GLS85LS1032B) 440mW typical (GLS85LS1016B)

360mW typical (GLS85LS1008B)
- Idle mode: 210mW typical

- Standby mode: 190mW typical

Expanded Data Protection

 Added data security through user-selectable protection zones

Integrated Voltage Detector

- Detects supply voltage fluctuations and generates reset during power-up and powerdown to prevent inadvertent writes
- Supports SMART Commands
- 20-Byte Serial Number
 - Factory pre-programmed 10-Byte unique ID
 - User-programmable 10-Byte ID
- Robust Built-in ECC
- NAND Configuration
 - 2 bits per cell (MLC)
- Temperature Range
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C

FBGA package

- 14.0 mm x 24.0 mm x 1.95 mm, 145-ball,
 1.0 mm ball pitch, FZJE
- All Devices are RoHS Compliant
 - Current product revision will only support SATA Revision 1.x with host transfer rate of up to 1.5 Gb/s (i.e. SATA 1.5 Gb/s). SATA 3.0 Gb/s refers to SATA Revision 2.x and is planned to be supported by our future product revisions.
 - For management of the Sleep Mode, please refer to "SATA NANDrive Application Design Guide."

Product Description

The GLS85LS1008B / 1016B / 1032B / 1064B Industrial Temperature and Commercial Temperature SATA NANDrive™ devices (referred to as "SATA NANDrive" in this datasheet) are fully integrated solid state drives. They combine an advanced Greenliant NAND controller and 8, 16, 32 or 64 GByte of NAND flash in a multi-chip package. These products are ideal for embedded and portable applications that require smaller form factor and more reliable data storage.

SATA-interface solid state mass storage technology is widely used in portable and industrial computers, settop boxes, multi-functional printers, point-of-sales terminals, video and audio recorders, medical instruments and car infotainment systems.

SATA NANDrive is a single device, solid state drive (SSD) that provides the functionality and compatibility of a complete SATA hard disk drive (HDD) in a 14 mm x 24 mm BGA package for easy, space saving mounting to a system motherboard. These products surpass traditional storage in their small size, security, reliability, ruggedness and low power consumption.

The integrated NAND flash controller with built-in advanced NAND management firmware communicates with the Host through the standard SATA protocol. It does not require any additional or proprietary software such as the Flash File System (FFS) and Memory Technology Driver (MTD).

SATA NANDrive is pre-programmed with a 10-Byte unique serial ID and has the option of programming an additional 10-Byte serial ID for even greater system security.

SATA NANDrive's advanced NAND management technology enhances data reliability and security, improves endurance and accurately estimates the remaining life of the NAND flash devices. This innovative technology combines robust NAND controller hardware error correction capabilities with advanced wear-leveling algorithms and bad block management to significantly extend the life of the product.

SATA NANDrive devices are offered in a 145-ball BGA, 1 mm ball pitch package. Please refer to Figure 3-1 for the pin assignments.

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1.0 GENERAL DESCRIPTION

Each SATA NANDrive contains an integrated SATA NAND flash memory controller and up to eight discrete NAND flash die in a BGA package. Refer to Figure 2-1 for the SATA NANDrive block diagram.

1.1 **Optimized SATA NANDrive**

The heart of SATA NANDrive is the SATA NAND flash memory controller which translates standard SATA signals into flash media data and control signals. The following components contribute to SATA NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates SATA commands into data and control signals required for flash media operation.

Internal Direct Memory Access (DMA)

SATA NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

Power Management Unit (PMU)

The PMU controls the power consumption of SATA NANDrive. The PMU dramatically reduces the power consumption of SATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode. ³⁾

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to ensure SATA NANDrive firmware integrity. For regular power management, the Host must send IDLE_IMMEDIATE command and wait for command ready before powering down SATA NANDrive.

For management of the Sleep Mode, please refer to "SATA NANDrive Application Design Guide."

1.1.4 **Embedded Flash File System**

The embedded flash file system is an integral part of SATA NANDrive. It contains MCU firmware that performs the following tasks:

- Translates host side signals into flash media writes and reads
- 2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media
- 3. Keeps track of data file structures
- 4. Manages system security for the selected protection zones

Error Correction Code (ECC) 1.1.5

High performance is achieved through optimized hardware error detection and correction.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for error reporting. During the product development stage, it is recommended to provide the SCI port on the PCB to aid in design validation.

1.1.7 Multi-tasking Interface

The multi-tasking interface enables fast, sequential write performance by allowing concurrent Read, Program and Erase operations to multiple flash media.

1.2 **SMT Reflow Consideration**

The SATA NANDrive family utilizes standard NAND flash for data storage. Because the high temperature in a surface-mount soldering reflow process may alter the content on NAND flash, it is recommended to program SATA NANDrive after the reflow process.

1.3 Advanced NAND Management

SATA NANDrive's integrated controller uses advanced wear-leveling algorithms to substantially increase the longevity of NAND flash media. Wear caused by data writes is evenly distributed in all or select blocks in the device that prevents "hot spots" in locations that are programmed and erased extensively. This effective wear-leveling technique results in optimized device endurance, enhanced data retention and higher reliability required by long-life applications.



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2.0 FUNCTIONAL BLOCKS

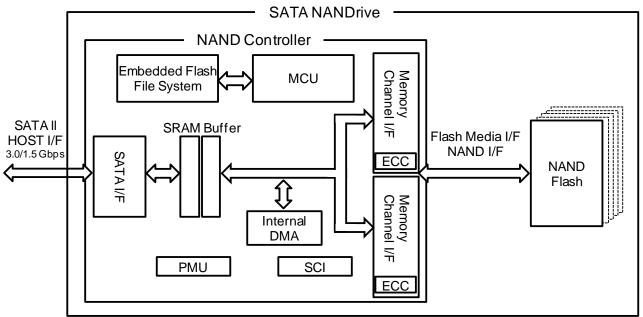


Figure 2-1: SATA NANDrive Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output.

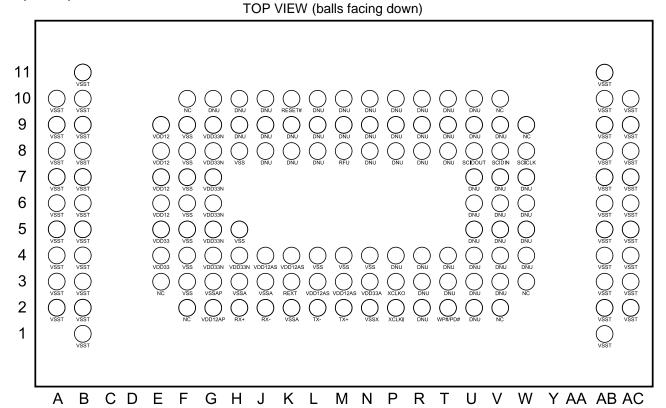


Figure 3-1: Pin Assignments for 145-Ball BGA

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Table 3-1: Din Assianments

Table 3-1: Pin Assignments					
Symbol	Ball No.	Ball Type	IO Type	Name and Functions	
		Host Side I	nterface		
RX+	H2	I	13	Analog Differential Input (+)	
RX-	J2	l	13	Analog Differential Input (-)	
TX+	M2	0	O3	Analog Differential Output (+)	
TX-	L2	0	O3	Analog Differential Output(-)	
0015		Communication	1	. ` ′	
SCIDIN	V8		I2U	SCI port data input	
SCIDOUT	U8	0	01	SCI port data output. No external pull-up or pull-dowr	
CCICI IX	N/O		IOD	resistor should connect to this signal.	
SCICLK	W8	Miscellar	I2D	SCI port clock	
		Wiiscellai	leous		
RFU	M8			Reserved for Future Use	
Rext	K3	I	l3	External Resistor, 1Kohms (1%) connected to GND	
RESET#	K10	I	I2U	This input is the active low hardware reset from host.	
WP#/PD#	T2 ⁴⁾	I	I2U	The WP#/PD# can be used for either the Write Protect mode or Power Down mode, but only one mode is active at any time.	
XCLKI	P2	1	XI	External clock source input for main clock; 25MHz crystal, need external 20pf capacitor to ground	
XCLKO	P3	0	ХО	External clock source output for main clock; 25MHz crystal, need external 20pf capacitor to ground	
NC	E3, F2, F10, V2, V10, W3, W9			No connect	
DNU	G10, H9, H10, J8, J9, J10, K8, K9, L8, L9, L10, M9, M10, N8, N9, N10, P4, P8, P9, P10, R2, R3, R4, R8, R9, R10, T3, T4, T8, T9, T10, U2, U3, U4, U5, U6, U7, U9, U10, V3, V4, V5, V6, V7, V9, W4, W5, W6, W7			Do Not Use. All these pins should not be connected.	
		Power and	Ground		
VDD33	E4, E5	Digital PWR		Supply voltage 3.3V	
VDD33A	N3	Analog PWR			
VDD33N	G4, G5, G6, G7, G8, G9, H4	Digital PWR			
VDD12	E6, E7, E8, E9	Digital PWR		Supply voltage 1.2V	
VDD12AS	J4, K4, L3, M3	Analog PWR		Analog supply voltage 1.2V (200mA max. total for both 1.2V analog power rails, VDD12AS and VDD12AP)	
VDD12AP	G2	Analog PWR		,	
Vss	F3, F4, F5, F6, F7, F8, F9, H5, H8, L4, M4, N4	Digital GND		Digital ground	
VSSX	N2	Analog GND		Analog ground	
VSST	A2, A3, A4, A5, A6, A7, A8, A9, A10, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, AB1, AB2, AB3, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10	GND		Connected to PCB ground plane for thermal dissipation. Not connected to any internal signal.	
VSSA	H3, J3, K2			Analog ground	
VSSAP	G3	Analog GND		Analog ground	
00, 11			1	1	

Table 3-2: I/O Type

Table 3-2. I/O Type		
I/O Type	Description	
13	Analog Input	
O3	Analog Output	
I2D	Input with Pull-down	
I2U	Input with Pull-up	
01	Output	
XI	Crystal Clock Input	
ΧO	Crystal Clock Output	

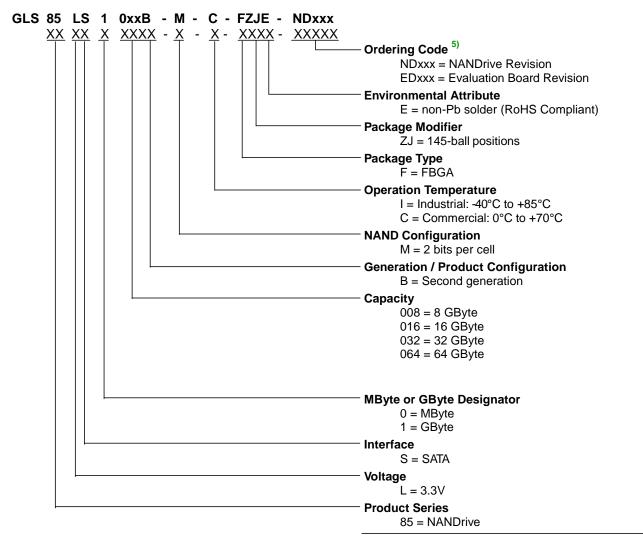
The command to configure the T2 pin in either PD# or WP# is prepared by the vendor-unique command. Please ask your Greenliant contact for details on the SMART command specification.

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4.0 PRODUCT ORDERING INFORMATION



5) Note that the top side marking on the package typically does not include ordering codes (e.g. NDxxx), unless it is a special C-SPEC (custom specification) which is required by the end-customer to be marked on the device.

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Valid Combinations

Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

Table 4-1: SATA NANDrive Product Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Package
8GB	Commercial (0°C to 70°C)	GLS85LS1008B-M-C-FZJE-ND102	FZJE, 14x24x1.95mm
	Industrial (-40°C to 85°C)	GLS85LS1008B-M-I-FZJE-ND102	FZJE, 14x24x1.95mm
16GB	Commercial (0°C to 70°C)	GLS85LS1016B-M-C-FZJE-ND102	FZJE, 14x24x1.95mm
	Industrial (-40°C to 85°C)	GLS85LS1016B-M-I-FZJE-ND102	FZJE, 14x24x1.95mm
32GB	Commercial (0°C to 70°C)	GLS85LS1032B-M-C-FZJE-ND102	FZJE, 14x24x1.95mm
	Industrial (-40°C to 85°C)	GLS85LS1032B-M-I-FZJE-ND102	FZJE, 14x24x1.95mm
64GB	Commercial (0°C to 70°C)	GLS85LS1064B-M-C-FZJE-ND102	FZJE, 14x24x1.95mm
	Industrial (-40°C to 85°C)	GLS85LS1064B-M-I-FZJE-ND102	FZJE, 14x24x1.95mm

Table 4-2: SATA NANDrive Evaluation Board Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Form Factor
8GB	Industrial (-40°C to 85°C)	GLS85LS1008B-M-I-1S-ED102	Module with SATA connector
16GB	Industrial (-40°C to 85°C)	GLS85LS1016B-M-I-1S-ED102	Module with SATA connector
32GB	Industrial (-40°C to 85°C)	GLS85LS1032B-M-I-1S-ED102	Module with SATA connector
64GB	Industrial (-40°C to 85°C)	GLS85LS1064B-M-I-1S-ED102	Module with SATA connector

Table 4-3: SATA NANDrive miniSATA Evaluation Board Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Form Factor
8GB	Industrial (-40°C to 85°C)	GLS85LS1008B-M-I-1MS-ED102	JEDEC MO-300
16GB	Industrial (-40°C to 85°C)	GLS85LS1016B-M-I-1MS-ED102	JEDEC MO-300
32GB	Industrial (-40°C to 85°C)	GLS85LS1032B-M-I-1MS-ED102	JEDEC MO-300
64GB	Industrial (-40°C to 85°C)	GLS85LS1064B-M-I-1MS-ED102	JEDEC MO-300



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4.1 Package Diagram

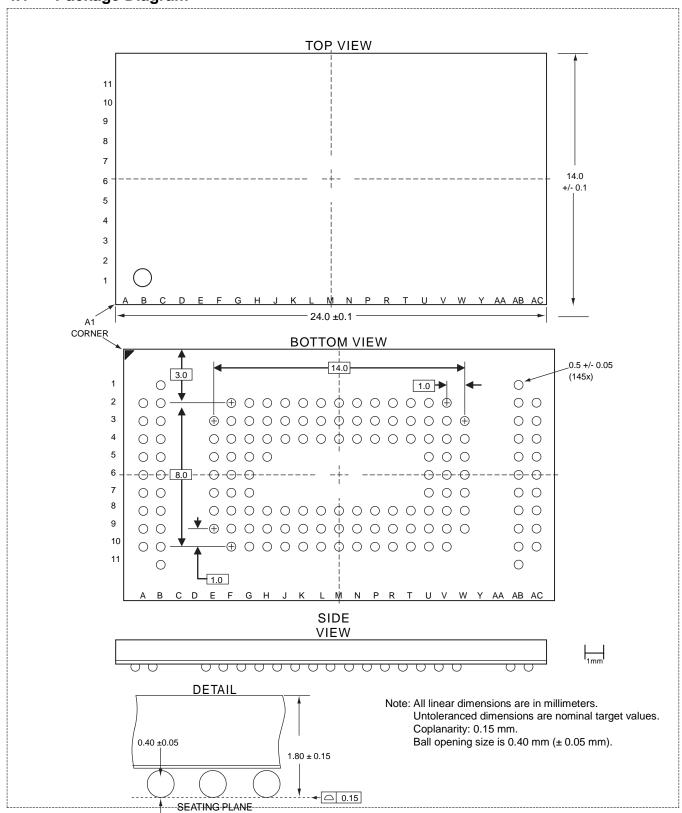


Figure 4-1: SATA NANDrive 145-Ball, Ball Grid Array (BGA) Greenliant Package Code: FZJ

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REVISION HISTORY

Revision	Description	Date
01.000	Initial release of Fact Sheet	April 5, 2012
01.001	Updated Section 1.2	April 26, 2012
01.002	Updated Ordering Information in Section 4.0 Updated IO type of SCICLK in Table3-1	August 16, 2012
02.000	Updated Valid Combinations in Section 4.0	October 25, 2012
02.001	Updated Ordering Information in Section 4.0	November 21, 2012
02.002	Placed Valid Combinations into table format in Section 4.0	February 25, 2013

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