

RoHS Compliant

SATA-Disk Module II

Datasheet for 7P/180D Low Profile

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Version 1.2



Apacer Technology Inc.

4th Fl., 75 Xintai 5th Rd., Sec.1, Hsichih, New Taipei City, Taiwan 221

Tel: +886-2-2698-2888 Fax: +886-2-2698-2889

www.apacer.com

Features:

- **Standard Serial ATA 2.6 (Gen. 2)**
 - Serial ATA 2.6 (Gen. 2)
 - SATA II, 3.0 Gbps
 - ATA-compatible command set
- **Capacities**
 - 512 MB
 - 1, 2, 4 GB
- **Performance**
 - Burst read/write: 300 MB/sec
 - Sustained read: up to 27 MB/sec
 - Sustained write: up to 23 MB/sec
- **Intelligent endurance design**
 - Built-in hardware BCH ECC, correcting 8-bit or 15-bit error per 512-byte data sector
 - Static wear-leveling scheme together with dynamical block allocation to significantly increase the lifetime of a flash device and optimize the disk performance
 - Flash bad-block management
 - S.M.A.R.T.
- **NAND Flash Type: SLC**
- **Data integrity under power-cycling**
 - No battery required for data storage
- **Temperature**
 - 0°C to 70°C for operating
 - -40°C to 100°C for storage
- **Supply voltage**
 - 3.3 V /5 V
- **Low power consumption**
 - Active mode: 230 mA* /165 mA (3.3 V /5 V)
 - Idle mode: 165 mA* /112 mA (3.3 V /5 V)
- **Connector**
 - 7-pin SATA female connector
 - 2-pin SATA power connector
- **RoHS compliant**

*Based on 2 GB model

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1. Product Description

1.1 Introduction

Apacer's SATA Disk Module (SDM) is a solid-state disk (SSD) drive that contains a controller, embedded firmware, and flash media along with a male connector. Using NAND flash memory devices, the SDM drive interfaces with the host allowing data to be seamlessly transferred between the host and the flash devices.

The SDM drive is designed with a single-chip controller, offering capacities of up to four gigabytes and providing full support for the SATA II high-speed interface standard. It can operate at sustained access rates of up to thirty five megabytes per second, which is much faster than any other competitor in the market.

In addition to buffer management through dynamical allocation, the SDM adopts the static wear-leveling scheme to allow uniform use of all storage blocks, ensuring that the lifetime of a flash media can be significantly increased and the disk performance is optimized as well. The SDM provides the S.M.A.R.T. feature complies to the SATA Rev. 2.6, ATA/ATAPI-7 specifications and uses the standard SMART command B0h to read data from the drive. This feature protects the user from unscheduled downtime by monitoring and storing critical drive performance.

1.2 Functional Block Diagram

The SDM drive includes a single-chip SATA II controller and the flash media, as well as the SATA standard interface. The controller integrates the flash management unit with the controller itself to support multi-channel, multi-bank flash arrays. Figure 1-1 shows the functional block diagram.

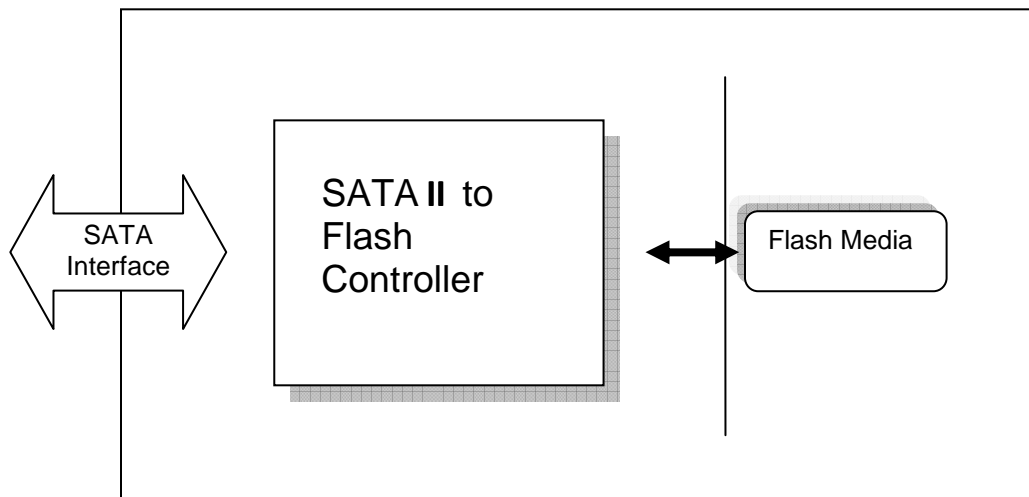


Figure 1-1 Apacer SDM block diagram

1.3 ATA Mode Support

The SDM provides ATA mode support as follows:

- Up to PIO mode-4
- Up to Multiword DMA mode-2
- Up to UDMA mode-5

1.4 Capacity Specification

Capacity specification of the SDM product family is available as shown in Table 1-1. It lists the specific capacity, the default numbers of logical cylinders and heads, and the number of logical sectors per track for each product line.

Table 1-1: Capacity specifications

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
512 MB	487,710,720	945	16	63	952,560
1 GB	992,968,704	1,924	16	63	1,939,392
2 GB	2,002,452,480	3,880	16	63	3,911,040
4 GB	4,021,936,128	7,793	16	63	7,855,344

1.5 Performance

Performance of the SDM is shown in Table 1-2

Table 1-2: Performance

Capacity	512 MB	1 GB	2 GB	4 GB
Performance				
Sustained read (MB/s)	22	27	27	27
Sustained write (MB/s)	8	12	22	23

Note: Performances vary from flash configurations.

1.6 Pin Assignments

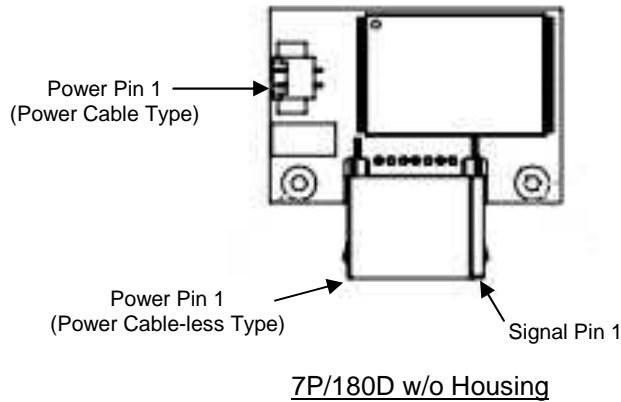


Table 1-3: Signal segment

Name	Type	Description
S1	GND	
S2	RxP	+ Differential Receive Signal
S3	RxN	- Differential Receive Signal
S4	GND	
S5	TxN	- Differential Transmit Signal
S6	TxP	+ Differential Transmit Signal
S7	GND	

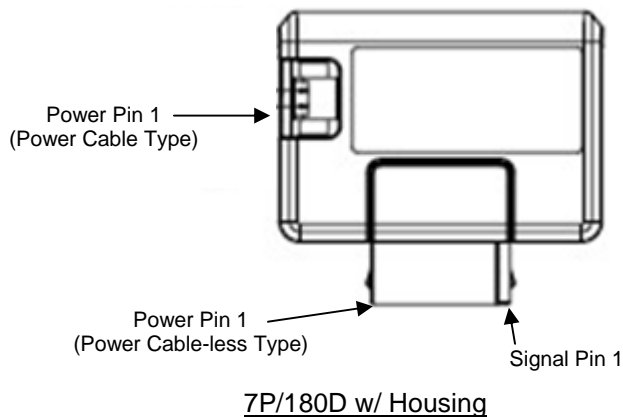


Table 1-4: Power segment

Pin	Signal/Description
P1	VCC (5V)
P2	GND

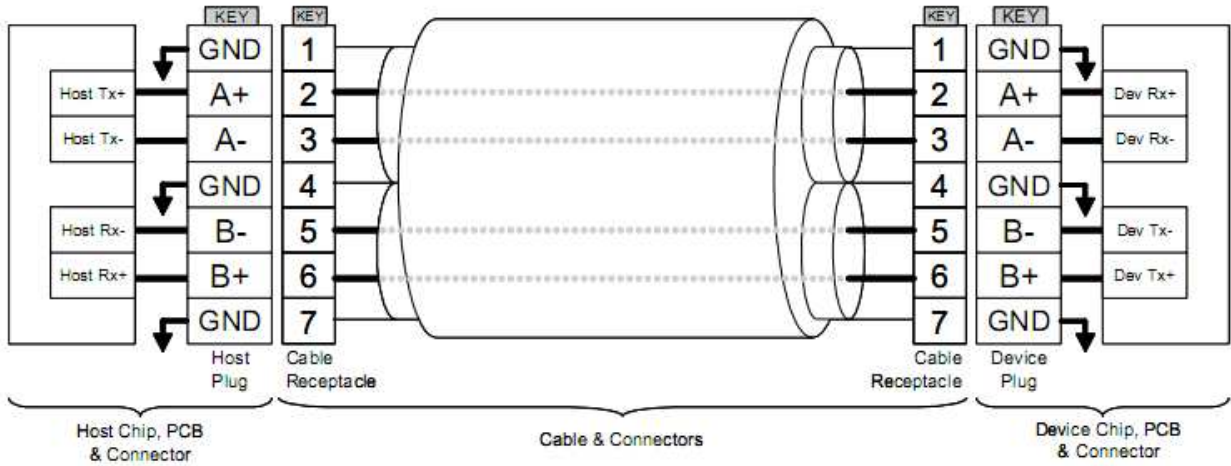


Figure 1-2 SATA Cable/Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

2. Software Interface

2.1 Command Set

Table 2-1 summarizes the ATA commands supported by the SDM.

Table 2-1 Command set

Command Name	Code (Hex)	FR ¹	SC ²	SN ³	CY ⁴	DH ⁵	LBA ⁶
Check-Power-Mode	E5h	-	-	-	-	D ⁸	-
Flush-Cache	E7h	-	-	-	-	D	-
Identify-Drive	ECh	-	-	-	-	D	-
Idle	E3h	-	Y ⁷	-	-	D	-
Idle-Immediate	E1h	-	-	-	-	D	-
Initialize-Drive-Parameters	91h	-	Y	-	-	Y	-
Recalibrate	10h	-	-	-	-	D	-
Read-DMA	C8h	-	Y	Y	Y	Y	Y
Read-Multiple	C4h	-	Y	Y	Y	Y	Y
Read-Sector(s)	20h	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40h	-	Y	Y	Y	Y	Y
SMART	B0h	-	Y	Y	Y	D	Y
Set-Features	EFh	Y	-	-	-	D	-
Set-Multiple-Mode	C6h	-	Y	-	-	D	-
Sleep	E6h	-	-	-	-	D	-
Standby	E2h	-	-	-	-	D	-
Standby-Immediate	E0h	-	-	-	-	D	-
Write-DMA	CAh	-	Y	Y	Y	Y	Y
Write-Multiple	C5h	-	Y	Y	Y	Y	Y
Write-Sector(s)	30h	-	Y	Y	Y	Y	Y

1. FR - Features register
2. SC - Sector Count register
3. SN - Sector Number register
4. CY - Cylinder High/Low registers
5. DH - Drive/Head Number register
6. LBA - Logical Block Address mode supported
7. Y - The register contains a valid parameter for this command.
8. For the Drive/Head register:
 - Y means both the SDM and Head parameters are used;
 - D means only the SDM parameter is valid, and not for the Head parameter.

2.1.1 Check-Power-Mode (98h or E5h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command								98h or E5h

The Check-Power-Mode command verifies the device's current power mode. When the device is configured for Standby mode, or is entering or exiting Standby, the BSY bit will be set and the Sector Count register is set to 00h, and the BSY bit is then cleared. In Idle mode, BSY is set and the Sector Count register is set to FFh, and then the BSY bit is cleared and an interrupt is issued.

2.1.2 Execute-Drive-Diagnostic (90h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command								90h

The Executive-Drive-Diagnostic command performs an internal read/write diagnostic test using AA55h and 55AAh. If an error is detected in the read/write buffer, the Error register will report the appropriate diagnostic code. The diagnostic codes are shown in Table 2-2.

Table 2-2 Diagnostic codes reported upon internal read/write testing

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controlling Microprocessor Error
8Xh	Slave Error

2.1.3 Flush-Cache (E7h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command								E7h

The Flush-Cache command causes an SAFD 253 drive to complete writing data from its cache. The drive then clears BSY and generates an interrupt.

2.1.4 Identify-Drive (ECh)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command								ECh

The Identify-Drive command enables the host to receive parameter information from the SAFD 253. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 2-3. All reserved bits or words are zero.

Table 2-3 Identify-Drive information (1/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
0	0040h	2	General configuration bit
1	xxxxh	2	Default number of cylinders
2	37C8h	2	Specific configuration
3	00xxh	2	Default number of heads
4	0000h	2	Retired
5	0000h	2	Retired
6	xxxxh	2	Default number of sectors per track
7-8	xxxxh	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	000Eh	2	Retired
10-19	xxxxh	20	Serial number (20 ASCII characters)
20	0000h	2	Buffer type
21	0000h	2	Buffer size in 512-byte increments
22	003Fh	2	Reserved
23-26	xxxxh	8	Firmware revision (8 ASCII characters)
27-46	xxxxh	40	Model number (40 ASCII characters)
47	8001h	2	Multiple Count: 15-8: 80h 7-0: 00h = Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on Read/Write Multiple commands
48	4000h	2	Reserved
49	2F00h	2	Capabilities: 15-14: Reserved for the Identify-Packet-Device command 13: 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12: Reserved for the Identify-Packet-Device command 11: 1 = IORDY supported 0 = IORDY may be supported 10: 1 = IORDY may be disabled 9: 1 = LBA supported 8: 1 = DMA supported 7-0: Retired
50	4000h	2	Reserved
51	0280h	2	Obsolete
52	0000h	2	Obsolete
53	0000h	2	Translation Parameters Are Valid: 15-3: Reserved 2: 1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid 1: 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid 0: Obsolete

Table 2-3 Identify-Drive information (2/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
54	xxxxh	2	Current numbers of cylinders
55	xxxxh	2	Current numbers of heads
56	xxxxh	2	Current sectors per track
57-58	xxxxh	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	0001h	2	Multiple Sector Settings: 15-9: Reserved 8: 1 = Multiple sector setting is valid 7-0: xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple commands
60-61	xxxxh	4	Total number of sectors addressable in LBA mode
62	0000h	2	Reserved
63	0007h	2	Multiword DMA Transfer: 15-3: Set as indicated in ATA/ATAPI-6 2: 1= Multiword DMA mode 2 and below are supported 1: 1= Multiword DMA mode 1 and below are supported
64	0003h	2	PIO Transfer mode supported
65	0078h	2	Minimum multiword DMA transfer cycle time per word: 15-0 cycle time in nanoseconds
66	0078h	2	Manufacturer's recommended multiword DMA transfer cycle time: 15-0 cycle time in nanoseconds
67	0078h	2	Minimum PIO transfer cycle time without flow control: 15-0 cycle time in nanoseconds
68	0078h	2	Minimum PIO transfer cycle time with IORDY flow control: 15-0 cycle time in nanoseconds
69-70	0000h	2	Reserved (for future command overlap and queuing)
71-74	0000h	8	Reserved for the Identify-Packet-Device command
75	0000h	2	Queue Depth: 15-5: Reserved 4-0: Maximum queue depth - 1
76	0606h	2	Serial ATA Capabilities: 15-11: Reserved 10: Supports Phy event counters 9: Supports receipt of host-initiated interface power management requests 8: Supports Native Command Queuing 7-3: Reserved for future Serial ATA signaling speed grades 2: 1 = Supports Serial ATA Gen2 signaling speed (3.0 Gbps) 1: 1 = Supports Serial ATA Gen1 signaling speed (1.5 Gbps) 0: Shall be cleared to zero
77	0000h	2	Reserved for future Serial ATA definition

Table 2-3 Identify-Drive information (3/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
78	0000h	2	Serial ATA Features Supported: 15-7: Reserved 6: 1 = Supports software settings preservation 5: Reserved 4: 1 = Supports in-order data delivery 3: 1 = Device supports initiating interface power management 2: 1 = Supports DMA Setup Auto-Activate optimization 1: 1 = Supports non-zero buffer offsets in DMA Setup FIS 0: Shall be cleared to zero
79	0000h	2	Serial ATA Features Enabled: 15-7: Reserved 6: 1 = Software settings preservation enabled 5: Reserved 4: 1 = In-order data delivery enabled 3: 1 = Device initiating interface power management enabled 2: 1 = DMA Setup Auto-Activate optimization enabled 1: 1 = Non-zero buffer offsets in DMA Setup FIS enabled 0: Shall be cleared to zero
80	01FEh	2	Major Version Number: (0000h or FFFFh = Drive does not report version) 15: Reserved 14: Reserved for ATA/ATAPI-14 13: Reserved for ATA/ATAPI-13 12: Reserved for ATA/ATAPI-12 11: Reserved for ATA/ATAPI-11 10: Reserved for ATA/ATAPI-10 9: Reserved for ATA/ATAPI-9 8: Reserved for ATA/ATAPI-8 7: Reserved for ATA/ATAPI-7 6: 1 = Supports ATA/ATAPI-6 5: 1 = Supports ATA/ATAPI-5 4: 1 = Supports ATA/ATAPI-4 3: 1 = Supports ATA-3 2: Obsolete 1: Obsolete 0: Reserved
81	0021h	2	Minor version number

Table 2-3 Identify-Drive information (4/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
82	0069h	2	Command Set Supported: 15: Obsolete 14: 1 = NOP command supported 13: 1 = Read-Buffer command supported 12: 1 = Write-Buffer command supported 11: Obsolete 10: 1 = Host Protected Area feature set supported 9: 1 = Device-Reset command supported 8: 1 = Service interrupt supported 7: 1 = Release interrupt supported 6: 1 = Look-ahead supported 5: 1 = Write cache supported 4: Shall be cleared to zero to indicate that the Packet command feature set is not supported 3: 1 = Mandatory Power Management feature set supported 2: 1 = Removable Media feature set supported 1: 1 = Security Mode feature set supported 0: 1 = SMART feature set supported
83	5001h	2	Command Sets Supported: 15: Shall be cleared to zero 14: Shall be set to one 13: 1 = Flush-Cache-Ext command supported 12: 1 = Mandatory Flush-Cache command supported 11: 1 = Device Configuration Overlay feature set supported 10: 1 = 48-bit Address feature set supported 9: 1 = Automatic Acoustic Management feature set supported 8: 1 = SET MAX security extension supported 7: See Address Offset Reserved Area Boot, INCITS TR27: 2001 6: 1 = Set-Features subcommand to spin up upon power-up 5: 1 = Power-up in Standby feature set supported 4: 1 = Removable Media Status Notification feature set supported 3: 1 = Advanced Power Management feature set supported 2: 1 = CFA feature set supported 1: 1 = Read/Write DMA Queued supported 0: 1 = Download-Microcode command supported

Table 2-3 Identify-Drive information (5/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
84	4000h	2	Command Set/Feature Supported Extension: 15: Shall be cleared to zero 14: Shall be set to one 13-6: Reserved 5: 1 = General Purpose Logging feature set supported 4: Reserved 3: 1 = Media Card Pass Through Command feature set supported 2: 1 = Media serial number supported 1: 1 = SMART self-test supported 0: 1 = SMART error-logging supported
85	0029h	2	Command Set/Feature Enabled: 15: Obsolete 14: 1 = NOP command enabled 13: 1 = Read-Buffer command enabled 12: 1 = Write-Buffer command enabled 11: Obsolete 10: 1 = Host Protected Area feature set enabled 9: 1 = Device-Reset command enabled 8: 1 = Service interrupt enabled 7: 1 = Release interrupt enabled 6: 1 = Look-ahead enabled 5: 1 = Write cache enabled 4: Shall be cleared to zero to indicate that the Packet Command feature set is not supported 3: 1 = Power Management feature set enabled 2: 1 = Removable Media feature set enabled 1: 1 = Security Mode feature set enabled 0: 1 = SMART feature set enabled

Table 2-3 Identify-Drive information (6/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
86	5000h	2	Command Sets Supported: 15: Shall be cleared to zero 14: Shall be set to one 13: 1 = Flush-Cache-Ext command supported 12: 1 = Mandatory Flush-Cache command supported 11: 1 = Device Configuration Overlay feature set supported 10: 1 = 48-bit Address feature set supported 9: 1 = Automatic Acoustic Management feature set supported 8: 1 = Set Max security extension supported 7: See Address Offset Reserved Area Boot, NCITS TR27: 2001 6: 1 = Set-Features subcommand to spin up upon power-up 5: 1 = Power-up in Standby feature set supported 4: 1 = Removable Media Status Notification feature set supported 3: 1 = Advanced Power Management feature set supported 2: 1 = CFA feature set supported 1: 1 = Read/Write DMA Queued supported 0: 1 = Download-Microcode command supported
87	4000h	2	Command Set/Feature Supported Extension: 15: Shall be cleared to zero 14: Shall be set to one 13-6: Reserved 5: 1 = General Purpose Logging feature set supported 4: Reserved 3: 1 = Media Card Pass Through Command feature set supported 2: 1 = Media serial number supported 1: 1 = SMART self-test supported 0: 1 = SMART error-logging supported

Table 2-3 Identify-Drive information (7/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
88	203Fh	2	Ultra DMA Modes: 15: Reserved 14: 1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected 13: 1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected 12: 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected 11: 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected 10: 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected 9: 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected 8: 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected 7: Reserved 6: 1 = Ultra DMA mode 6 and below are supported 5: 1 = Ultra DMA mode 5 and below are supported 4: 1 = Ultra DMA mode 4 and below are supported 3: 1 = Ultra DMA mode 3 and below are supported 2: 1 = Ultra DMA mode 2 and below are supported 1: 1 = Ultra DMA mode 1 and below are supported 0: 1 = Ultra DMA mode 0 is supported

Table 2-3 Identify-Drive information (8/8)

Word Address	Default Value	Total Bytes	Data Field Type Information
89	xxxxh	2	Time required for security erase unit completion
90	xxxxh	2	Time required for enhanced security erase unit completion
91	0000h	2	Current advanced power management value
92	0000h	2	Master Password Revision Code
93	0000h	2	Hardware reset result
94	80FEh	2	15-8: Vendor's recommended acoustic management value 7-0: Current automatic acoustic management value
95-99	0000h	10	Reserved
100-103	xxxxh	8	Maximum user LBA for 48-bit Address feature set.
104-126	0000h	46	Reserved
127	0000h	2	Removable Media Status Notification feature set support
128	0000h	2	Security status
129-159	0000h	62	Vendor unique bytes
160	0000h	2	CFA Power mode 1
161-175	0000h	30	Reserved for assignment by the CompactFlash™ Association
176-205	0000h	60	Current media serial number
206-254	0000h	98	Reserved
255	xxxxh	2	Integrity Word: 15-8: Checksum 7-0: Signature

Note: The default value specified by xxxx means it depends on the device configuration.

2.1.5 Idle (97h or E3h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count	Timer Count (5 ms increments)							
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X		Drive			X	
Command	97h or E3h							

The Idle command causes the SAFD 253 to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the Automatic Power-down mode is enabled. If the sector count is zero, the Automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 ms) is different from the ATA/SATA specification.

2.1.6 Idle-Immediate (95h or E1h)

Register	7	6	5	4	3	2	1	0	
Features					X				
Sector Count					X				
Sector Number (LBA Low)					X				
Cylinder Low (LBA Mid)					X				
Cylinder High (LBA High)					X				
Device	X			Drive	X				
Command	95h or E1h								

The Idle-Immediate command causes the SAFD 253 to set BSY, enter the idle mode, clear BSY, and generate an interrupt.

2.1.7 Initialize-Drive-Parameters (91h)

Register	7	6	5	4	3	2	1	0	
Features					X				
Sector Count	Number of sectors								
Sector Number (LBA Low)					X				
Cylinder Low (LBA Mid)					X				
Cylinder High (LBA High)					X				
Device	X	0	X	Drive	Max Head				
Command	91h								

The Initialize-Drive-Parameters command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

2.1.8 Recalibrate (10h)

Register	7	6	5	4	3	2	1	0	
Features					X				
Sector Count					X				
Sector Number (LBA Low)					X				
Cylinder Low (LBA Mid)					X				
Cylinder High (LBA High)					X				
Device	1	LBA	1	Drive	X				
Command	10h								

The Recalibrate command is effectively a no-operation and is provided for the compatibility purpose.

2.1.9 Read-DMA (C8h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	C8h							

The Read-DMA command allows the host to read data using the DMA transfer protocol. This command executes in a similar manner to the Read-Sector(s) command except for the following:

- The host initializes the DMA channel prior to issuing the command
- Data transfers are qualified by DMARQ and are performed by the DMA channel
- The ATA flash-disk controller issues only one interrupt per command to indicate that data transfer has terminated and status is available.

2.1.10 Read-Multiple (C4h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	C4h							

The Read-Multiple command executes similarly to the Read-Sector command with the exception that interrupts are issued only when a block containing the counts of sectors defined by the Set-Multiple command is transferred.

2.1.11 Read-Sector(s) (20h or 21h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	20h or 21h							

The Read-Sector(s) command allows the host to read from 1 to 256 sectors as specified in the Sector Count register. If the Sector Count register is set to "0h", 256 sectors of data will be made available. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the SAFD 253 sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads 512 bytes of data from the buffer. At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

2.1.12 Read-Verify-Sector(s) (40h or 41h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	40h or 41h							

The Read-Verify-Sector(s) command operates similarly to the Read-Sector(s) command, with the exception that it does not set the DRQ bit and does not transfer data to the host. Once the requested sectors have been verified, the onboard controller clears the BSY bit and issues an interrupt.

2.1.13 Set-Features (EFh)

Register	7	6	5	4	3	2	1	0
Features	Feature							
Sector Count	X							
Sector Number (LBA Low)	X							
Cylinder Low (LBA Mid)	X							
Cylinder High (LBA High)	X							
Device	X			Drive	X			
Command	EFh							

The Set-Features command is used by the host to establish or select certain features. The Features register defines all features that are supported, as listed in Table 2-4.

Table 2-4 Features supported

Feature	Operation
01h	Enable 8-bit data transfers
02h	Enable Write Cache
03h	Set transfer mode based on value in Sector Count register
09h	Enable Extended Power Operations
55h	Disable Read Look Ahead
66h	Disable Power-on Reset (POR) establishment of defaults at software reset
69h	NOP - Accepted for backward compatibility
81h	Disable 8-bit data transfer
82h	Disable Write Cache
89h	Disable Extended Power operations
96h	NOP - Accepted for backward compatibility
97h	Accepted for backward compatibility. Use of this feature is not recommended
AAh	Enable Read-Look-Ahead
CCh	Enable Power-on Reset (POR) establishment of defaults at software reset

Note that feature 03h allows the host to select the transfer mode by specifying a value in the Sector Count register. These bits are further defined as shown in Table 2-5.

Table 2-5 Values available in Transfer mode

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode1
Multi-word DMA mode	00100b	mode1
Ultra-DMA mode	01000b	mode1
Reserved	Other	n/a

The upper 5 bits define the type of transfer, and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

2.1.14 Set-Multiple-Mode (C6h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	X							
Cylinder Low (LBA Mid)	X							
Cylinder High (LBA High)	X							
Device	X			Drive	X			
Command	C6h							

The Set-Multiple-Mode command allows the host to access the drive via Read-Multiple and Write-Multiple ATA commands. Additionally, the command sets the block count (i.e., the number of sectors within the block) for the Read/Write Multiple commands. The sector count per block is set in the Sector Count register.

2.1.15 Set-Sleep-Mode (99h or E6h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command	99h or E6h							

The Set-Sleep-Mode command allows the host to set the device in Sleep mode. When the onboard controller transitions to the Sleep mode, it clears the BSY bit and issues an interrupt, and the device interface becomes inactive. The Sleep mode can be exited by issuing either a hardware or software reset.

2.1.16 Standby (96h or E2h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command	96h or E2h							

The Standby command, when issued by the host, will transition the device into the Standby mode. If the Sector Count Register is set to a value other than "0h", the Auto Power-down function is enabled and the device will return to the Idle mode.

2.1.17 Standby-Immediate (94h or E0h)

Register	7	6	5	4	3	2	1	0
Features					X			
Sector Count					X			
Sector Number (LBA Low)					X			
Cylinder Low (LBA Mid)					X			
Cylinder High (LBA High)					X			
Device		X			Drive		X	
Command	94h or E0h							

The Standby-Immediate command, when issued by the host, will transition the device into the Standby mode.

2.1.18 Write-DMA (CAh)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	CAh							

This Write-DMA command allows the host to write data using the DMA transfer protocol. This command executes in a similar manner to Write-Sector(s) except for the following:

- The host initializes the DMA channel prior to issuing the command;
- Data transfers are qualified by DMARQ and are performed by the DMA channel;
- The ATA flash-disk controller issues only one interrupt per command to indicate that data transfer has terminated and status is available.

2.1.19 Write-Multiple (C5h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	C5h							

The Write-Multiple command operates in the same manner as the Write-Sector command. When it was issued, the device will set the BSY bit within 400 nsec, and an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

2.1.20 Write-Sector(s) (30h or 31h)

Register	7	6	5	4	3	2	1	0
Features	X							
Sector Count	Sector Count							
Sector Number (LBA Low)	Sector Number (LBA 7-0)							
Cylinder Low (LBA Mid)	Cylinder Low (LBA 15-8)							
Cylinder High (LBA High)	Cylinder High (LBA 27-24)							
Device	1	LBA	1	Drive	Head (LBA 27-24)			
Command	30h or 31h							

This Write-Sector(s) command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. When it is issued, the device will set the BSY bit within 400 nsec, and an interrupt is generated at the completion of a transferred block of sectors. The DRQ bit is set at the beginning of a block transfer.

2.1.21 SMART (B0h)

SMART Read Data

COMMAND CODE – B0h

SUBCOMMAND – D0h (To read SMART data, including attribute ID, attribute value, worst value, and raw data)

PROTOCOL – PIO data in

INPUTS

The Features register shall be set to D0h. The LBA Mid register shall be set to 4Fh. The LBA High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	na							
LBA Low	na							
LBA Mid	4Fh							
LBA High	C2h							
Device	1	na	1	DEV	na	na	na	na
Command	B0h							

NORMAL OUTPUTS

If this command succeeds, SAFD will return 512 bytes of data and normal status; otherwise, SAFD will return error status.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Device register

DEV indicates the selected device

Status register

BSY shall be cleared to zero

DRDY shall be set to one

DF (Device Fault) shall be cleared to zero

DRQ shall be cleared to zero

ERR shall be cleared to zero

ERROR OUTPUTS

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
LBA Low	na							
LBA Mid	na							
LBA High	na							
Device	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV indicates the selected device

Status register

BSY shall be cleared to zero

DRDY shall be set to one

DF (Device Fault) shall be cleared to zero

DRQ shall be cleared to zero

ERR shall be cleared to zero

DATA DESCRIPTION

SAFD will return 512 bytes of data defined in Table 2-6.

Table 2-6 Device attributes data structure (512 bytes)

Bytes	Format	Type	Description
2	binary	Read-only	Data structure revision = 0001 for this spec
12	(Table 2-9)	Read/Write	1st individual attribute data
...			...
12	(Table 2-9)	Read/Write	30th individual attribute data
1	(Refer to SFF-8035i)	Read-only	Off-line data collection status
1			Vendor-specific
2	(Refer to SFF-8035i)		Total time in seconds to complete off-line data collection activity
1			Vendor specific
1	(Refer to SFF-8035i)		Off-line data collection capability
2	(Refer to SFF-8035i)		S.M.A.R.T. capability
16			Reserved (00h)
125			Vendor-specific
1		Read-only	Data structure checksum
512			Total bytes

Currently, SAFD253 defines two versions of SMART specification. First, implemented attribute ID is defined as shown in Table 2-7 and Table 2-8.

Table 2-7 Individual attribute data structure (12 bytes per attribute)

Bytes	Parameter	Description
1	Attribute ID	01h to FFh (E5h, E8h~EFh, and F3h are defined in SAFD 253 version SFDAXx1A) – refer to Table 2-10
2	Status flag	0002h
1	Attribute value	64h
8	Vendor-specific	

Table 2-8 Implemented Attribute ID

ID (Hex)	Description
E5	Flash ID
E8	Die variable of Bank 0, Die 0
E9	Die variable of Bank 0, Die 1
EA	Die variable of Bank 1, Die 0
EB	Die variable of Bank 1, Die 1
EC	Die variable of Bank 2, Die 0
ED	Die variable of Bank 2, Die 1
EE	Die variable of Bank 3, Die 0
EF	Die variable of Bank 3, Die 1
F3	Firmware version information
F4	Overbit
F5	Die variable of Bank 4, Die 0
F6	Die variable of Bank 4, Die 1
F7	Die variable of Bank 5, Die 0
F8	Die variable of Bank 5, Die 1
F9	Die variable of Bank 6, Die 0
FB	Die variable of Bank 6, Die 1
FC	Die variable of Bank 7, Die 0
FD	Die variable of Bank 7, Die 1

Flash ID

- Attribute name: Flash ID
- Attribute ID: E5h
- Attribute meaning: Return the Flash ID (up to 8 bytes). Refer to Table 2-9.

Table 2-9 Attribute meaning of the Flash ID

Byte	Description
0	Reserved
1	Flash ID (Byte 1)
2	Flash ID (Byte 2)
3	Flash ID (Byte 3)
4	Flash ID (Byte 4)
5	Flash ID (Byte 5)
6	Flash ID (Byte 6)
7	Flash ID (Byte 7)

Firmware Version Information

- Attribute name: Firmware version information
- Attribute ID: F3h
- Attribute meaning: Return the Firmware version information (up to 8 bytes). Refer to Table 2-10.

Table 2-10 Attribute meaning of the Firmware version information

Byte	Description
0	Not to be disclosed
1	Not to be disclosed
2	Not to be disclosed
3	Not to be disclosed
4	Not to be disclosed
5	Not to be disclosed
6	Channel number
7	Bank number

Die Variable

- Attribute name: Die Variable of Bank N and Die M
- Attribute ID: For various bands and die, the attribute IDs may be E8h-EFh, F5h~F9h and FBh-FDh
- Attribute meaning: Return the average erase count, maximum erase count, average good block count and free list count. Refer to Table 2-11.

Table 2-11 Attribute meaning of the Die Variable

Byte	Description
0	Average Erase Count (bit 8~15)
1	Average Erase Count (bit 0~7)
2	Max Erase Count (bit 8~15)
3	Max Erase Count (bit 0~7)
4	Average Good Block Count (bit 8~15)
5	Average Good Block Count (bit 0~7)
6	Average Free List Count (bit 8~15)
7	Average Free List Count (bit 0~7)

Secondly, implemented attribute ID is defined in Table 2-12 and Table 2-13.

Table 2-12 Individual attribute data structure (12 bytes per attribute)

Bytes	Parameter	Description
1	Attribute ID	01h to FFh (E5h, E8h, EAh, and EBh are defined in SAFD 253 version SFDAXx1B and later) – refer to Table 2-15
2	Status flag	0002h
1	Attribute value	64h
8	Vendor-specific	

Table 2-13 Implemented Attribute ID

ID (Hex)	Description
E5	Flash ID
E8	Firmware version information
EA	Average Erase Count and Maximum Erase Count
EB	Good Block Count and Spare Block Count

Flash ID

- Attribute name: Flash ID
- Attribute ID: E5h
- Attribute meaning: Return the Flash ID (up to 7 bytes). Refer to Table 2-14.

Table 2-14 Attribute meaning of the Flash ID

Byte	Description
0	Reserved
1	Flash ID (Byte 1)
2	Flash ID (Byte 2)
3	Flash ID (Byte 3)
4	Flash ID (Byte 4)
5	Flash ID (Byte 5)
6	Flash ID (Byte 6)
7	Flash ID (Byte 7)

Firmware Version Information

- Attribute name: Firmware version information
- Attribute ID: E8h
- Attribute meaning: Return the Firmware version information (up to 8 bytes). Refer to Table 2-15.

Table 2-15 Attribute meaning of the Firmware version information

Byte	Description
0	Not to be disclosed
1	Not to be disclosed
2	Not to be disclosed
3	Not to be disclosed
4	Not to be disclosed
5	Not to be disclosed
6	Channel number
7	Bank number

Average Erase Count and Maximum Erase Count

- Attribute name: Average Erase Count and Maximum Erase Count
- Attribute ID: E8h
- Attribute meaning: Return the average erase count and maximum erase count. Refer to Table 2-16.

Table 2-16 Attribute meaning of the Average/Max Erase Count

Byte	Description
0	Average Erase Count (bit 16~19)
1	Average Erase Count (bit 8~15)
2	Average Erase Count (bit 0~7)
3	Max Erase Count (bit 16~19)
4	Max Erase Count (bit 8~15)
5	Max Erase Count (bit 0~7)
6	Reserved
7	Reserved

Good Block Count and Spare Block Count

- Attribute name: Good Block Count and Spare Block Count
- Attribute ID: E8h
- Attribute meaning: Return the good block count and the spare block count. Refer to Table 2-17.

Table 2-17 Attribute meaning of the Good Block Count and Spare Block Count

Byte	Description
0	Good Block Count (bit 16~19)
1	Good Block Count (bit 8~15)
2	Good Block Count (bit 0~7)
3	Spare Block Count (bit 8~15)
4	Spare Block Count (bit 0~7)
5	Reserved
6	Reserved
7	Reserved

3. Flash Management

3.1 Error Correction/Detection

The SDM implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 8 bits or 15 bits error in 512 bytes.

3.2 Bad Block Management

Although bad blocks on the flash media are already identified by the flash manufacturer, they can also be accumulated over time during operation. The SDM's controller maintains a table that lists those normal blocks with disk data, the free blocks for wear leveling, and bad blocks with errors. When a normal block is detected broken, it is replaced with a free block and listed as a bad block. When a free block is detected broken, it is then removed from the free block list and marked as a bad block.

During device operation, this ensures that newly accumulated bad blocks are transparent to the host. The device will stop file write service once there are only two free blocks left such that the read function is still available for copying the files from the disk into another.

3.3 Wear Leveling

The NAND flash devices are limited by a certain number of write cycles. When using a FAT-based file system, frequent FAT table updates are required. If some area on the flash wears out faster than others, it would significantly reduce the lifetime of the whole SSD, even if the erase counts of others are far from the write cycle limit. Thus, if the write cycles can be distributed evenly across the media, the lifetime of the media can be prolonged significantly. This scheme is called wear leveling.

Apacer's wear-leveling scheme is achieved both via buffer management and Apacer-specific static wear leveling. They both ensure that the lifetime of the flash media can be increased, and the disk access performance is optimized as well.

3.4 Power Failure Management

The Low Power Detection on the controller initiates crucial data saving before the power supplied to the device is too low. This feature prevents the device from crash and ensures data integrity during an unexpected power-off.

3.5 S.M.A.R.T.

S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology, an open standard allowing disk drives to automatically monitor their own health and report potential problems. It protects the user from unscheduled downtime by monitoring and storing critical drive performance and calibration parameters. Ideally, this should allow taking proactive actions to prevent impending drive failure.

Apacer SDM uses the standard SMART command B0h to read data from the drive for SMART feature as the SATA Rev. 2.6 ATA/ATAPI-7 specifications. Based on the SFF-8035i Rev. 2.0 specifications, Apacer SMART defines 3 vendor-specified SMART Attribute IDs (E5h, EAh-EBh, and E8h) in the SDM. They represent Flash ID, maximum erase count, average erase count, good block count, free-list block count, and firmware version information. When the Apacer SMART Utility running on the host, it analyzes and reports the disk status to the host before the SDM is in critical condition.

4. Environmental Specifications

4.1 Environments

The SDM environmental specifications follow the US Military Standard MIL-STD-810F, as shown in Table 4-1.

Table 4-1 SDM environmental specifications (plan)

Environment	Specification
Temperature	0°C to 70°C (Operating)
	-40°C to 100°C (Non-operating)
Humidity	5% to 95% RH (Non-condensing)
Vibration	Sine wave: 5~55~5 Hz (X, Y, Z) Random: 10-2000 Hz, 16.3 G (X, Y, Z)
Shock	Acceleration: 1,500 G, 0.5 ms Peak acceleration: 50 G, 11 ms

5. Electrical Specification

Caution: Absolute Maximum Stress Ratings – (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Table 5-1: Operating voltage

Ambient Temperature	3.3V	5V
0°C to 70°C	3.135-3.465V	4.75-5.25V

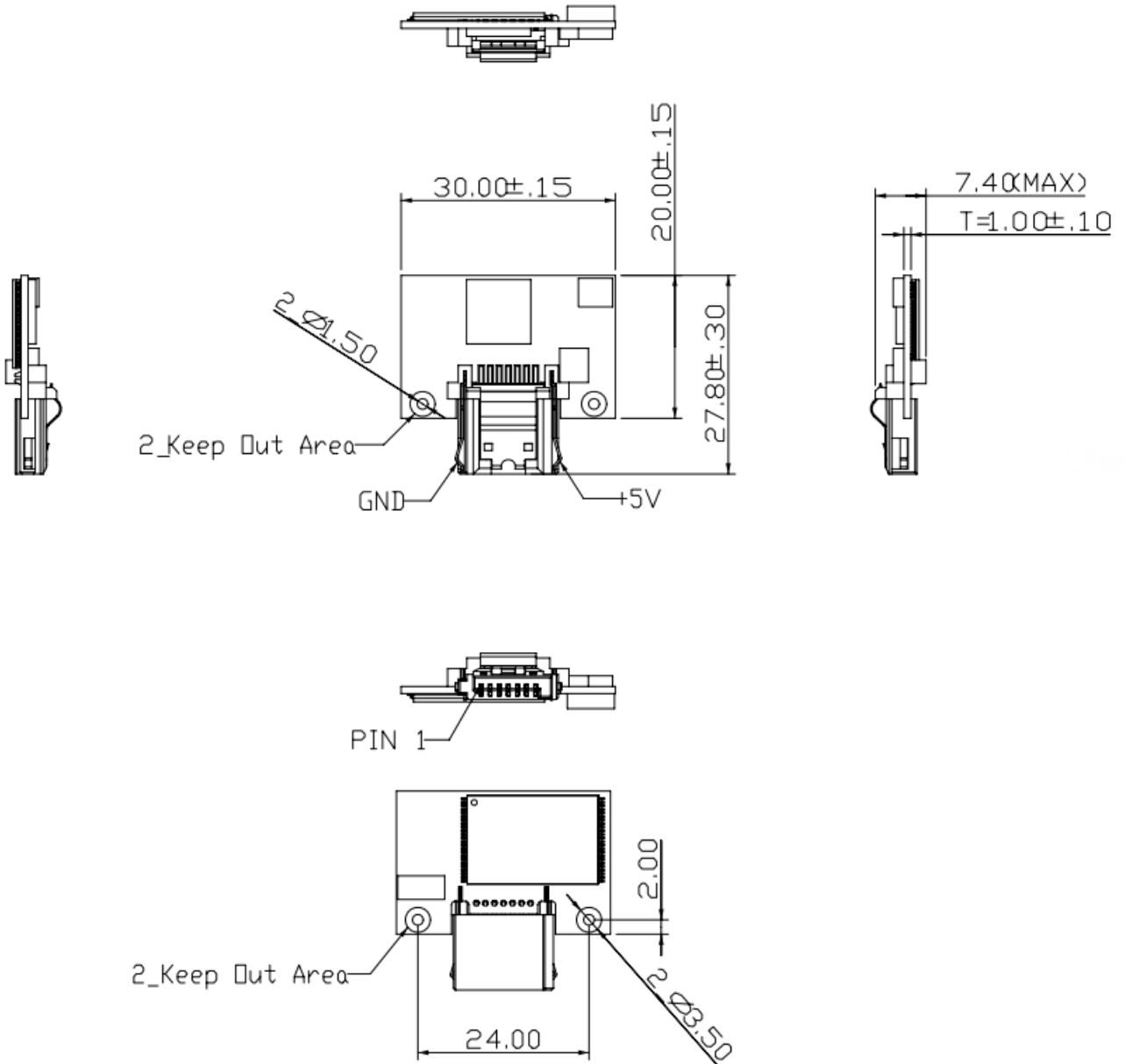
Table 5-2: Absolute maximum power pin stress ratings

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min. to 6.5V max.
Voltage on any pin except V_{DD} with respect to GND	V	-0.5V min. to $V_{DD} + 0.5V$ max.

6. Physical Characteristics

6.1 Power Cable-less Type

6.1.1 W/O Housing (Refer to SDM Power Cable-less Design Guide)

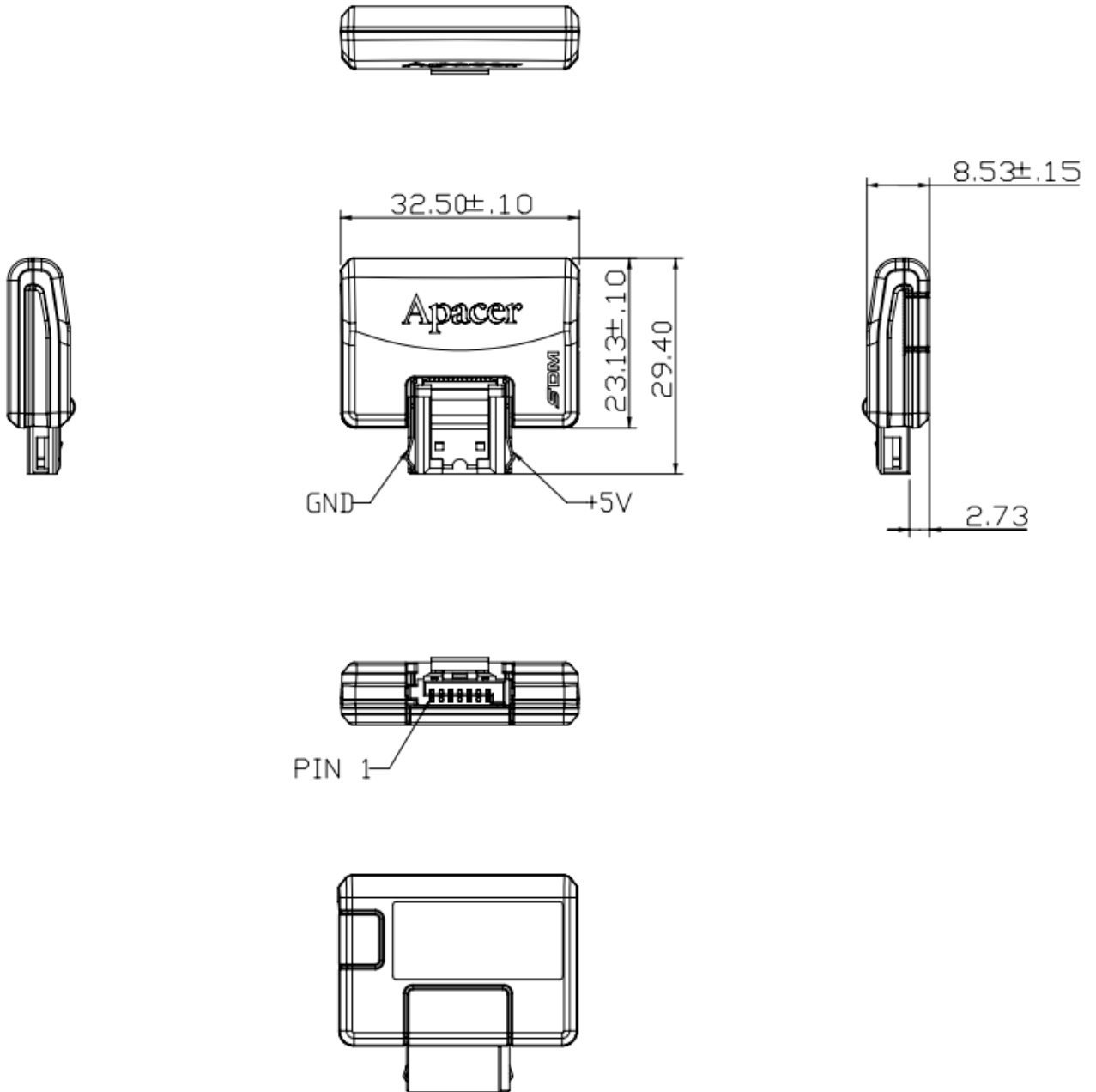


Unit: mm
 Tolerance: ± 0.25

SATA-Disk Module II AP-SDMxxxxXPANS-HTX



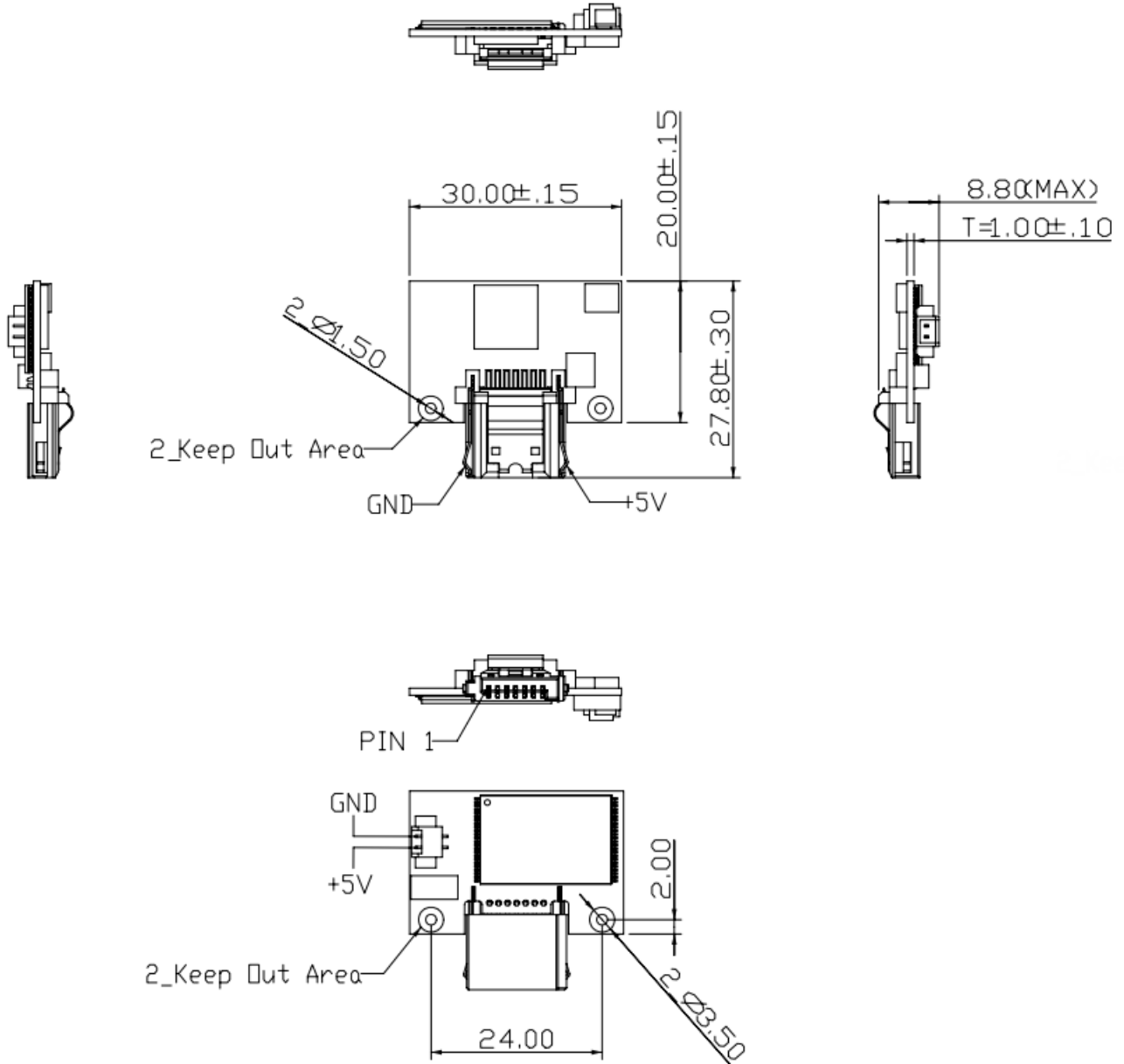
6.1.2 W/Housing (Refer to SDM Power Cable-less Design Guide)



Unit: mm
Tolerance: ± 0.25

6.2 Power Cable Type

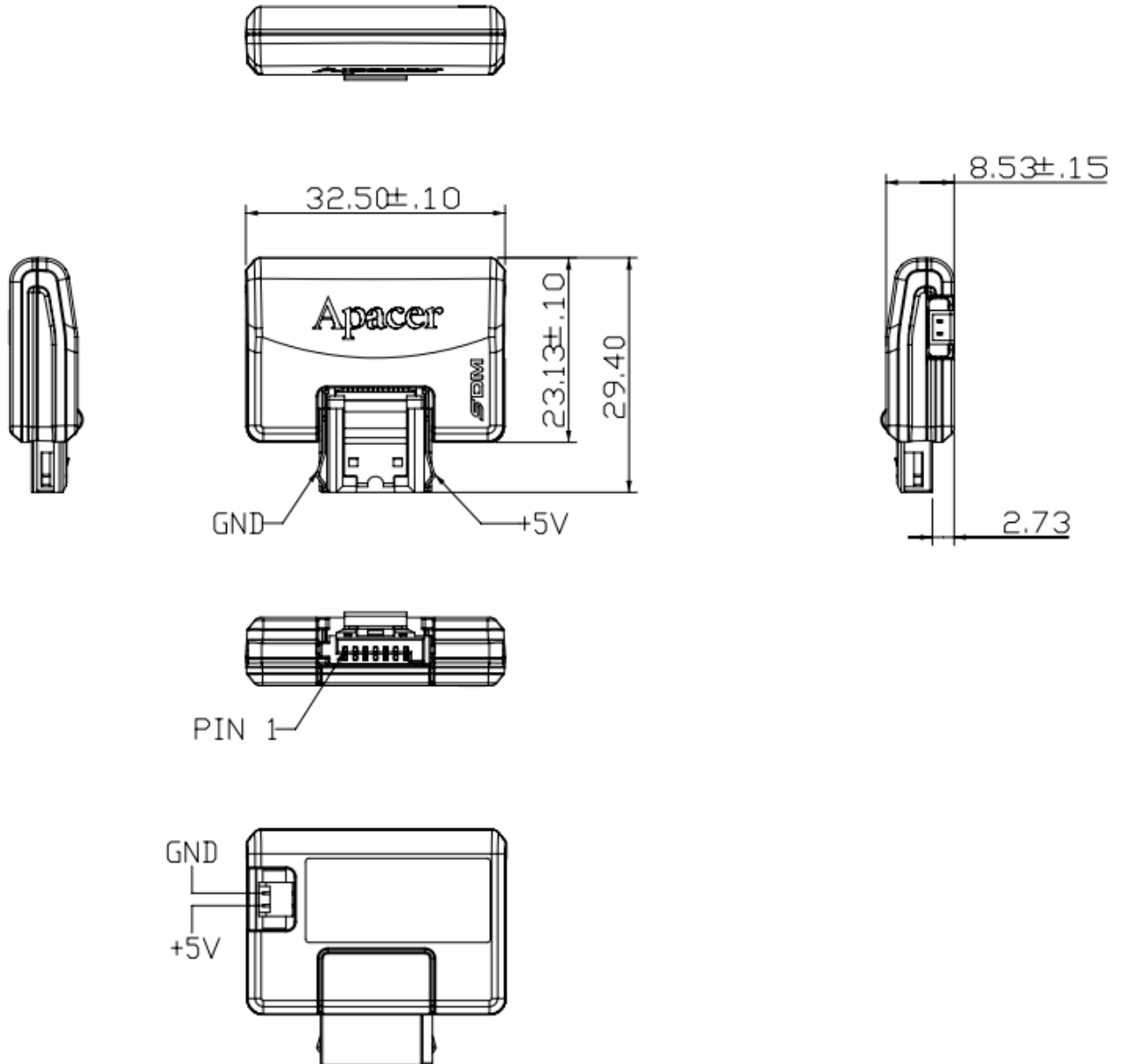
6.2.1 W/O Housing



Unit: mm
 Tolerance: ± 0.25

SATA-Disk Module II
AP-SDMxxxxXPANS-HTX

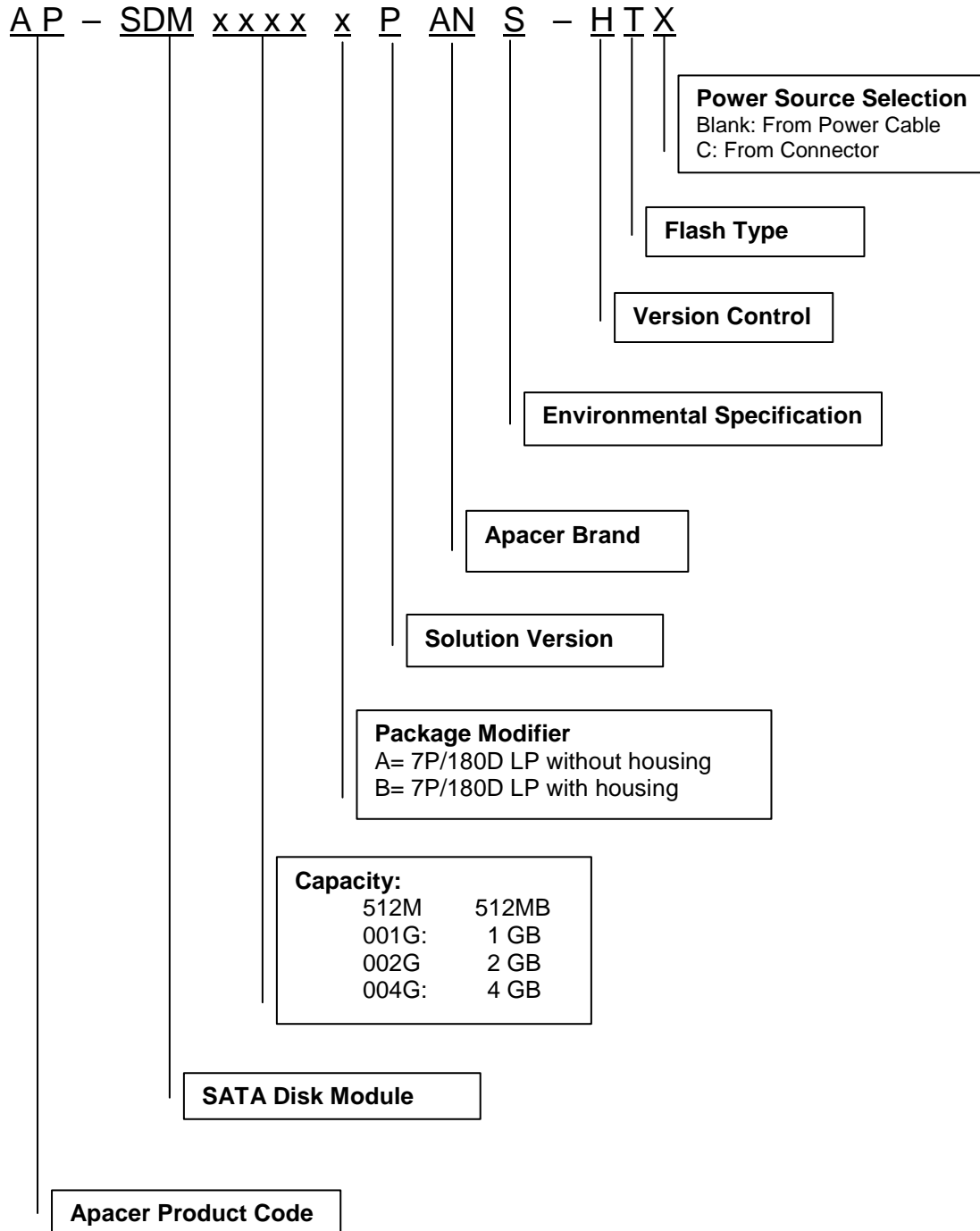
6.2.2 W/Housing



Unit: mm
Tolerance: ± 0.25

7. Product Ordering Information

7.1 Product Code Designations



7.2 Valid Combinations

7P/180D Low Profile without housing; Power Source from Cable

Capacity	Model Number
512MB	AP-SDM512MAPANS-HT
1GB	AP-SDM001GAPANS-HT
2GB	AP-SDM002GAPANS-HT
4GB	AP-SDM004GAPANS-HT

7P/180D Low Profile without housing; Power Source from Connector

Capacity	Model Number
512MB	AP-SDM512MAPANS-HTC
1GB	AP-SDM001GAPANS-HTC
2GB	AP-SDM002GAPANS-HTC
4GB	AP-SDM004GAPANS-HTC

7P/180D Low Profile with housing; Power Source from Cable

Capacity	Model Number
512MB	AP-SDM512MBPANS-HT
1GB	AP-SDM001GBPANS-HT
2GB	AP-SDM002GBPANS-HT
4GB	AP-SDM004GBPANS-HT

7P/180D Low Profile with housing; Power Source from Connector

Capacity	Model Number
512MB	AP-SDM512MBPANS-HTC
1GB	AP-SDM001GBPANS-HTC
2GB	AP-SDM002GBPANS-HTC
4GB	AP-SDM004GBPANS-HTC

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

Revision	Date	Description	Remark
1.0	10/28/2009	Official release	
1.1	11/05/2010	Added 3.3V support at supply voltage	
1.2	01/18/2011	Updated product ordering information	

Global Presence

Taiwan (Headquarters)	Apacer Technology Inc. 4 th Fl, 75 Xintai 5 th Rd., Sec.1 Hsichih, New Taipei City Taiwan, 221 R.O.C. Tel: +886-2-2698-2888 Fax: +886-2-2698-2889 amtsales@apacer.com
U.S.A.	Apacer Memory America, Inc. 386 Fairview Way, Suite102, Milpitas, CA 95035 Tel: 1-408-518-8699 Fax: 1-408-935-9611 sa@apacerus.com
Japan	Apacer Technology Corp. 5F, Matsura Bldg., Shiba, Minato-Ku Tokyo, 105-0014, Japan Tel: 81-3-5419-2668 Fax: 81-3-5419-0018 jpsservices@apacer.com
Europe	Apacer Technology B.V. Aziëlaan 22, 5232 BA 's-Hertogenbosch, The Netherlands Tel: 31-73-645-9620 Fax: 31-73-645-9629 sales@apacer.nl
China	Apacer Electronic (Shanghai) Co., Ltd 1301, No.251,Xiaomuqiao Road, Shanghai, 200032, China Tel: 86-21-5529-0222 Fax: 86-21-5206-6939 sales@apacer.com.cn
India	Apacer Technologies Pvt Ltd, #1064, 1st Floor, 7th 'A' Main, 3rd Block Koramangala, Bangalore – 560 034 Tel: +91 80 4152 9061/62/63 Fax: +91 80 4170 0215 sales_india@apacer.com